

**TSS463 VAN**  
**Van Controller Serial Interface**  
**TSS461C VAN**  
**Van Controller**

**TSS463/TSS461C**  
**VAN Controllers**  
**1999 January**

TEMIC SEMICONDUCTORS IS AN ATMEL COMPANY

## 1. Contents

<b>1. Contents</b> .....	<b>2</b>
<b>2. General Information</b> .....	<b>3</b>
<b>3. Technology Information</b> .....	<b>4</b>
3.1 WAFER PROCESS TECHNOLOGY .....	4
3.2 PRODUCT DESIGN .....	5
3.3 PACKAGE TECHNOLOGY .....	6
3.3.1 SOIC.300 16 leads.....	6
3.3.2 Other available packages .....	7
3.4 TEST .....	7
3.5 DEVICE CROSS SECTION .....	8
3.6 WAFER PROCESS CONTROL .....	9
<b>4. Qualification</b> .....	<b>10</b>
4.1 CHANGE PROCEDURE.....	11
4.2 QUALIFICATION FLOW .....	12
4.3 WAFER PROCESS QUALIFICATION .....	13
4.4 PACKAGE QUALIFICATION .....	14
4.5 DEVICE QUALIFICATION .....	16
4.5.1 ESD and Latch-up results .....	17
4.5.2 Failure Mechanisms and Corrective Actions .....	17
4.5.3 Qualification status.....	17
4.6 OUTGOING QUALITY AND RELIABILITY .....	18
4.6.1 AOQ (Average Outgoing Quality) .....	18
4.6.2 EFR (Early Failure Rate).....	19
4.6.3 LFR (Latent Failure Rate) .....	19
<b>5. User Information</b> .....	<b>20</b>
5.1 SOLDERING RECOMMENDATIONS .....	20
5.2 DRY PACK ORDERING RULES .....	20
5.3 ESD CAUTION.....	20
<b>6. Environmental Information</b> .....	<b>21</b>
<b>7. Other Data</b> .....	<b>22</b>
7.1 ISO9001 APPROVAL CERTIFICATE.....	22
7.2 DATABOOK REFERENCE.....	23
7.3 ADDRESS REFERENCE.....	23
<b>8. Revision History</b> .....	<b>24</b>

### 2. General Information

Product Name: TSS463 / TSS461C  
Function: Van Controllers  
Specific features: Serial Interface (TSS463)

Wafer process: Z86E

Available plastic package types: SOIC16 (TSS463), SOIC24 (TSS461C)

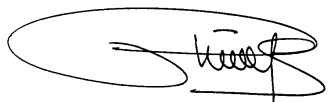
Locations:

Process, product development	TEMIC Semiconductors Nantes, France
Wafer plant	TEMIC Semiconductors Nantes, France
QC responsibility	TEMIC Semiconductors Nantes, France
Assembly	ANAM, Korea, Philippines

Probe test	TEMIC Semiconductors Nantes, France
Final test	GATEWAY Philippines ANAM Korea

Quality Assurance	TEMIC Semiconductors Nantes, France
Reliability testing	TEMIC Semiconductors Nantes, France
Failure analysis	TEMIC Semiconductors Nantes, France

Quality Assurance Management Nantes



Signed.....

## Qualpack TS80C31X2/C32X2

---

### 3. Technology Information

#### 3.1 Wafer Process Technology

Process type (Name):	CMOS (SCMOS1/2 - Z86E)
Base material:	Silicon Epi substrate type
Wafer Thickness (final)	475um
Wafer diameter	150mm
Number of masks	13
Gate oxide	
Material	Silicon dioxide
Thickness	195 A
Polysilicon	
Number of layers	1
Thickness	3000 A
Metal	
Number of layers	2
Layer 1 material	TiN/W
Layer 1 thickness	600 + 5000 A
Layer 2 material	Ti/AlCu
Layer 2 thickness	7000 A
Passivation	
Material	Si <sub>3</sub> N <sub>4</sub> on SiO <sub>2</sub>
Thickness	10000 A

### 3.2 Product Design

Die size (TSS463)	11.15mm <sup>2</sup> (3610μm*3280μm)
Die size (TSS461C)	8.46mm <sup>2</sup> (3480μm*2610μm)
Logic Effective channel length	0.8μm
Gate poly width	0.8μm
Gate poly spacing	1.2μm
Metal 1 width	1.3um
Metal 1 spacing	1.5um
Metal 2 width	1.6um
Metal 2 spacing	1.6um
Contact size	1.0μm
Via size	1.4μm

## Qualpack TS80C31X2/C32X2

---

### 3.3 Package Technology

#### 3.3.1 SOIC.300 16 leads

Package weight	0,43 g	
Chip separation method		Sawing
Lead frame		
Material	Cu	
Thickness	10 mils	
Size	270*270 mils <sup>2</sup>	
Lead plating	Electroplated Sn/Pb 85/15	
Die attach		
Material	Silver epoxy	
Type	Ablestick 84-1 LMISR4	
Wire bonding		
Material	Gold	
Diameter	33um	
Method	Thermosonic	
Molding		
Material	Nitto MP8000AN	
Flammability rating	UL94V-0	
Marking		
Method	Printed ink	
Coding example	TEMIC <i>optional special customer marking</i> TSS463 YY MM	
Dry packing	No	
Tube packed		
Primary	Tube	
Material	Antistatic PVC	
Number per unit	47	
Secondary	Box	
Material	Cardboard	
Number per unit	1692	
Labelling (minimum)	Device type, Quantity, Date Code, Prod. code	
Bar coding	Code 39 to EIA-556-A	

### Tape packed

Primary

Material

Number per unit

Secondary

Material

Number per unit

Labelling (minimum)

Bar coding

Tape

Antistatic PVC

31

Box

Cardboard

1116

Device type, Quantity, Date Code, Prod. code

Code 39 to EIA-556-A

### 3.3.2 Other available packages

No other package available

### Dry packing

SOIC 16

SOIC 24

No

No

### 3.4 Test

Probe equipment

Probe temperature

Sentry 15

125°C

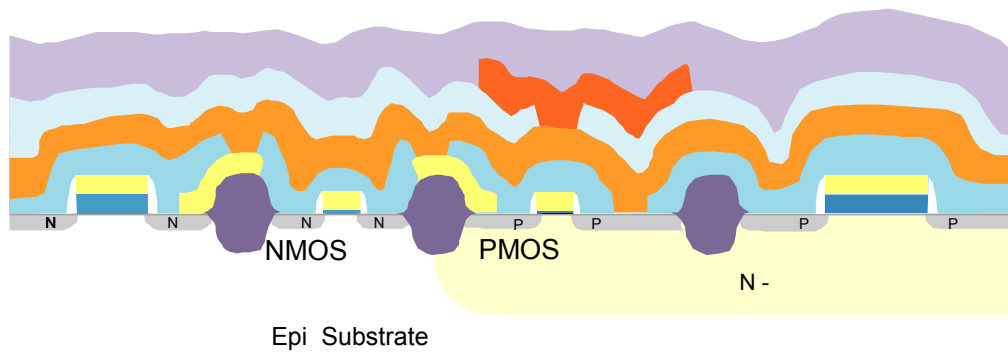
Test equipment

Test temperature

Sentry 15

25°C, 125°C(sampling)

3.5 Device Cross Section

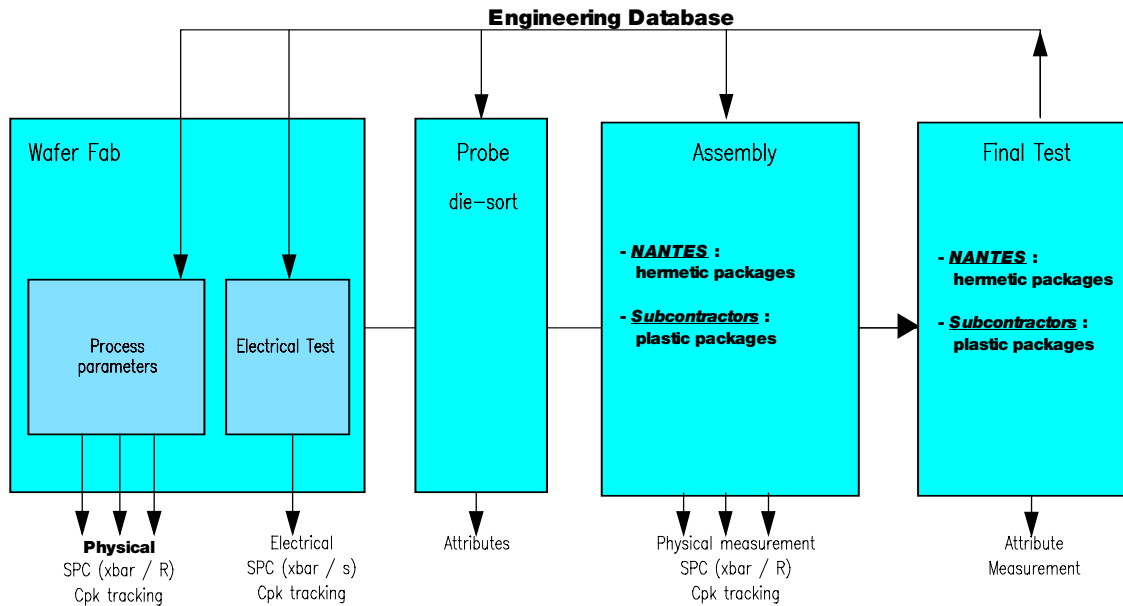


- |   |   |   |   |
|---|---|---|---|
|  Thin Oxide  |  Planarization |  Transversal Isolation Oxide |  Passivation |
|  Polysilicon |   |  Metal 1                     |  Metal 2     |



### 3.6 Wafer Process Control

All the inspections and controls are defined as a process step in the production management software, and are led by using a centralized SPC software. PC system could be summarized as follows:

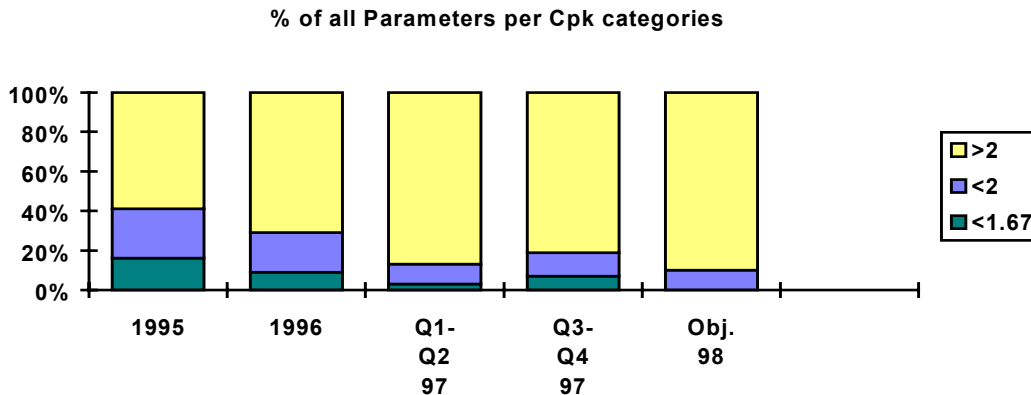


Critical process parameters are identified by using F.M.E.A. and other advanced tools.

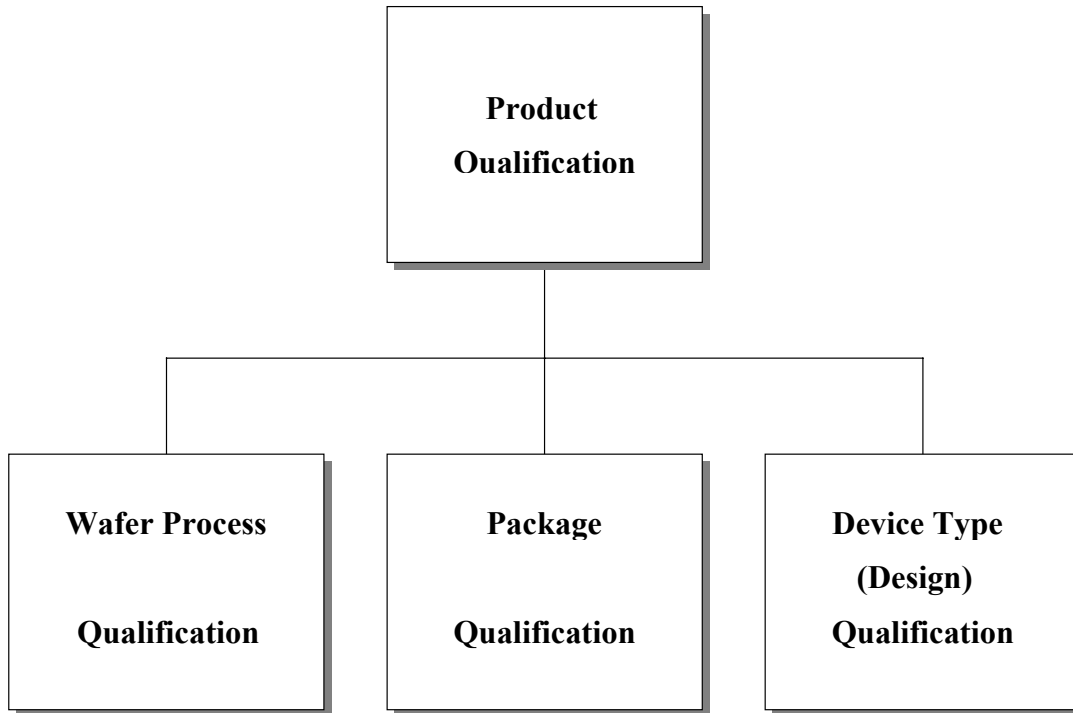
Those parameters are followed in real time with the SPC methodology and their capability is measured and monthly reported in the Operation Review.

For end 1997, the Cpk target is the following :

**all parameters with Cpk above 1.67**



#### 4. Qualification



All product qualifications are split into three distinct steps as shown above. This same procedure is also used to qualify a change. Before a product is released for use, it must have been manufactured using a qualified wafer and package process. Before a device is released for production processing, it must also have successfully completed its required specific qualification.

The standard tests which are used for this procedure are shown in the section "**Qualification Flow**"

### 4.1 Change Procedure

All changes are controlled by ECN (Engineering Change Notice). All major changes are notified to those customers using products which are affected by the change.

A major change is defined as a change which affects the electrical and/or mechanical specification as defined in the datasheet or which affects the following parameters as defined hereafter:

<b>1</b>	<b>General Major Changes</b>
1-1	Manufacturing line
1-2	Sequence of fabrication process cycle
1-3	Material
1-4	Electrical parameter
1-5	Dimension
1-6	Pad location
1-7	Die size

<b>2</b>	<b>Changes specific to wafer fabrication area</b>
2-1	Doping process
2-2	Gate oxide formation method
2-3	Equipement change
2-4	Layer thickness
2-5	Module dimensions

<b>3</b>	<b>Changes specific to to assembly process area</b>
3-1	Sawing process
3-2	Die attach process
3-3	Wire interconnect method
3-4	Molding process
3-5	Tinning process

<b>4</b>	<b>Changes specific to test area</b>
4-1	Specification limit
4-2	Test coverage reduction
4-3	Product identification
4-4	Final conditioning

## Qualpack TS80C31X2/C32X2

### 4.2 Qualification Flow

#### General Requirements for Plastic packaged CMOS IC

Standard	Test Description	Qualification type (acceptance)
MIL-STD 883D Method 1005	<b>Electrical Life Test (Early Failure Rate)</b> 12 hours 150°C (Tj) 5.75V	Device (1/2000 12h)
MIL-STD 883D Method 1005	<b>Electrical Life Test (Latent Failure Rate)</b> 1000 hours 150°C 5.75V Dynamic or Static	Device (0/116 500h)
MIL-STD 883D Method 3015.7	<b>Electrostatic Discharge HBM</b> +/-2000v 1.5kOhm/100pF/3 pulses	Device (0/3 per level)
JEDEC 17	<b>Latch up</b> 50mW power injection 125°C	Device (0/10)
MHS PAQA0046	<b>PROM Dataretention</b> High Temperature Storage 165°C	Device (0/45 500h)
MIL-STD 883D Method 1010	<b>Temperature Cycling</b> 1000 cycles -65°C/150°C air/air	Device and Package (0/45 500c)
MHS PAQA0184	<b>Pressure Pot after Mounting Stress</b> 168 hours 130°C/85%RH	Device and Package (0/45 168h)
EIA JESD22-A101	<b>85/85 Humidity Test</b> 1000 hours 85°C/85%RH	Die and Package (0/45 500h)
EIA JESD22-A110	<b>HAST</b> 336 hours 130°C/85%RH/5.5V	Device and Package (0/45 168h)
EIA JESD22-A112	<b>Resistance to Soldering Heat</b> Infra Red Stress 220°C/25s/3 times	Package (0/10 per class)
MIL-STD 883D Method 2003	<b>Solderability</b>	Package (0/3)
MIL-STD 883D Method 2015	<b>Marking Permanency</b>	Package (0/3)

### 4.3 Wafer Process Qualification

This section summarizes the global 1998 reliability results of the products manufactured with the same technology as the VAN TSS463 and TSS461C (Z86 processes).

Wafer Process	Device Types	Test Description	Step	Result	Comment
Z86	Microcontrollers and dedicated	EFR Dynamic Life Test	12h	3/22888	
		LFR Dynamic Life Test	500h 1000h	1/1155	
Z86	Memory, Asic,	EFR Dynamic Life Test	12h	1/5209	
		LFR Dynamic Life Test	500h 1000h	1/685	
Z86	TSS463	EFR Dynamic Life Test	12h	Estimated	65 ppm
		LFR Dynamic Life Test	500h 1000h		3.9 fit
Z86	TSS461C	EFR Dynamic Life Test	12h	Estimated	49 ppm
		LFR Dynamic Life Test	500h 1000h		2.9 fit
		Failure mechanisms	All	50% 17% 17% 17%	Poly silicide defect metal resistor shift bonding
Global	All products	EFR Dynamic Life Test	12h	4/28097	165 ppm (20mm <sup>2</sup> )
		LFR Life Test	500h 1000h	2/1840	10 fit (20mm <sup>2</sup> )

## Qualpack TS80C31X2/C32X2

### 4.4 Package Qualification

This section presents TSS463 and TSS461C package qualification results, including additional measurements intending to fulfil Q100 Automotive Standard requirements.

Lot Number	Device Type	Test Description	Step	Result	Comment
Z21538F	TSS463 in SO 16 (1)	Thermal Cycles 85/85 Humidity Resistance to Soldering Heat HAST after Soldering Stress (with 5.5v bias)	1000c 2000c 1000h 2000h Level 1 Level 3 168h	0/45 0/45 0/45 0/45 1/10 0/10 0/45	1 die top delamination
Z21997A	TSS463 in SO 16 (2)	Thermal Cycles 85/85 Humidity HAST after Soldering Stress 165c HT Storage Physical Dimensions Bonding Destructive Tests (4) Resistance to Soldering Heat	500c 1000c 500h 1000h 168h SAM 500h 1000h Visual WP BS Level 1 Level 2 Level 5	0/45 0/45 (3) 0/45 0/45 (3) 0/45 (3) 0/10 0/45 0/45 0/5 0/30 (5) 0/30 0/10 0/10 0/10	AVG=77.3 STD=8.9 CPK=1.8 MAX=98.9 MIN=61.1 AVG=17.4 STD=1.5 CPK=2.3 MAX=21.1 MIN=14.3
W28184C	29C461B in SO 24 (1)	Thermal Cycles 85/85 Humidity HAST after Soldering Stress	500c 1000c 500h 1000h 168h	0/45 0/45 0/45 0/45 0/45	
Z04948C	TSS461C	Thermal Cycles 85/85 Humidity HAST after Soldering Stress HAST 5.5V	500c 1000c 500h 1000h 168h 168h 336h	0/45 0/45 0/45 0/45 0/45 0/45 0/45	

Lot Number	Device Type	Test Description	Step	Result	Comment
Z20569K	HMT-65664A in SO 28 (2)	Thermal Cycles	500c	0/45	
			1000c	0/45	
		85/85 Humidity	500h	0/45	
			1000h	0/45	
			2000h	0/45	
		Resistance to Soldering Heat	Level 1	0/10	
		Marking Permanency	-	0/3	
HAST after Soldering Stress (with 5.5v bias)	168h	0/45			
Global	All products	Mounting Stress level 1	Elect.	0/255	0 ppm
		Climatic Tests	-	0/720	0 %

Notes:

- (1) SUMITOMO 6300 molding compound
- (2) NITTO MP8000 molding compound
- (3) Electrical test with Quality program at 25°C, 125°C and -40°C
- (4) Performed on molded device opened using acid
- (5) No Lifted Ball Bond, breakdown observed on wires (83%) and over the stich (17%)

## Qualpack TS80C31X2/C32X2

### 4.5 Device Qualification

This section presents TSS463 and TSS461C device qualification results, including additional measurements intending to fulfil Q100 Automotive Standard requirements.

Lot Number	Device Type	Test Description	Step	Result	Comment
Z21538F	TSS463 in SO 16	EFR Dynamic Life Test	12h	0/261	
		LFR Dynamic Life Test	500h	0/116	
			1000h	0/116	
Z21997	TSS463 in SO 16	EFR Dynamic Life Test	12h	0/800	
			48h	0/304	
		LFR Dynamic Life Test	500h	0/45	
			1000h	0/45 (6)	
W28184C	29C461B in SO 24	EFR Dynamic Life Test	12h	0/298	
		LFR Dynamic Life Test	500h	0/72	
			1000h	0/72	
Z04948C	TSS461C in SO 24	EFR Dynamic Life Test	12h	0/296	
		LFR Dynamic Life Test	500h	0/78	
			1000h	0/78	
Global	All products	EFR Dynamic Life Test	12h	0/1655	0 ppm measured
		LFR Dynamic Life Test	500h	0/311	18 fit measured
			1000h	0/311	

Notes:

- (6) Electrical test with Quality program at 25°C, 125°C and -40°C



### 4.5.1 ESD and Latch-up results

Lot Number	Device Type	Test Description	Step	Result	Comment
Z21538B	TSS463 SO 16	ESD HBM model	3000v	0/10	CLASS 2 Leakage pin 6
			4000v	1/13	
			4500v	0/4	
		ESD CDM model	5000v	3/13	Leakages pin 2,6,15 CLASS C6 (EOS/ESD of association)
			1500v	0/10	
			Latch up Vcc overstress	10v	
LU power injection	50mW	0/10			
Z19814	TSS461C DIL 24.3	ESD HBM model	3000v	0/5	CLASS 2 Leakages CLASS C6
			4000v	3/3	
		ESD CDM model	1500v	0/4	
	TSS461C	Latch up Vcc overstress	10v	0/10	
		LU power injection	50mW	0/10	

### 4.5.2 Failure Mechanisms and Corrective Actions

Failure Mechanism	Root Cause	Corrective Action	Date	Effect	Check of Efficiency
Poly silicide defects	Process conditions	Reduce silicide temperature, increase duration	Nov 97	Robustness improved	EFR monitoring
Die top delamination	Sumitomo6300 molding compound	Move to Nitto MP8000	Jan 98	No more moitures sensitivity	pass level 1 of JESD 22 A112

### 4.5.3 Qualification status

The Wafer Process and the assembly are qualified and controlled by regular monitoring.

The TSS461C VAN is full qualified since 1996 July.  
The TSS463 VAN is full qualified since 1997 October.

Additional measurements done in 1998 and generic results demonstrate compliance of the two products to Q100 Automotive Standard.

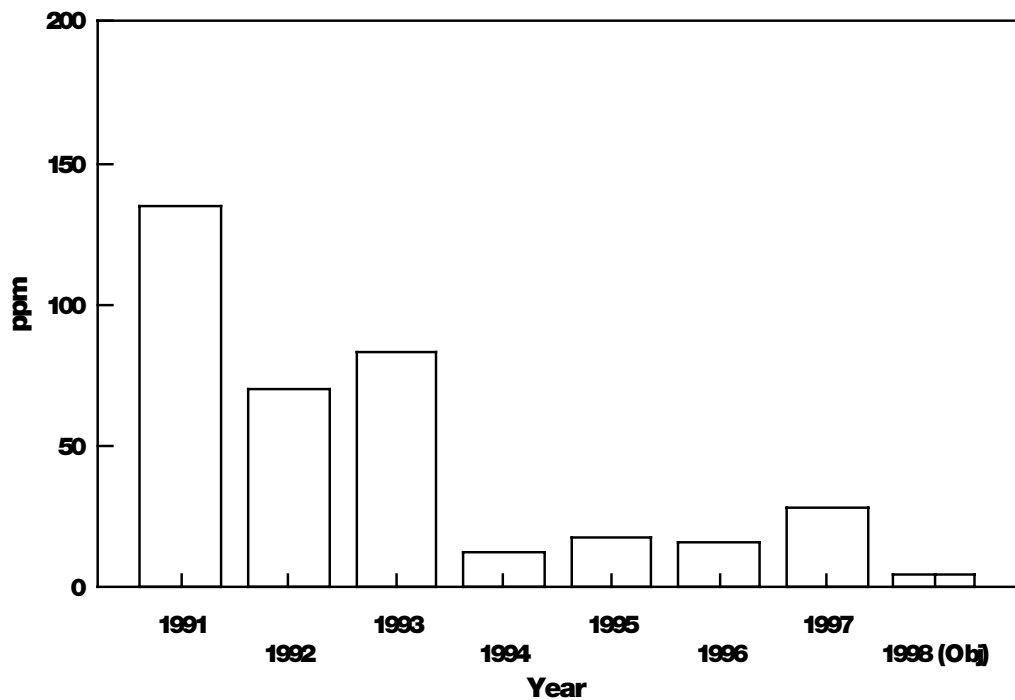
## Qualpack TS80C31X2/C32X2

---

### Outgoing Quality and Reliability

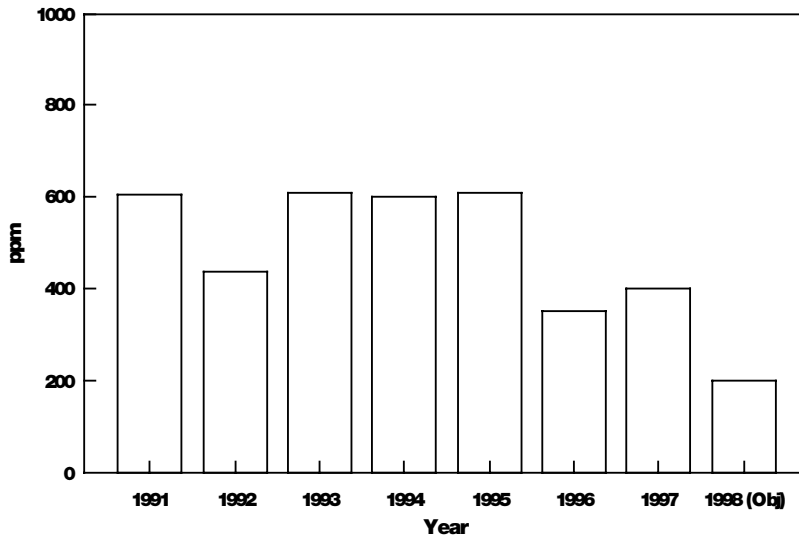
#### 4.5.4 AOQ (Average Outgoing Quality)

The AOQ is measured following 100% test by sampling outgoing product. The results of this inspection are recorded in ppm (parts per million) using the method defined in JEDEC 16. The figures below cover the last years for both the subject and structurally similar products.



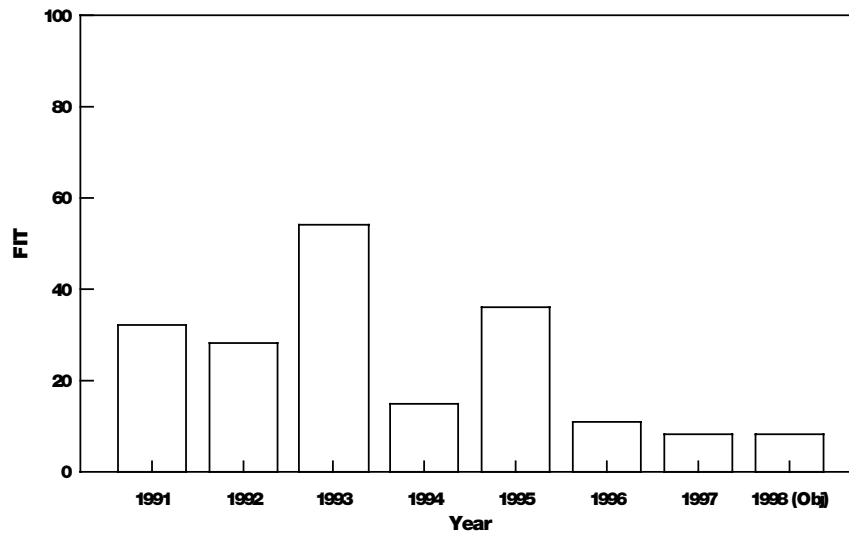
### 4.5.5 EFR (Early Failure Rate)

The EFR is measured on a sample of devices by operating them at an elevated temperature and measuring the number which fails to meet specification after 12 hours at 150°C. The figure is expressed in terms of ppm.



### 4.5.6 LFR (Latent Failure Rate)

The LFR is measured by operating devices at elevated temperatures for 1000 hours and measuring the failure rate. Using the Arrhenius law, the expected failure rate at a operating temperature of 55°C is calculated using an activation Energy of 0.6 eV with a confidence level of 60%. This is expressed in units per billion hours (FIT).



## 5. User Information

### 5.1 Soldering Recommendations

For DRY PACKED products, TEMIC recommends to strictly follow the procedure described hereunder:

- Dry packed products must not be stored more than 1 year at 40°C - 90%rh (worst storage conditions assumed)
  
- A longer storage period is allowed taking into account the following conditions:  
5 years max at 25°C (+/-5°C) - 50%rh
  
- From opening of the packs, the product must be assembled within 48 hours.  
(worst in-process storage condition assumed: 30°C - 60%rh)
  
- If they cannot be soldered within this time period, then the pieces must be dried at 125°C for 24 hours. Only one drying is allowed.
  
- Max relative humidity allowed in the bag is 20% (readable on the indicator inside the bag). If this value is reached, then the parts must be dried at 125°C for 24 hours before mounting.
  
- For high sensitive products, the delay between pack opening and assembly is reduced to 6 hours (Level 6 of JEDEC 22-A112). In this case, a warning printed on each pack advises the user of this restriction .

### 5.2 DRY PACK Ordering rules

TEMIC qualification procedure allows to classify products according to JEDEC 22-A112 and to determine the convenient conditioning for safe customer use.

Nevertheless, even if the product is not classified as moisture sensitive, it is possible (for example if storage conditions are not properly controlled) to order product with a Dry Pack.

In this case the product name suffix will be ":D" or ":xD".

### 5.3 ESD caution

The user must protect components against EOS and ESD damages by grounding personal and workstations.

## **6. Environmental Information**


The TEMIC Environmental Policy aims at:

- Reducing the use of harmful chemicals in its processes
- Reducing the content of harmful materials in its products
- Using re-cyclable materials wherever possible
- Reducing the energy content of its products

As part of that plan, Ozone Depleting Chemicals are being replaced either by TEMIC / MHS or its sub-contractor's processes.

7. Other Data

7.1 ISO9001 Approval Certificate



**CERTIFICAT**      **CERTIFICATE**

**N° QUAL/1991/275**

*L'AFAQ certifie que le système qualité adopté par,  
AFAQ certifies that the quality system developed by :*

**MATRA MHS**

*pour les activités suivantes,  
for the following activities :*

**CONCEPTION ET PRODUCTION DE CIRCUITS INTEGRES ET ASICS.**

**DESIGN AND PRODUCTION OF INTEGRATED CIRCUITS AND ASICS.**

*exercées sur le(s) site(s) suivant(s),  
carried out in the following location(s) :*

**La Chantrerie F-44087 NANTES**



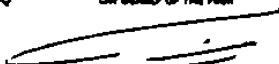
*a été évalué et jugé conforme aux exigences de la norme,  
has been assessed and found to conform to the requirements of the standard :*

**ISO 9001 (1994)**

*Le présent certificat, délivré dans les conditions fixées par l'AFAQ, est valable jusqu'au,  
This certificate, delivered under AFAQ rules, is valid until :*

**2000-07-17**

*(année-mois-jour)      Signeux, le      1997-07-18      (year-month-day)*

<p><small>LE PRÉSIDENT DU COMITÉ DE CERTIFICATION THE PRESIDENT OF THE CERTIFICATION COMMITTEE</small></p>  <p><b>A. PIGEONNIER</b></p>	<p><small>LE DIRECTEUR GÉNÉRAL DE L'AFAQ THE MANAGING DIRECTOR OF AFAQ</small></p>  <p><b>O. PEYRAT</b></p>	<p><small>LE REPRÉSENTANT DE L'ENTREPRISE ON BEHALF OF THE FIRM</small></p>  <p><b>F. FAES</b></p>
--	--	--

### 7.2 Databook Reference

Direct access on the web to datasheet at:

**<http://www.temic-semi.com>**

Select:      Products  
                 Automotive ICs  
                 Multiplex ICs

### 7.3 Address Reference

All enquiries relating to this document should be addressed to the following:

TEMIC Semiconductors  
BP70602  
44306 Nantes Cedex 3  
France  
Telephone (33) 2 40 18 18 18  
Telefax    (33) 2 40 18 19 20

Or direct contact same address  
Pascal LECUYER  
Quality Engineer  
Telephone (33) 2 40 18 17 73  
Telefax    (33) 2 40 18 19 00

## 8. Revision History

Issue	Modification Notice	Application Date
0	TSS463 VAN Qualification Report	1997 October
1	Qualpack TSS463 Van	1998 February
2	Qualpack TSS463 and TSS461C VAN CONTROLLERS	1999 January

### Remarks:

The information given in this document is believed to be accurate and reliable. However, no responsibility is assumed by TEMIC for its use. No specific guarantee or warranty is implied or given by this data unless agreed in writing elsewhere.

TEMIC reserve the right to update or modify this information without notification , at any time, in the interest of providing the latest information.

Parts of this publication may be reproduced without special permission on the condition that our author and source are quoted and that two copies of such extracts are placed at our disposal after publication. Before use of such reproduced material the user should check that the information is current.

Written permission must be obtained from the publisher for complete reprints or translations.