



TN8, TS8 and TYNx08 Series

SENSITIVE & STANDARD

8A SCRs

Table 1: Main Features

Symbol	Value	Unit
$I_{T(RMS)}$	8	A
V_{DRM}/V_{RRM}	600 to 1000	V
I_{GT}	0.2 to 15	mA

DESCRIPTION

Available either in sensitive (**TS8**) or standard (**TN8 / TYN**) gate triggering levels, the 8A SCR series is suitable to fit all modes of control, found in applications such as overvoltage crowbar protection, motor control circuits in power tools and kitchen aids, inrush current limiting circuits, capacitive discharge ignition and voltage regulation circuits...

Available in through-hole or surface-mount packages, they provide an optimized performance in a limited space area.

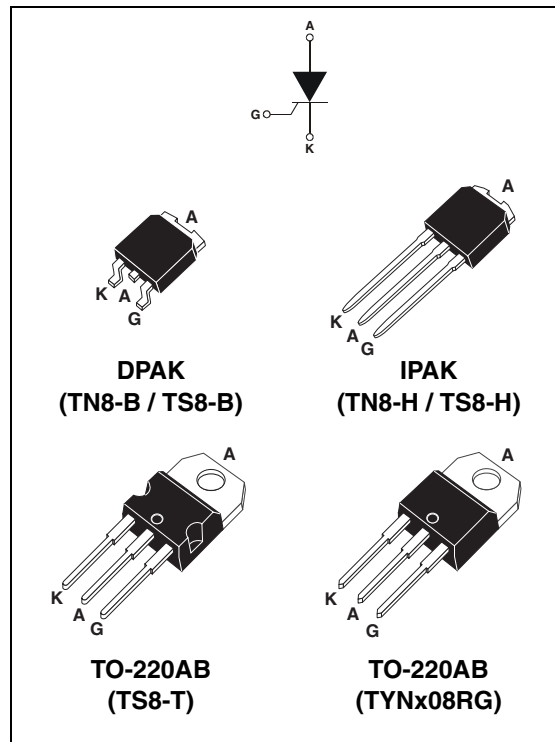


Table 2: Order Codes

Part Numbers	Marking
TN805-x00B	TN805x00
TN805-x00B-TR	TN805x00
TN805-x00H	TN805x00
TN815-x00B	TN815x00
TN815-x00B-TR	TN815x00
TN815-x00H	TN815x00
TS820-x00B	TS820x00
TS820-x00B-TR	TS820x00
TS820-x00H	TS820x00
TS820-x00T	TS820x00T
TYNx08RG	TYNx08

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Table 3: Absolute Ratings (limiting values)

Symbol	Parameter		Value		Unit	
			TS8/TN8	TYN08		
$I_{T(RMS)}$	RMS on-state current (180° conduction angle)	$T_c = 110^\circ\text{C}$	8		A	
$I_{T(AV)}$	Average on-state current (180° conduction angle)	$T_c = 110^\circ\text{C}$	5		A	
I_{TSM}	Non repetitive surge peak on-state current	$t_p = 8.3\text{ ms}$	$T_j = 25^\circ\text{C}$	73	100	A
		$t_p = 10\text{ ms}$		70	95	
I^2t	I^2t Value for fusing	$t_p = 10\text{ ms}$	$T_j = 25^\circ\text{C}$	24.5	45	A^2s
di/dt	Critical rate of rise of on-state current $I_G = 2 \times I_{GT}$, $t_r \leq 100\text{ ns}$	$F = 60\text{ Hz}$	$T_j = 125^\circ\text{C}$	50		$\text{A}/\mu\text{s}$
I_{GM}	Peak gate current	$t_p = 20\text{ }\mu\text{s}$	$T_j = 125^\circ\text{C}$	4		A
$P_{G(AV)}$	Average gate power dissipation		$T_j = 125^\circ\text{C}$	1		W
T_{stg} T_j	Storage junction temperature range Operating junction temperature range			- 40 to + 150 - 40 to + 125		$^\circ\text{C}$
V_{RGM}	Maximum peak reverse gate voltage (for TN8 & TYN08 only)			5		V

Tables 4: Electrical Characteristics ($T_j = 25^\circ\text{C}$, unless otherwise specified)

■ SENSITIVE

Symbol	Test Conditions			TS820	Unit	
I_{GT}	$V_D = 12\text{ V}$ $R_L = 140\text{ }\Omega$		MAX.	200	μA	
V_{GT}			MAX.	0.8	V	
V_{GD}	$V_D = V_{DRM}$ $R_L = 3.3\text{ k}\Omega$ $R_{GK} = 220\text{ }\Omega$	$T_j = 125^\circ\text{C}$	MIN.	0.1	V	
V_{RG}	$I_{RG} = 10\text{ }\mu\text{A}$		MIN.	8	V	
I_H	$I_T = 50\text{ mA}$ $R_{GK} = 1\text{ k}\Omega$		MAX.	5	mA	
I_L	$I_G = 1\text{ mA}$ $R_{GK} = 1\text{ k}\Omega$		MAX.	6	mA	
dV/dt	$V_D = 65\% V_{DRM}$ $R_{GK} = 220\text{ }\Omega$	$T_j = 125^\circ\text{C}$	MIN.	5	$\text{V}/\mu\text{s}$	
V_{TM}	$I_{TM} = 16\text{ A}$ $t_p = 380\text{ }\mu\text{s}$		$T_j = 25^\circ\text{C}$	MAX.	1.6	V
V_{t0}	Threshold voltage		$T_j = 125^\circ\text{C}$	MAX.	0.85	V
R_d	Dynamic resistance		$T_j = 125^\circ\text{C}$	MAX.	46	$\text{m}\Omega$
I_{DRM} I_{RRM}	$V_{DRM} = V_{RRM}$ $R_{GK} = 220\text{ }\Omega$	$T_j = 25^\circ\text{C}$	MAX.	5	μA	
		$T_j = 125^\circ\text{C}$		1	mA	

■ STANDARD

Symbol	Test Conditions		TN805	TN815	TYNx08	Unit		
I_{GT}	$V_D = 12\text{ V}$	$R_L = 33\ \Omega$	MIN.	0.5	2	2	mA	
			MAX.	5	15	15		
V_{GT}			MAX.	1.3		V		
V_{GD}	$V_D = V_{DRM}$	$R_L = 3.3\text{ k}\Omega$	$T_j = 125^\circ\text{C}$	MIN.	0.2		V	
I_H	$I_T = 100\text{ mA}$ Gate open		MAX.	25	40	30	mA	
I_L	$I_G = 1.2\ I_{GT}$		MAX.	30	50	70	mA	
dV/dt	$V_D = 67\% V_{DRM}$	Gate open	$T_j = 125^\circ\text{C}$	MIN.	50	150	150	V/ μs
V_{TM}	$I_{TM} = 16\text{ A}$	$t_p = 380\ \mu\text{s}$	$T_j = 25^\circ\text{C}$	MAX.	1.6		V	
V_{t0}	Threshold voltage		$T_j = 125^\circ\text{C}$	MAX.	0.85		V	
R_d	Dynamic resistance		$T_j = 125^\circ\text{C}$	MAX.	46		m Ω	
I_{DRM} I_{RRM}	$V_{DRM} = V_{RRM}$		$T_j = 25^\circ\text{C}$	MAX.	5		μA	
			$T_j = 125^\circ\text{C}$		2		mA	

Table 6: Thermal resistance

Symbol	Parameter		Value	Unit	
$R_{th(j-c)}$	Junction to case (D.C.)		20	$^\circ\text{C}/\text{W}$	
$R_{th(j-a)}$	Junction to ambient (D.C.)	$S = 0.5\text{ cm}^2$	DPAK	70	$^\circ\text{C}/\text{W}$
			IPAK	100	
			TO-220AB	60	

S = Copper surface under tab.

Figure 1: Maximum average power dissipation versus average on-state current

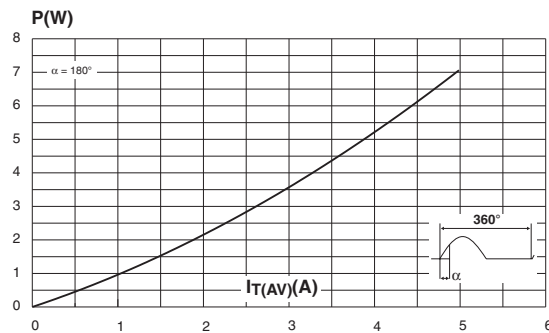
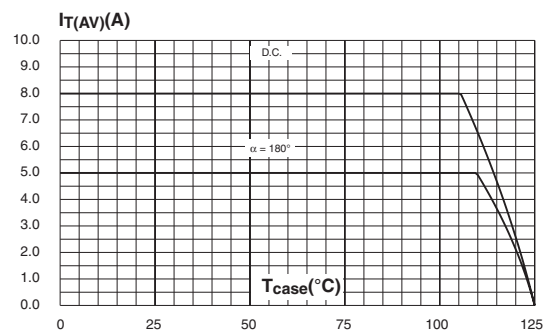


Figure 2: Average and D.C. on-state current versus case temperature



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Figure 3: Average and D.C. on-state current versus ambient temperature (device mounted on FR4 with recommended pad layout) (DPAK)

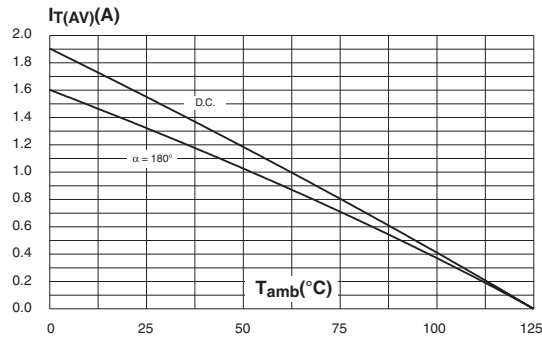


Figure 4: Relative variation of thermal impedance junction to case versus pulse duration

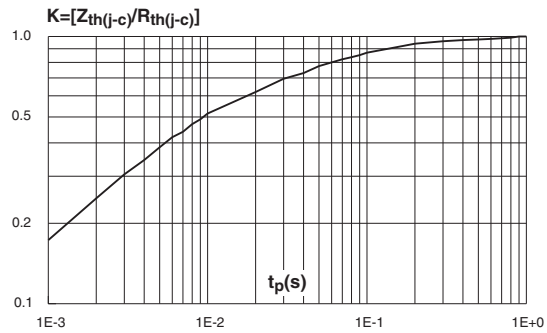


Figure 5: Relative variation of thermal impedance junction to ambient versus pulse duration (recommended pad layout, FR4 PC board for DPAK)

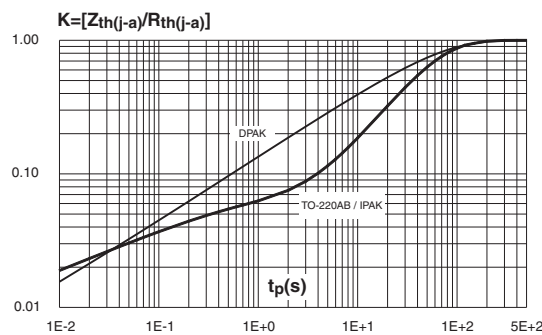


Figure 6: Relative variation of gate trigger current and holding current versus junction temperature for TS8 series

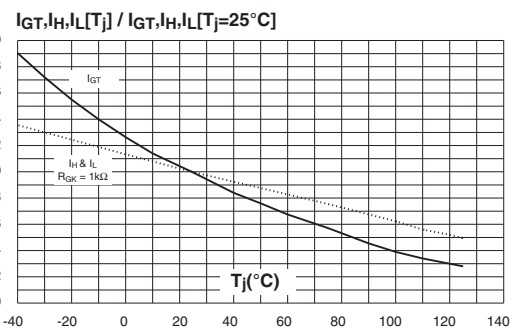


Figure 7: Relative variation of gate trigger current and holding current versus junction temperature for TN8 & TYN08 series

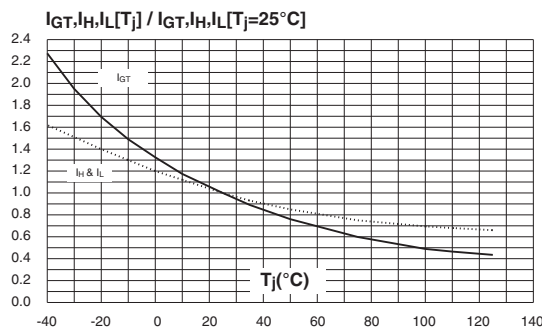


Figure 8: Relative variation of holding current versus gate-cathode resistance (typical values) for TS8 series

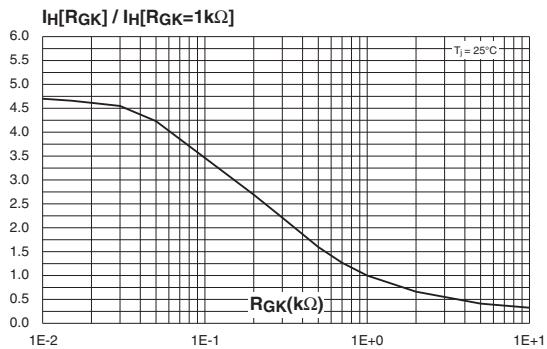


Figure 9: Relative variation of dV/dt immunity versus gate-cathode resistance (typical values) for TS8 series

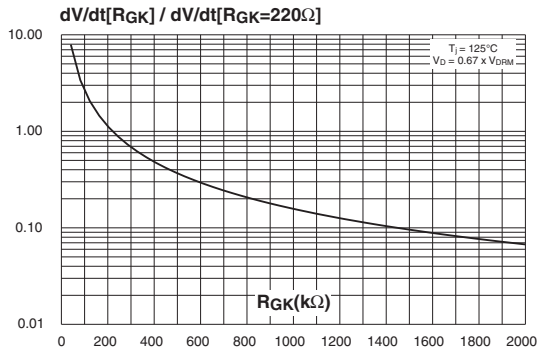


Figure 10: Relative variation of dV/dt immunity versus gate-cathode capacitance (typical values) for TS8 series

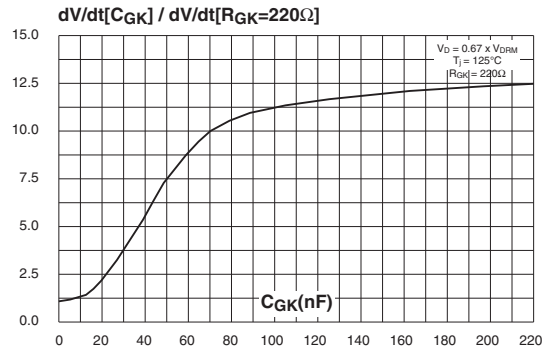


Figure 11: Surge peak on-state current versus number of cycles

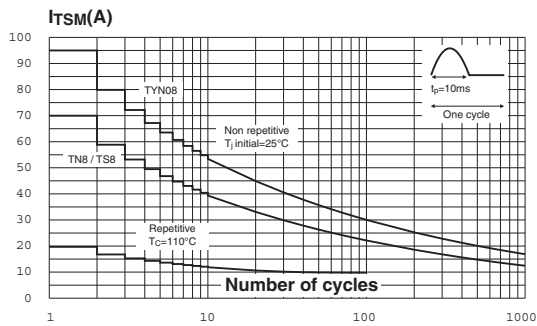


Figure 12: Non-repetitive surge peak on-state current for a sinusoidal pulse with width $t_p < 10\text{ ms}$, and corresponding values of I^2t

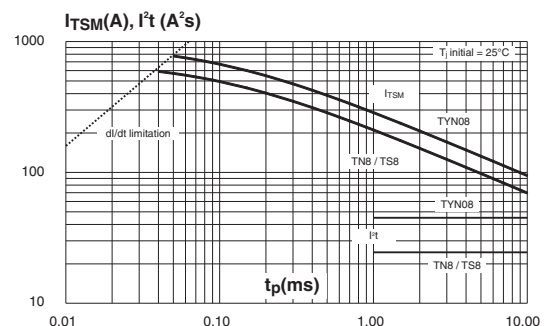


Figure 13: On-state characteristics (maximum values)

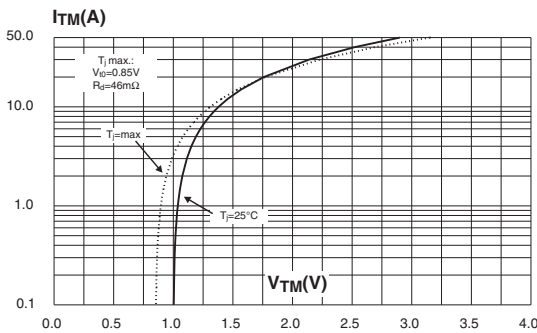
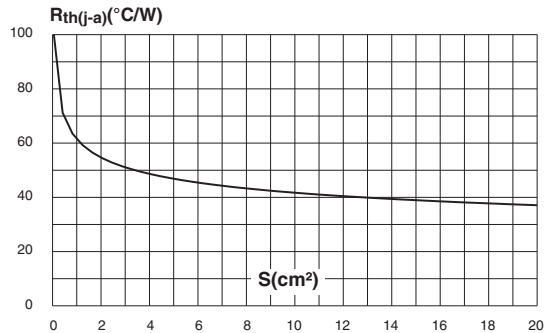


Figure 14: Thermal resistance junction to ambient versus copper surface under tab (epoxy printed circuit board FR4, copper thickness: 35μm) (DPAK)



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Figure 17: Ordering Information Scheme (TN8 series)

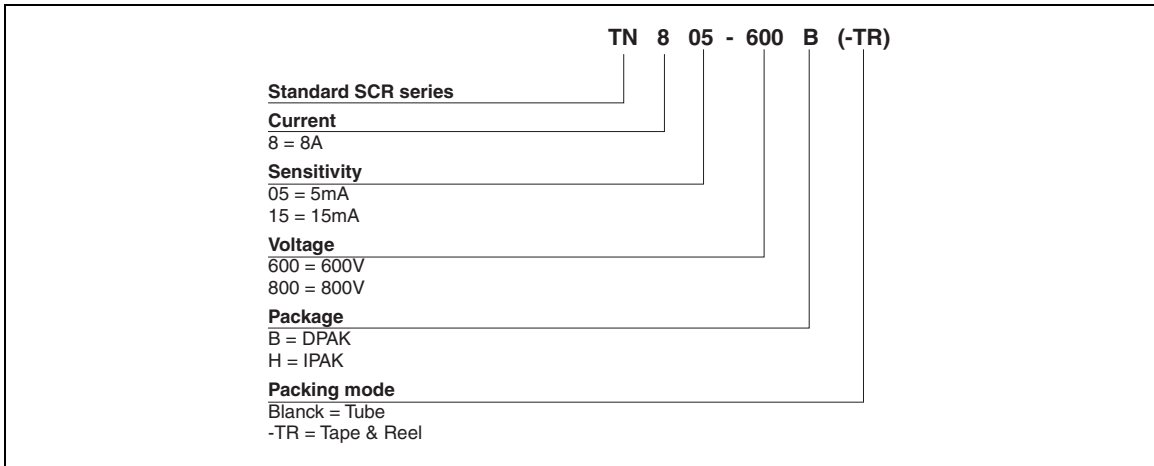


Figure 18: Ordering Information Scheme (TS8 series)

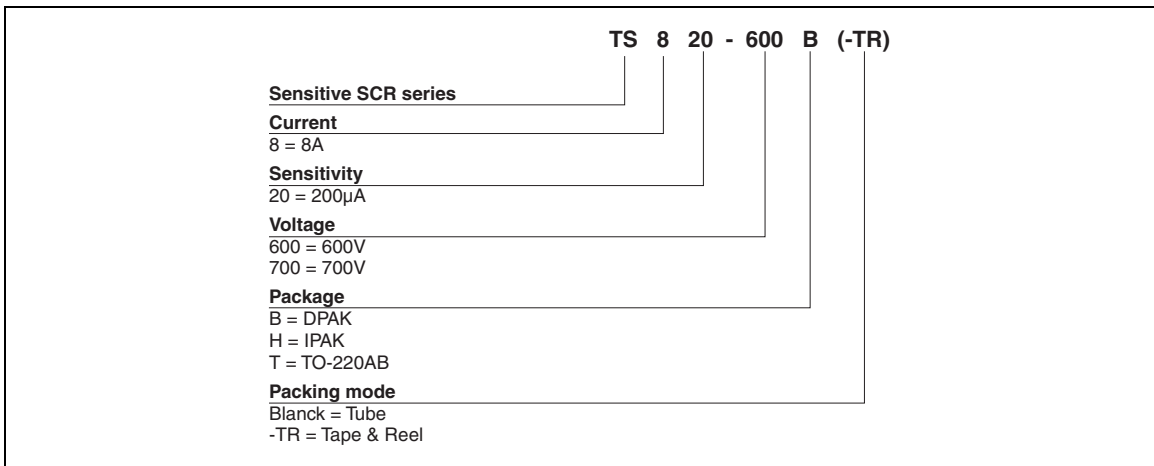


Figure 19: Ordering Information Scheme (TYN08 series)

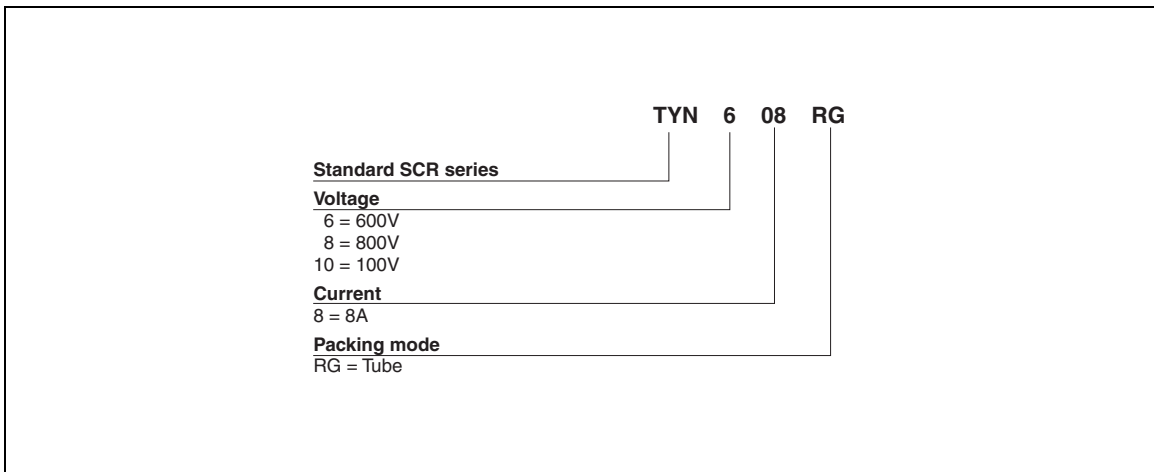


Table 7: Product Selector

Part Numbers	Voltage (xxx)				Sensitivity	Package
	600 V	700 V	800 V	1000 V		
TN805-xxxB	X		X		5 mA	DPAK
TN805-xxxH	X		X		5 mA	IPAK
TN815-xxxB	X		X		15 mA	DPAK
TN815-xxxH	X		X		15 mA	IPAK
TS820-xxxB	X	X			0.2 mA	DPAK
TS820-xxxH	X	X			0.2 mA	IPAK
TS820-xxxT	X	X			0.2 mA	TO-220AB
TYNx08RG	X		X	X	15 mA	TO-220AB

Figure 20: DPAK Package Mechanical Data

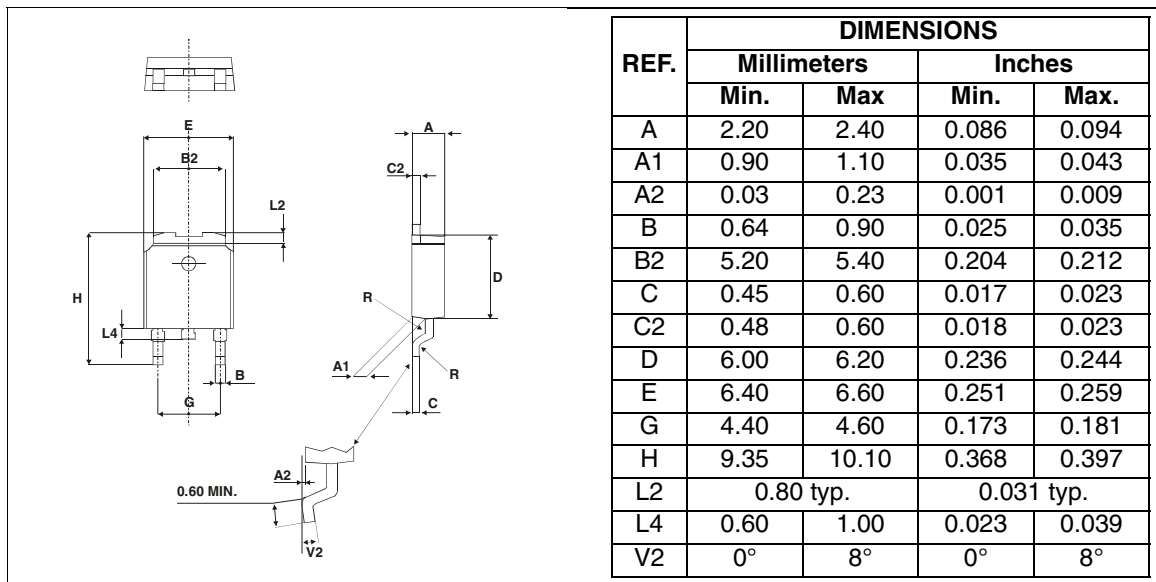


Figure 21: DPAK Foot Print Dimensions (in millimeters)

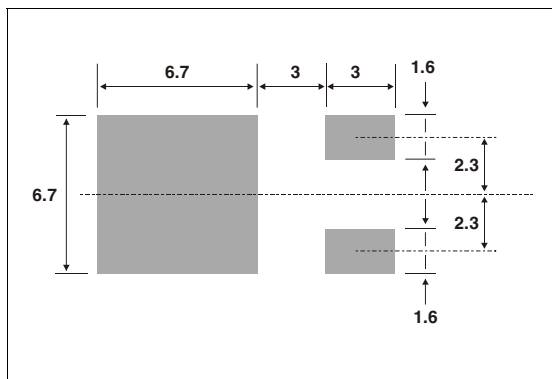


Figure 22: IPAK Package Mechanical Data

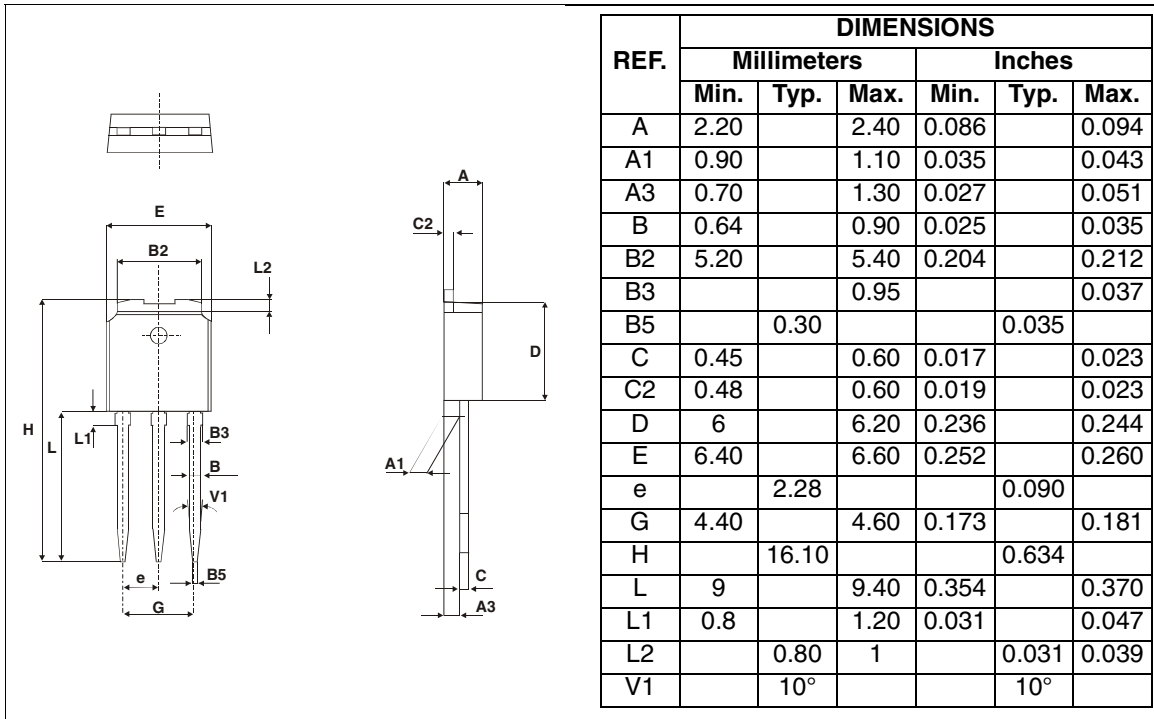


Figure 23: TO-220AB Package Mechanical Data

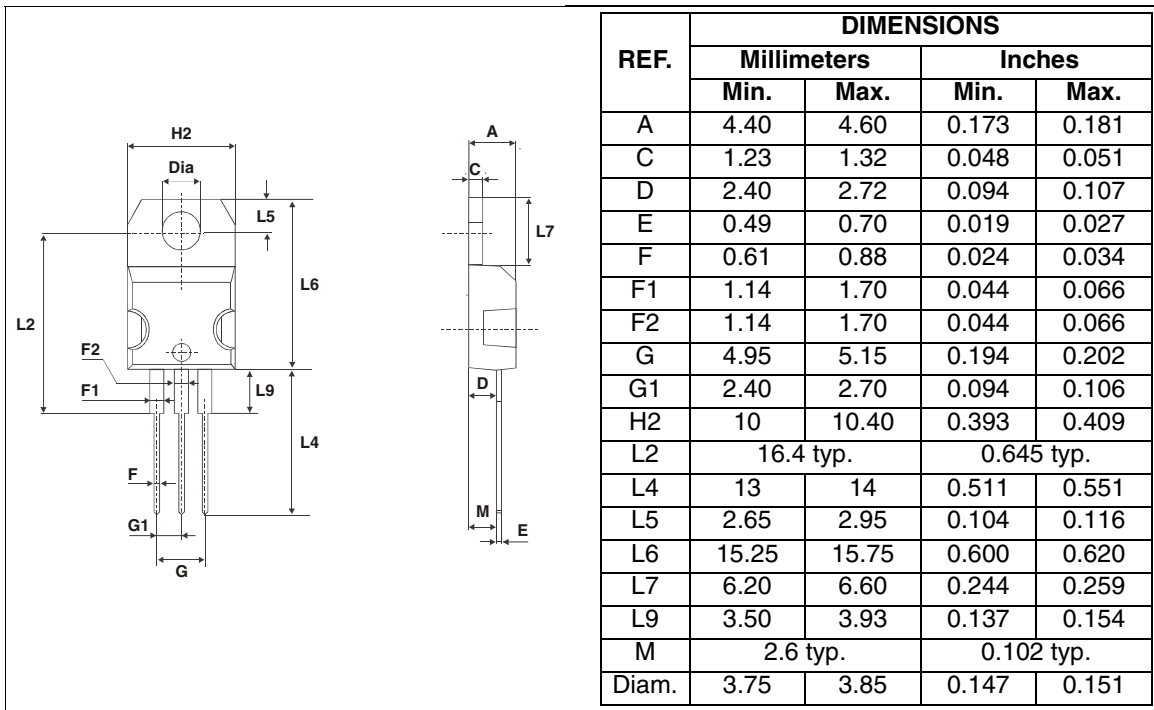
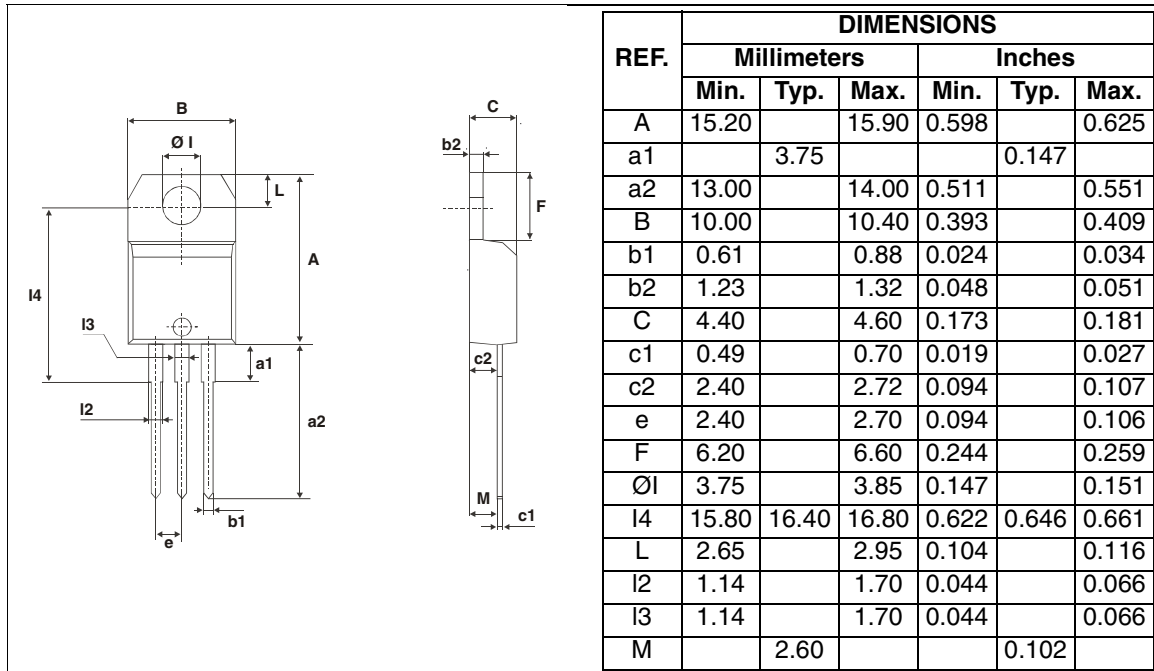


Figure 24: TO-220AB Package Mechanical Data



In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 8: Ordering Information

Ordering type	Marking	Package	Weight	Base qty	Delivery mode
TN805-x00B	TN805x00	DPAK	0.3 g	75	Tube
TN805-x00B-TR	TN805x00	DPAK	0.3 g	2500	Tape & reel
TN805-x00H	TN805x00	IPAK	0.4 g	75	Tube
TN815-x00B	TN815x00	DPAK	0.3 g	75	Tube
TN815-x00B-TR	TN815x00	DPAK	0.3 g	2500	Tape & reel
TN815-x00H	TN815x00	IPAK	0.4 g	75	Tube
TS820-x00B	TS820x00	DPAK	0.3 g	75	Tube
TS820-x00B-TR	TS820x00	DPAK	0.3 g	2500	Tape & reel
TS820-x00H	TS820x00	IPAK	0.4 g	75	Tube
TS820-x00T	TS820x00T	TO-220AB	2.3 g	50	Tube
TYNx08RG	TYNx08	TO-220AB	2.3 g	50	Tube

Note: x = voltage

Table 9: Revision History

Date	Revision	Description of Changes
Apr-2002	4A	Last update.
13-Feb-2006	5	TO-220AB delivery mode changed from bulk to tube. ECOPACK statement added.



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