

### A 0.65V/1µA Nanopower Voltage Detector with Dual Outputs FEATURES DESCRIPTION

- Nanopower Voltage Detector in Single 4 mm<sup>2</sup> Package
- Ultra Low Total Supply Current: 1µA (max)
- ♦ Supply Voltage Operation: 0.65V to 2.5V
- Preset 0.78V UVLO Trip Threshold
- Internal ±10mV Hysteresis
- Resettable Latched Comparator
- Complimentary and Open-drain Comparator Outputs
- Separate Comparator Output Supply Pin

APPLICATIONS

Power-Fail Indicator Low-Battery Detection Battery-Backup Detection CPU, Microprocessor, and Logic Reset Controller Battery-powered Systems The TS12001 voltage detector combines a 0.58V reference and a comparator with resettable comparator latch in a single package. The TS12001 operates from a single 0.65V to 2.5V power supply and consumes less than 1µA total supply current. Optimized for ultra-long life operation, the TS12001 expands Touchstone's growing "NanoWatt Analog<sup>™</sup> high-performance analog integrated circuits portfolio.

The voltage detector exhibits a preset UVLO threshold voltage of 0.78V (typ) or can be set to other threshold voltages with two external resistors. The comparator exhibits  $\pm 10$ mV of internal hysteresis for clean, chatter-free output switching. The TS12001 also offers both push-pull and open-drain outputs. When compared against similar products, the TS12001 offers a factor-of-2 lower power consumption and at least a 33% reduction in pcb area.

The TS12001 is fully specified over the -40°C to +85°C temperature range and is available in a low-profile, 10-pin 2x2mm TDFN package with an exposed back-side paddle.

### **TYPICAL APPLICATION CIRCUIT**



The Touchstone Semiconductor logo and "NanoWatt Analog" are registered trademarks of Touchstone Semiconductor, Incorporated.



### **ABSOLUTE MAXIMUM RATINGS**

Supply Voltage (VIN to VSS)	+2.75V
Supply Voltage (OV <sub>DD</sub> to V <sub>SS</sub> )	+2.75V
Input Voltage	
SET	$V_{SS} - 0.3V$ to V <sub>IN</sub> + 0.3V
LHDET	V <sub>ss</sub> - 0.3V to +5.5V
Output Voltage	
REFOUT	$V_{SS} - 0.3V$ to $V_{IN} + 0.3V$
COUTPP	$V_{SS}$ - 0.3V to $OV_{DD}$ + 0.3V
COUTOD	V <sub>ss</sub> - 0.3V to +5.5V

Output Current	
COUTPP, COUTOD	20mA
Short-Circuit Duration	
(REFOUT, COUTPP, COUTOD)	Continuous
Continuous Power Dissipation ( $T_A = +70^{\circ}C$ )	
10-Pin TDFN (Derate at 13.48mW/°C above -	+70°C) 1078mW
Operating Temperature Range	40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	65°C to +150°C
Lead Temperature (Soldering, 10s)	+300°C

Electrical and thermal stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to any absolute maximum rating conditions for extended periods may affect device reliability and lifetime.

### PACKAGE/ORDERING INFORMATION



Lead-free Program: Touchstone Semiconductor supplies only lead-free packaging.

Consult Touchstone Semiconductor for products specified with wider operating temperature ranges.



## ELECTRICAL CHARACTERISTICS

 $V_{IN} = OV_{DD} = 0.8V$ ;  $V_{SS} = 0V$ ;  $V_{SET} = V_{SS}$ ;  $V_{COUTPP} = HiZ$ ;  $V_{COUTOD} = HiZ$ ;  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ . See note 1.

$\begin{array}{c c c c c c c c c c c c c c c c c c c $	PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Supply Voltage	V <sub>IN</sub>			0.65		2.5	V
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	O mark O mark		DEFOUE	T <sub>A</sub> = +25°C			0.8	
$ \begin{array}{ c c c c c }  UUC O Urput Voltage \\ \hline OV_{00} \\ Voltage \\ \hline Output Driver Supply Current \\ Voltage \\ \hline Output Driver \\ Supply Current \\ \hline Ioop \\ \hline V_{N} rising until COUTPP switches LOW \\ \hline V_{N} rising until COUTPP switches HIGH \\ \hline V_{N} rising until COUTPP switches LOW \\ \hline V_{N} rising until COUTPP switches HIGH \\ \hline V_{N} risi$	Supply Current	I <sub>IN</sub>	REFOUT = open	-40°C ≤ T <sub>A</sub> ≤ 85°C			1	μΑ
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	UVLO Output							
$ \begin{array}{c c c c c c c } \hline \begin{tabular}{ c c c c c c } \hline \begin{tabular}{ c c c c c c c } \hline \begin{tabular}{ c c c c c c c } \hline \begin{tabular}{ c c c c c c c } \hline \begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	Driver Supply	OV <sub>DD</sub>			0.65		2.5	V
$ \begin{array}{ c c c c } \hline \text{Output Driver} \\ \hline \text{Preset UVLO} \\ \hline \text{Preset UVLO} \\ \hline \text{Trip Point} \end{array} & \hline \begin{tabular}{ c c c c } \hline \begin{tabular}{ c c c c c } \hline \begin{tabular}{ c c c c } \hline \begin{tabular}{ c c c c c } \hline \begin{tabular}{ c c c c } \hline \begin{tabular}{ c c c c c c } \hline \begin{tabular}{ c c c c c c c } \hline \begin{tabular}{ c c c c c c c c } \hline \begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	Voltage							
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Output Driver						0.1	uА
$\begin{array}{ c c c c c c } \mbox{Preset UVLO} & V_{N1} tailing until COUTPP switches LOW & 725 7.61 7.97 \\ V_{N1} rising until COUTPP switches HIGH & 743 781 818 818 \\ \hline V_{SET} rising until COUTPP switches HIGH & 74 - 25 °C 540 567 595 \\ \hline -40 °C \leq T_{A} \leq 85 °C 534 & 604 \\ \hline V_{SET} rising until COUTPP switches HIGH & 74 - 25 °C 550 & 620 \\ \hline V_{SET} rising until COUTPP switches HIGH & 74 - 25 °C 550 & 620 \\ \hline V_{SET} rising until COUTPP switches HIGH & 74 - 25 °C 550 & 620 \\ \hline V_{SET} rising until COUTPP switches HIGH & 74 - 25 °C 550 & 620 \\ \hline V_{SET} rising until COUTPP switches HIGH & 74 - 25 °C 550 & 620 \\ \hline V_{SET} rising until COUTPP switches HIGH & 74 - 25 °C 550 & 620 \\ \hline V_{SET} rising until COUTPP switches HIGH & 13 & \mu \\ \hline V_{SET} rising & V_{SET} rising & V_{SET} rising & 0 & 0 & 0 & 0 \\ \hline V_{SET} rising & V_{SET} rising & V_{SET} rising & 0 & 0 & 0 & 0 \\ \hline V_{SET} rising until coutrape switched Output & 10 & 0 & 0 & 0 \\ \hline V_{SET} rising transacture tached Output & 0.78 V \leq V_{N} \leq 1.1 V & 0.1 & 0.1 \\ \hline V_{SET} rising & V_{L} & Comparator Latched Output & 0.78 V \leq V_{N} \leq 1.1 V & 0.2 & 0.2 \\ \hline UHDET Input & V_{H} & Comparator Latched Output & 0.78 V \leq V_{N} \leq 1.1 V & V_{N} - 0.1 & 0 & 0.2 \\ \hline HDET Input & V_{H} & Comparator Latched Output & 0.78 V \leq V_{N} \leq 1.1 V & V_{N} - 0.1 & 0 & 0.2 \\ \hline HDET Input & V_{H} & Comparator Latched Output & 0.78 V \leq V_{N} \leq 1.1 V & V_{N} - 0.1 & 0 & 0.4 \\ \hline HDET Input & V_{H} & Comparator Latched Output & 0.78 V \leq V_{N} \leq 2.5 V & 1 & 0 & 0.2 \\ \hline HDET Input & V_{H} & Comparator Latched Output & 0.78 V \leq V_{N} \leq 5.5 & 5.77 & 600 \\ \hline Output Voltage & V_{REF} & V_{SS}; V_{EHDET} = 5.5 V & 1 & 0 & 0.5 \\ \hline Cutrapt V_{IHDET} = 100 \mu A & V_{IH} & 0.5 & 0.5 & 0.5 & 0.5 \\ \hline Output High Voltage & V_{OL} & COUTPP; I_{OUT} = 100 \mu A & V_{N} - 0.1 & V \\ \hline Output Low V_{OL} & COUTOP; I_{OUT} = 100 \mu A & V_{SS} + 0.1 & V \\ \hline Output Low V_{OL} & COUTOP; I_{OUT} = 100 \mu A & V_{SS} + 0.1 & V \\ \hline Output Low V_{OL} & Sourcing; V_{COUTPP} = V_{SS} & 0.1 & 0.5 & 0.1 & 0 & 0.5 \\ \hline Output Low V_{O$	Supply Current	.000						<b>1</b>
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Preset UVLO		V <sub>IN</sub> falling until COUTPP switches LOW		725	761	/9/	mV
$ \begin{array}{ c c c c c c c } SET Trip Point & V_{SET} falling until COUTPP switches LOW & \frac{1.4 + 25^{\circ}C}{-40^{\circ}C} \leq 5.4^{\circ}d} \leq 567 & 534 & 604 \\ \hline -40^{\circ}C \leq T_A \leq 85^{\circ}C} & 554 & 604 \\ \hline -40^{\circ}C \leq T_A \leq 85^{\circ}C} & 550 & 662 & 620 \\ \hline -40^{\circ}C \leq T_A \leq 85^{\circ}C} & 550 & 662 & 620 & 62$	Trip Point		V <sub>IN</sub> rising until COUTPP switches HIGH	T 0500	743	781	818	
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $			V <sub>SET</sub> falling until COUTPP switches LOW	$I_A = +25^{\circ}C$	540	567	595	
$ \begin{array}{ c c c c c c c c c } \hline V_{\text{SET}} \mbox{ rising until COUTPP switches HIGH } & \hline I_A = +25^{\circ}C & 560 & 587 & 615 \\ \hline I_A = +25^{\circ}C & 550 & 620 \\ \hline V_{\text{SET}} \mbox{ rising } & V_{\text{SET}} \mbox{ rising } & I & I & I \\ \hline V_{\text{SET}} \mbox{ rising } & V_{\text{SET}} \mbox{ rising } & I & I & I \\ \hline V_{\text{SET}} \mbox{ rising } & V_{\text{SET}} \mbox{ rising } & I & I & I \\ \hline Preset UV.0 \\ \mbox{ Trip Hysteresis } & I & I & I \\ \hline Preset UV.0 \\ \mbox{ SET Input } \\ \mbox{ Leakage } & See \mbox{ Note } 2 & 90 & I & mV \\ \hline SET \mbox{ rise rise } V_{\text{SET}} \mbox{ Vser } V_{\text{SET}} \mbox{ Leakage } \mbox{ Comparator Latched Output } \mbox{ D.78V $\le V_{\text{IN} $\le 1.1V$ V \mbox{ N} $< 0.2$ } \mbox{ 0.2 } \mbox{ Vill HDET} \mbox{ risk risk } 1.1V \mbox{ Vill $< 0.78V $\le V_{\text{IN} $\le 1.1V$ V \mbox{ N} $< 0.2$ } \\ V_{\text{IHDET} \mbox{ risk } 1.1V \mbox{ Vill $< 0.78V $\le V_{\text{IN} $\le 1.1V$ V \mbox{ N} $< 0.2$ } \\ V_{\text{IHDET} \mbox{ risk } 1.1V \mbox{ Vill $< 0.78V $\le V_{\text{IN} $\le 1.1V$ V \mbox{ N} $< 0.2$ } \\ V_{\text{IHDET} \mbox{ risk } 1.1V \mbox{ Vill $< 0.78V $\le V_{\text{IN} $\le 1.1V$ V \mbox{ N} $< 0.2$ } \\ V_{\text{IHDET} \mbox{ risk } 1.1V \mbox{ Vill $< 0.78V $\le V_{\text{IN} $\le 2.5V$ } \\ 1 \ V \\mbox{ N} \\ 0.2$ \\ V_{\text{IHDET} \mbox{ risk } 1.1V \mbox{ Vill $< 0.78V $\le V_{\text{IN} $\le 2.5V$ } \\ 1 \\ V_{\text{IH}} \\ 0.2$ \\ Comparator Latched Output \mbox{ Disk } 1.1V  Vill $< 0.5$ \\ 555 \\ 555 \\ 555 \\ 557 \\ 600 \\\ mV \\\ 0.2$ \\ $	SET Trip Point			$-40^{\circ}C \le I_A \le 85^{\circ}C$	534		604	
SET Trip Response TimeVast rising Vast rising13 $\mu$ SPreset UVLO Trip HysteresisVast falling10 $\mu$ SSET Enable ThresholdSee Note 290 $mV$ SET Input LeakageVast = Vss; Vast = V_N90 $mV$ SET Input LeakageVast = Vss; Vast = V_N90 $mV$ SET Input LeakageVast = Vss; Vast = V_N $0.78V \le V_{IN} \le 1.1V$ $0.1$ UnderstandComparator Latched Output Enabled $0.78V \le V_{IN} \le 1.1V$ $0.2$ UHDET Input Low VoltageVILComparator Latched Output Disabled $0.78V \le V_{IN} \le 1.1V$ $0.2$ UHDET Input LeakageVILComparator Latched Output Disabled $0.78V \le V_{IN} \le 1.1V$ $0.2$ UHDET Input LeakageVILComparator Latched Output Disabled $0.78V \le V_{IN} \le 1.1V$ $0.2$ UHDET Input LeakageVILComparator Latched Output Disabled $0.78V \le V_{IN} \le 1.1V$ $V_{IN} \cdot 0.1$ Utput VoltageVIHDisabled $1.1V < V_{IN} \le 2.5V$ $1$ $V$ Utput VoltageVREFVIENDET = $V_{SS}$ ; $V_{EHDET} = 5.5V$ $I$ $100$ $nA$ Reference LoadVREF $V_{REF} = V_{SS}$ ; $V_{EHDET} = 5.5V$ $I$ $100$ $nA$ Output VoltageVoHCOUTPP; Iour = $100\mu$ A $V_{IN} - 0.1$ $V$ $V_{SS} + 0.1$ $V$ Output Low VoltageVoLCOUTPP; Iour = $100\mu$ A $V_{IN} - 0.1$ $V_{SS} + 0.1$ $V$ Output Low VoltageVoLCOUTPP; Iour =	'		V <sub>SET</sub> rising until COUTPP switches HIGH	$I_A = +25^{\circ}C$	560	587	615	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $				$-40^{\circ}C \le I_A \le 85^{\circ}C$	550		620	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	SET Trip		V <sub>SET</sub> rising			13		us
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Response Time		V <sub>SET</sub> falling			10		
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Preset UVLO					±10		mV
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	CET Enchlo							
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	SET Enable		See Note 2		90			mV
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	SET Input				-			
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Leakage		$V_{SET} = V_{SS}; V_{SET} = V_{IN}$				20	nA
Liber Input Low VoltageVILEnabledEnabled1.1V < VIN $\leq 2.5V$ 0.2VLHDET Input High VoltageVIHComparator Latched Output Disabled $0.78V \leq V_{IN} \leq 1.1V$ VIN $\cdot 0.1$ VLHDET Input LeakageVVIHComparator Latched Output Disabled $0.78V \leq V_{IN} \leq 1.1V$ VIN $\cdot 0.1$ VLHDET Input LeakageVVIHVIHVIH $1.1V < V_{IN} \leq 2.5V$ 1VLHDET Input LeakageVVIHVIH $1.1V < V_{IN} \leq 2.5V$ 1VReference Load RegulationVREFVREF $100$ nAnAReference Load RegulationVREF $I_{OUT} = \pm 100nA$ $T_A = \pm 25^{\circ}C$ $555$ $577$ $600$ Output High VoltageVOHCOUTPP; IOUT = $-100\muA$ $V_{IN} - 0.1$ $V_{IN} - 0.1$ $V$ Output Low VoltageVOLCOUTPP; IOUT = $100\muA$ $V_{IN} - 0.1$ $V_{SS} + 0.11$ $V$ Output Low VoltageVOLCOUTOD; IOUT = $100\muA$ $V_{SS} + 0.11$ $V$ $V_{SS} + 0.11$ $V$ Output Short- CircuitIscSourcing; V_{COUTPP} = V_{IN} $0.1$ $0.5$ $mA$ Current,IscSinking; V_{COUTPP} = V_{IN} $0.1$ $1.4$ $mA$	LHDFT Input		Comparator Latched Output	$0.78V \le V_{IN} \le 1.1V$			0.1	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Low Voltage	VIL	Enabled	$1.1V < V_{\rm IN} \le 2.5V$			0.2	V
High VoltageVIHDisabledDisabled1.1V < VIN < 1.1V < VIN <	LHDFT Input		Comparator Latched Output	$0.78V \le V_{\rm IN} \le 1.1V$	VIN -0.1		0.2	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	High Voltage	VIH	Disabled	1.1V < V <sub>IN</sub> ≤ 2.5V	1			V
$\begin{array}{c c c c c c c c c c c c c c c c c c c $								
Reference Output Voltage $V_{REF}$ $T_A = +25^{\circ}C$ 555577600 602mVReference Load Regulation $I_{0UT} = \pm 100$ nA $I_{0UT} = \pm 100$ nA $0.5$ <td>Leakage</td> <td></td> <td><math>V_{\text{LHDET}} = V_{\text{SS}}; V_{\text{LHDET}} = 5.5V</math></td> <td></td> <td></td> <td></td> <td>100</td> <td>nA</td>	Leakage		$V_{\text{LHDET}} = V_{\text{SS}}; V_{\text{LHDET}} = 5.5V$				100	nA
Output Voltage $V_{REF}$ $-40^{\circ}C \le T_A \le 85^{\circ}C$ $552$ $602$ $mV$ Reference Load Regulation $I_{0UT} = \pm 100nA$ $I_{0UT} = \pm 100nA$ $0.5$ $\%$ Output High Voltage $V_{OH}$ COUTPP; $I_{0UT} = -100\muA$ $V_{IN} - 0.1$ $V$ $V$ Output Low Voltage $V_{OL}$ COUTPP; $I_{0UT} = 100\muA$ $V_{IN} - 0.1$ $V$ $V$ Output Low Voltage $V_{OL}$ COUTPP; $I_{0UT} = 100\muA$ $V_{SS} + 0.1$ $V$ Output Low Voltage $V_{OL}$ COUTOD; $I_{0UT} = 100\muA$ $V_{SS} + 0.11$ $V$ Output Short- Circuit Current, $I_{SC}$ Sourcing; $V_{COUTPP} = V_{SS}$ $0.1$ $mA$ Sinking; $V_{COUTPP} = V_{IN}$ $0.5$ $mA$	Reference			T <sub>A</sub> = +25°C	555	577	600	
Reference Load Regulation $I_{OUT} = \pm 100nA$ $I_{OUT} = \pm 100nA$ $0.5$ %Output High Voltage $V_{OH}$ COUTPP; $I_{OUT} = -100\muA$ $V_{IN} - 0.1$ $V$ Output Low Voltage $V_{OL}$ COUTPP; $I_{OUT} = -100\muA$ $V_{IN} - 0.1$ $V$ Output Low Voltage $V_{OL}$ COUTPP; $I_{OUT} = 100\muA$ $V_{SS} + 0.11$ $V$ Output Low Voltage $V_{OL}$ COUTOD; $I_{OUT} = 100\muA$ $V_{SS} + 0.11$ $V$ Output Low Voltage $V_{OL}$ COUTOD; $I_{OUT} = 100\muA$ $0.1$ $mA$ Output Short- Circuit Current, $I_{SC}$ Sinking; $V_{COUTPP} = V_{IN}$ $0.5$ $mA$	Output Voltage	V <sub>REF</sub>		-40°C ≤ T <sub>A</sub> ≤ 85°C	552		602	mv
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Reference							
RegulationImage: Course of the second state of the second st	Load		$I_{OUT} = \pm 100 nA$				0.5	%
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Regulation							
VoltageVoHCOUTPP; Iout = 100 $\mu$ AVIN=0.1VOutput Low VoltageVoLCOUTPP; Iout = 100 $\mu$ AVVss + 0.1VOutput Low VoltageVoLCOUTOD; Iout = 100 $\mu$ AVss + 0.11VOutput Short- Circuit Current,IscSourcing; Vcourpp = Vss0.1mASinking; Vcourpp = VIN0.5mA	Output High	Van			V. 01			V
	Voltage	∨он	$COUTFF, 100T = -100\mu A$		$v_{\rm IN} = 0.1$			v
VoltageVolOCOTINI, Hour = HoupinVisition = HoupinOutput Low VoltageVolCOUTOD; Iout = 100 $\mu$ AVisition = VisitionOutput Short- Circuit Current,Sourcing; V_{COUTPP} = Visition0.1mASinking; V_{COUTPP} = Visition0.5mASinking; V_{COUTOP} = Visition1.4mA	Output Low	Va	COLITEP: $I_{OUT} = 100 \mu \Delta$				$V_{aa} \pm 0.1$	V
	Voltage	VOL					V55 1 0.1	v
Voltage Sourcing; V_{COUTPP} = V_{SS} 0.1 mA   Output Short- Circuit Current, Sinking; V_{COUTPP} = V_{IN} 0.5 mA	Output Low	Voi	COUTOD: Jour = 100µA				$V_{ss} + 0.11$	V
Output Short- CircuitSourcing; $V_{COUTPP} = V_{SS}$ 0.1mASinking; $V_{COUTPP} = V_{IN}$ 0.5mACurrent,Sinking; $V_{COUTOP} = V_{IN}$ 1.4mA	Voltage	• OL					133 . 01.1	· · ·
Circuit Current,IscSinking; $V_{COUTPP} = V_{IN}$ 0.5mASinking: $V_{COUTOP} = V_{IN}$ 1.4mA	Output Short-	l .	Sourcing; V <sub>COUTPP</sub> = V <sub>SS</sub>		0.1			mA
Current,   Sinking; $V_{COUTOD} = V_{IN}$   1.4   mA	Circuit	I <sub>SC</sub>	Sinking; $V_{COUTPP} = V_{IN}$		0.5			mA
	Current,		Sinking; $V_{COUTOD} = V_{IN}$			1.4		mA
Lookago COUTOD; V <sub>COUTOD</sub> = 5V 20 nA	Open Drain		COUTOD; V <sub>COUTOD</sub> = 5V				20	nA

**Note 1:** All devices are 100% production tested at  $T_A = +25^{\circ}C$  and are guaranteed by characterization for  $T_A = T_{MIN}$  to  $T_{MAX}$ , as specified. **Note 2:** A SET voltage above this threshold voltage enables the SET pin voltage to control the comparator output.



### **PIN FUNCTIONS**

PIN	NAME	FUNCTION	
1	VIN	Positive Supply Voltage. Connect a 0.1µF bypass capacitor from this pip to apply V(SS/CND	
2	SET	External UVLO Trip Threshold Set Pin. When this pin is set to VSS, the internal preset 0.78V UVLO trip threshold controls the comparator output. When the applied voltage to this pin is higher than 90mV, the SET pin sets the trip threshold and controls the comparator output. If the SET pin is not used, connect the pin to to VSS.	
3	NC	No Connection	
4	VSS	Negative Supply Voltage.	
5	LHDET	Latch Enable Pin. When LHDET is set HIGH, the outputs of the comparator will toggle normally based on the inputs to the comparator. When LHDET is set LOW and COUTPP is HIGH, COUTPP will remain HIGH despite any changes to the input of the comparator. COUTPP will once again respond to changes to the input when LHDET is toggled HIGH. If COUTPP is initially LOW and the LHDET is then LOW, COUTPP will stay LOW. If a LOW-to-HIGH transition occurs on COUTPP, COUTPP will switch to HIGH and stay HIGH and not respond to any changes at the input. The LHDET pin must always be set to a known state. For unlatched comparator operation, set LHDET to HIGH. The open-drain output (COUTOD) is the inverted version of the COUTPP output.	
6	REFOUT	0.58V Reference Output	
7	NC	No Connection	
8	COUTOD	Comparator Open-Drain Output	
9	COUTPP	Comparator Push-Pull Output	
10	OVDD	Output Driver Positive Supply Voltage. Connect a 0.1µF bypass capacitor from this pin to analog VSS/GND.	
EP		Exposed paddle is electrically connected to VSS/GND.	





#### THEORY OF OPERATION

The TS12001 combines a  $0.58V \pm 4.5\%$  reference and an analog comparator with a resettable comparator latch in a single package. The TS12001 operates from a single 0.65V to 2.5V power supply and consumes less than 1µA total supply current. The TS12001 comparator has a push-pull and opendrain output driver. The push-pull output driver is powered from a separate supply voltage,  $OV_{DD}$ . The open-drain output stage allows for easy output voltage level translation as may be required when driving systems powered with a different power supply rail. The analog comparator exhibits  $\pm 10mV$  of internal hysteresis for clean, chatter-free output switching. The internal reference was designed to sink or source up to  $0.1\muA$  load currents.

The TS12001 has a preset UVLO threshold voltage of 0.78V (typ) or can be set to other threshold voltages with two external resistors where the divided

voltage is applied to the SET pin. When the SET pin voltage is grounded or it is less than approximately 90mV, the internal preset UVLO threshold circuit will control the comparator outputs. If the SET pin is above approximately 90mV, the external voltage divider circuit will control the comparator outputs. The 0.58V reference voltage is tied to the inverting input of the comparator and the output of a switch is connected to the non-inverting input of the comparator. The output of the switch is either the SET voltage or the internal UVLO threshold voltage, depending on whether the SET pin voltage is above or below approximately 90mV. If the switch output is above 0.58V, the push-pull output (COUTPP) will be HIGH and the open-drain output (COUTOD) will be LOW and vice versa. For proper operation, the supply voltage V<sub>IN</sub> must be applied before the output driver supply voltage  $(OV_{DD})$  is applied.

The TS12001 has a latch enable pin (LHDET) that

TS12001DS r1p0

# TS12001

allows the output of the comparator to latch to a HIGH state under certain conditions. If LHDET is set HIGH, the COUTPP output will switch based on the input to the comparator. When LHDET is set LOW and COUTPP is HIGH, COUTPP will remain HIGH until LHDET goes LOW. When COUTPP is initially LOW instead, COUTPP will latch HIGH until a LOW-to-HIGH transition occurs on the COUTPP output. In essence, the LHDET pin offers a LOW-to-HIGH detection. However, LHDET must not be left open. The open-drain output, COUTOD, is the inverter version of the COUTPP output. Connect LHDET to  $V_{IN}$  for normal operation or to  $V_{SS}$  for LHDET enable.

If the SET pin is not used, it cannot be left unconnected and should be tied to  $V_{\mbox{\scriptsize SS}}.$ 

#### Comparator

The TS12001 has an internal comparator that can eliminate supply glitches that commonly occur when output transitions occur. In addition, the input exhibits  $\pm 10$ mV of internal hysteresis in order to insure clean output switching behavior. The outputs can swing to

#### **APPLICATIONS INFORMATION**

#### External Voltage Detector Design

Depending on the battery voltage used and the voltage one wishes to detect, the TS12001 can be designed accordingly. As shown in Figure 1, R1 and R2 can be selected based on the desired voltage to detect. Table 1. provides R1 and R2 resistor combinations for detecting various  $V_{\rm IN}$  voltages.

V <sub>IN</sub> Threshold Voltage(V)	R1(MΩ)	R2(MΩ)	
0.9	2.2	4.02	
1.07	3.32	4.02	
1.28	4.75	4.02	
1.52	6.49	4.02	
1.85	8.66	4.02	

Table 1. Resistor Combinations for Several  $V_{\mbox{\scriptsize IN}}$  Threshold Voltages

The design equation for this circuit is shown below. The SET pin voltage ( $V_{SET}$ ) that will cause a HIGH-to-LOW transition on the output is approximately 580mV. To design the circuit, R1 or R2 can be selected along with the desired battery voltage to detect.

Page 6



within 100mV of the supply rails. The COUTPP output can source and sink 0.1mA and 0.5mA of current. The COUTD outputs can sink 1.4mA of current with  $V_{COUTOD} = 0.78V$ 

#### Internal Reference

The TS12001's on-board 0.58V  $\pm$ 4.5% reference voltage can source and sink 0.1µA and 0.1µA of current and can drive a capacitive load less than 50pF and greater than 50nF with a maximum capacitive load of 250nF. The higher the capacitive load, the lower the noise on the reference voltage and the longer the time needed for the reference voltage to respond and become available on the REFOUT pin. With a 250nF capacitive load, the response time is approximately 20ms. While also available as a separate pin as REFOUT, the reference is tied internally to the inverting input of the comparator.

Then, the second resistor value can be evaluated using the voltage divider equation below.

$$R1=\frac{V_{IN} \times R2 - V_{SET} \times R2}{V_{SET}}$$

#### A Nanopower 1.8V Core System Voltage Detector

When power supply rails sag in any system, it is important to alert the CPU. A CPU can be used to detect when I/O or core system voltages sag below a prescribed threshold as shown Figure 2. In this circuit, a 1.8V core system voltage detector is designed around the TS12001 providing a low battery detect signal. R1 and R2 were selected to set a SET voltage at 582mV so that when VCORE drops below 1.77V, the TS12001 output transitions to LOW. It is recommended to use 1% resistors for optimal accuracy. The circuit consumes approximately 0.75 $\mu$ A of current when VCORE = 1.8V.

#### PC Board Layout and Power-Supply Bypassing

While power-supply bypass capacitors are not typically required, it is good engineering practice to use 0.1uF bypass capacitors close to the device's power supply pins. When the power supply impedance is high, the power supply leads are long, or there is excessive noise on the power supply traces. To reduce stray capacitance, it is also good



engineering practice to make signal trace lengths as short as possible. Also recommended are a ground plane and surface mount resistors and capacitors.

#### **Input Noise**

Radiated noise is common in low power circuits that require high impedance circuits. To minimize this effect, all traces between any of the inputs and passive component networks should be made as short as possible.



Figure 1. External Voltage Detector Design Circuit



Figure 2. A Nanopower 1.8V Core System Voltage Detector Circuit



### PACKAGE OUTLINE DRAWING

#### 10-Pin TDFN22 Package Outline Drawing

(N.B., Drawings are not to scale)



Information furnished by Touchstone Semiconductor is believed to be accurate and reliable. However, Touchstone Semiconductor does not assume any responsibility for its use nor for any infringements of patents or other rights of third parties that may result from its use, and all information provided by Touchstone Semiconductor and its suppliers is provided on an AS IS basis, WITHOUT WARRANTY OF ANY KIND. Touchstone Semiconductor reserves the right to change product specifications and product descriptions at any time without any advance notice. No license is granted by implication or otherwise under any patent or patent rights of Touchstone Semiconductor. Touchstone Semiconductor assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications, customers should provide adequate design and operating safeguards. Trademarks and registered trademarks are the property of their respective owners.

Touchstone Semiconductor, Inc. 630 Alder Drive, Milpitas, CA 95035 +1 (408) 215 - 1220 • www.touchstonesemi.com