Fractional-N Frequency Synthesizer

ADF4154

FEATURES

RF bandwidth 500 MHz to 4 GHz
2.7 V to 3.3 V power supply
Separate V_P allows extended tuning voltage
Programmable dual-modulus prescaler 4/5, 8/9
Programmable charge pump currents
3-wire serial interface
Digital lock detect
Power-down mode
Pin compatible with the ADF4110/ADF4111/ ADF4112/ADF4113, ADF4106 and ADF4153
Programmable modulus on fractional-N synthesizer
Trade-off noise versus spurious performance
Fast-lock mode with built-in timer

APPLICATIONS

CATV equipment
Base stations for mobile radio (GSM, PCS, DCS, CDMA, WCDMA)
Wireless handsets (GSM, PCS, DCS, CDMA, WCDMA)
Wireless LANs
Communications test equipment

GENERAL DESCRIPTION

The ADF4154 is a fractional-N frequency synthesizer that implements local oscillators in the up conversion and down conversion sections of wireless receivers and transmitters. It consists of a low noise digital phase frequency detector (PFD), a precision charge pump, and a programmable reference divider. There is a Σ-Δ based fractional interpolator to allow programmable fractional-N division. The INT, FRAC, and MOD registers define an overall N divider (N = (INT + (FRAC/MOD))). In addition, the 4-bit reference counter (R counter) allows selectable REF_{IN} frequencies at the PFD input. A complete phase-locked loop (PLL) can be implemented if the synthesizer is used with an external loop filter and a voltage controlled oscillator (VCO).

A key feature of the ADF4154 is the fast-lock mode with a built-in timer. The user can program a predetermined count-down time value so that the PLL will remain in wide bandwidth mode, instead of having to control this time externally.

Control of all on-chip registers is via a simple 3-wire interface. The device operates with a power supply ranging from 2.7 V to 3.3 V, and can be powered down when not in use.

FUNCTIONAL BLOCK DIAGRAM

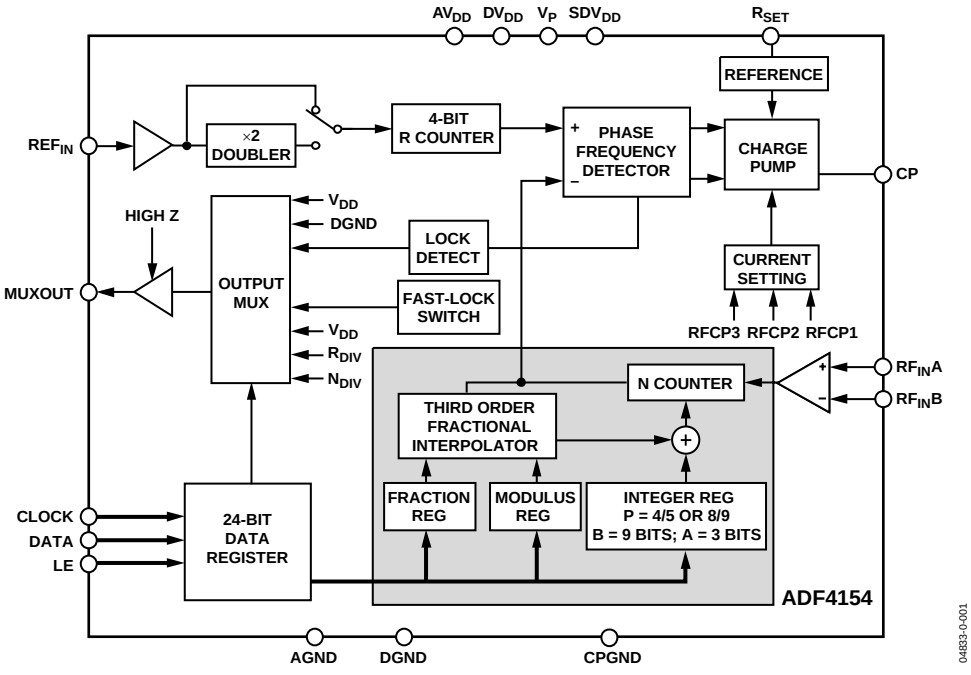

Figure 1.

Rev. 0

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SPECIFICATIONS

Table 1. AV_{DD} = DV_{DD} = SDV_{DD} = 2.7 V to 3.3 V; V_P = AV_{DD} to 5.5 V; AGND = DGND = 0 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted; dBm referred to 50 Ω. The operating temperature for the B version is −40°C to +80°C.

Parameter	B Version	Unit	Test Conditions/Comments
RF CHARACTERISTICS (3 V)			See Figure 18 for input circuit.
RF Input Frequency (RF_{IN})[1]	0.5/4.0	GHz min/max	−8 dBm/0 dBm min/max. For lower frequencies, ensure slew rate > 396 V/µs.
	1.0/4.0	GHz min/max	−10 dBm/0 dBm min/max.
REFERENCE CHARACTERISTICS			See Figure 17 for input circuit.
REF_{IN} Input Frequency[1]	10/250	MHz min/max	For f < 10 MHz, use a dc-coupled, CMOS compatible square wave, slew rate > 21 V/µs.
REF_{IN} Input Sensitivity	0.7/AV_{DD}	V p-p min/max	AC-coupled.
	0 to AV_{DD}	V max	CMOS compatible.
REF_{IN} Input Capacitance	10	pF max	
REF_{IN} Input Current	±100	µA max	
PHASE DETECTOR			
Phase Detector Frequency[2]	32	MHz max	
CHARGE PUMP			
I_{CP} Sink/Source			Programmable. See Table 5.
High Value	5	mA typ	With R_{SET} = 5.1 kΩ.
Low Value	312.5	µA typ	
Absolute Accuracy	2.5	% typ	With R_{SET} = 5.1 kΩ.
R_{SET} Range	1.5/10	kΩ min/max	
I_{CP} Three-State Leakage Current	1	nA typ	Sink and source current.
Matching	2	% typ	0.5 V < V_{CP} < V_P − 0.5.
I_{CP} vs. V_{CP}	2	% typ	0.5 V < V_{CP} < V_P − 0.5.
I_{CP} vs. Temperature	2	% typ	V_{CP} = V_P/2.
LOGIC INPUTS			
V_{INH}, Input High Voltage	1.4	V min	
V_{INL}, Input Low Voltage	0.6	V max	
I_{INH}/I_{INL}, Input Current	±1	µA max	
C_{IN}, Input Capacitance	10	pF max	
LOGIC OUTPUTS			
V_{OH}, Output High Voltage	1.4	V min	Open-drain 1 kΩ pull-up to 1.8 V.
V_{OL}, Output Low Voltage	0.4	V max	I_{OL} = 500 µA.
POWER SUPPLIES			
AV_{DD}	2.7/3.3	V min/V max	
DV_{DD}, SDV_{DD}	AV_{DD}		
V_P	AV_{DD}/5.5	V min/V max	
I_{DD}[3]	24	mA max	20 mA typical.
Low Power Sleep Mode	1	µA typ	
NOISE CHARACTERISTICS			
Phase Noise Figure of Merit[4]	−213	dBc/Hz typ	
ADF4154 Phase Noise Floor[5]	−143	dBc/Hz typ	@ 10 MHz PFD frequency.
	−139	dBc/Hz typ	@ 26 MHz PFD frequency.
Phase Noise Performance[6]			@ VCO output.
1750 MHz Output[7]	−102	dBc/Hz typ	@ 1 kHz offset, 26 MHz PFD frequency.

[1] Use a square wave for frequencies below f_{MIN}.
[2] Guaranteed by design. Sample tested to ensure compliance.
[3] AC coupling ensures AV_{DD}/2 bias. See Figure 17 for typical circuit.
[4] This figure can be used to calculate phase noise for any application. Use the formula −213 + 10log(f_{PFD}) + 20logN to calculate in-band phase noise performance, as seen at the VCO output. The value given is the lowest noise mode.
[5] The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20logN (where N is the N-divider value). The value given is the lowest noise mode.
[6] The phase noise is measured with the EVAL-ADF4154EB1 evaluation board and the HP8562E spectrum analyzer.
[7] f_{REFIN} = 26 MHz; f_{PFD} = 26 MHz; offset frequency = 1 kHz; RF_{OUT} = 1750 MHz; loop B/W = 20 kHz; lowest noise mode.

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TIMING CHARACTERISTICS

Table 2. AV_{DD} = DV_{DD} = SDV_{DD} = 2.7 V to 3.3 V; V_P = AV_{DD} to 5.5 V; AGND = DGND = 0 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted; dBm referred to 50 Ω.

Parameter[1]	Limit at T_{MIN} to T_{MAX} (B Version)	Unit	Test Conditions/Comments
t_1	20	ns min	LE Setup Time
t_2	10	ns min	DATA to CLOCK Setup Time
t_3	10	ns min	DATA to CLOCK Hold Time
t_4	25	ns min	CLOCK High Duration
t_5	25	ns min	CLOCK Low Duration
t_6	10	ns min	CLOCK to LE Setup Time
t_7	20	ns min	LE Pulse Width

[1] Guaranteed by design, but not production tested.

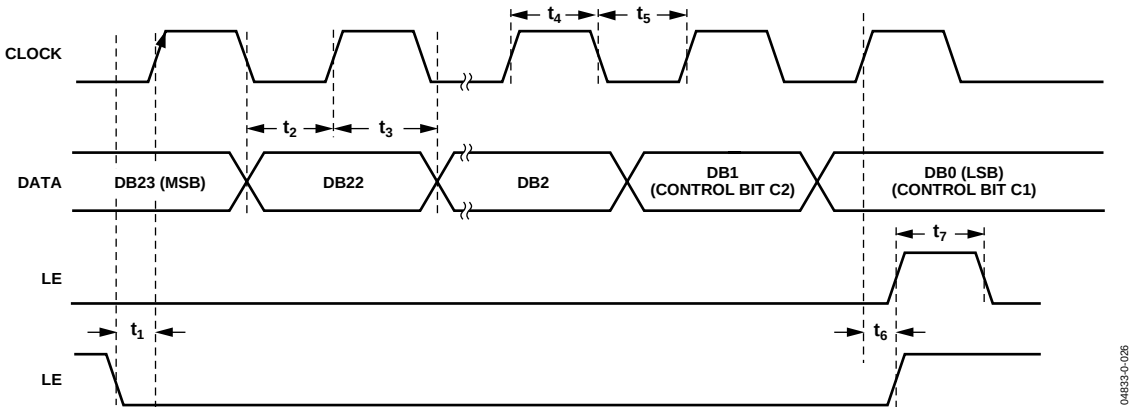

Figure 2. Timing Diagram

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ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute Maximum Ratings.[1, 2, 3] T_A = 25°C, unless otherwise noted.

Parameter	Rating
V_{DD} to GND	−0.3 V to +4 V
V_{DD} to V_{DD}	−0.3 V to +0.3 V
V_P to GND	−0.3 V to +5.8 V
V_P to V_{DD}	−0.3 V to +5.8 V
Digital I/O Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Analog I/O Voltage to GND	−0.3 V to V_{DD} + 0.3 V
REF_{IN}, RF_{IN} to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
TSSOP θ_{JA} Thermal Impedance	150.4°C/W
LFCSP θ_{JA} Thermal Impedance (Paddle Soldered)	122°C/W
LFCSP θ_{JA} Thermal Impedance (Paddle Not Soldered)	216°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[1] This device is a high performance RF integrated circuit with an ESD rating of < 2 kV, and it is ESD sensitive. Proper precautions should be taken for handling and assembly.
[2] GND = A_{GND} = D_{GND} = 0 V.
[3] V_{DD} = AV_{DD} = DV_{DD} = SDV_{DD}.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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PIN CONFIGURATION AND PIN FUNCTION DESCRIPTIONS

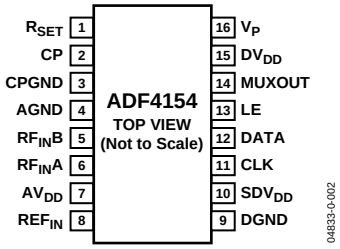

Figure 3. TSSOP Pin Configuration

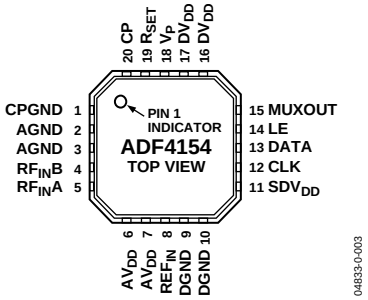

Figure 4. LFCSP Pin Configuration

Table 4. Pin Function Descriptions

TSSOP	LFCSP	Mnemonic	Description
1	19	R_{SET}	Connecting a resistor between this pin and ground sets the maximum charge pump output current. The relationship between I_{CP} and R_{SET} is $$I_{CP\max} = \frac{25.5}{R_{SET}}$$ where R_{SET} = 5.1 kΩ and I_{CPmax} = 5 mA.
2	20	CP	Charge Pump Output. When enabled, this provides ±I_{CP} to the external loop filter, which in turn drives the external VCO.
3	1	CPGND	Charge Pump Ground. This is the ground return path for the charge pump.
4	2, 3	AGND	Analog Ground. This is the ground return path of the prescaler.
5	4	$RF_{IN}B$	Complementary Input to the RF Prescaler. This point should be decoupled to the ground plane with a small bypass capacitor, typically 100 pF (see Figure 18).
6	5	$RF_{IN}A$	Input to the RF Prescaler. This small-signal input is normally ac-coupled from the VCO.
7	6, 7	AV_{DD}	Positive Power Supply for the RF Section. Decoupling capacitors to the digital ground plane should be placed as close as possible to this pin. AV_{DD} has a value of 3 V ± 10%. AV_{DD} must have the same voltage as DV_{DD}.
8	8	REF_{IN}	Reference Input. This is a CMOS input with a nominal threshold of $V_{DD}/2$ and an equivalent input resistance of 100 kΩ (see Figure 17). This input can be driven from a TTL or CMOS crystal oscillator, or it can be ac-coupled.
9	9, 10	DGND	Digital Ground.
10	11	SDV_{DD}	Σ-Δ Power. Decoupling capacitors to the digital ground plane should be placed as close as possible to this pin. SDV_{DD} has a value of 3 V ± 10%. SDV_{DD} must have the same voltage as DV_{DD}.
11	12	CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the shift register on the CLK rising edge. This input is a high impedance CMOS input.
12	13	DATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs as the control bits. This input is a high impedance CMOS input.
13	14	LE	Load Enable, CMOS Input. When LE is high, the data stored in the shift registers is loaded into one of the four latches, the latch being selected using the control bits.
14	15	MUXOUT	This multiplexer output allows either the RF lock detect, the scaled RF, or the scaled reference frequency to be accessed externally.
15	16, 17	DV_{DD}	Positive Power Supply for the Digital Section. Decoupling capacitors to the digital ground plane should be placed as close as possible to this pin. DV_{DD} has a value of 3 V ± 10%. DV_{DD} must have the same voltage as AV_{DD}.
16	18	V_P	Charge Pump Power Supply. This should be greater than or equal to V_{DD}. In systems where V_{DD} is 3 V, it can be set to 5.5 V and used to drive a VCO with a tuning range of up to 5.5 V.

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TYPICAL PERFORMANCE CHARACTERISTICS

Figure 5 to Figure 10, and Figure 12: RF_{OUT} = 1.722 GHz, PFD Frequency = 26 MHz, INT = 66, Channel Spacing = 200 kHz, Modulus = 130, Fraction = 30/130, and I_{CP} = 5 mA.

Loop Bandwidth = 20 kHz, Reference = 26 MHz, VCO = Vari-L VCO190-1750T, Evaluation Board = EVAL-ADF4154EB1. Measurements were taken on the HP8562E spectrum analyzer.

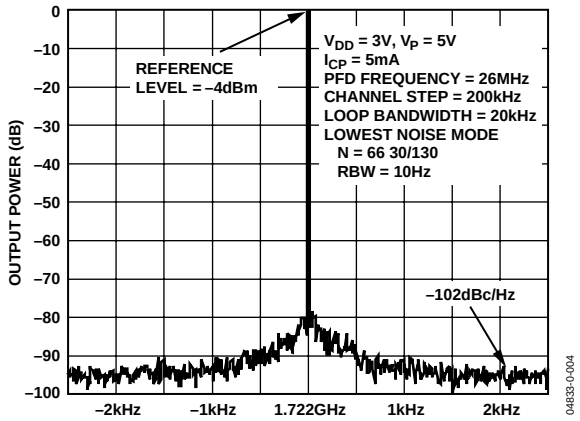

Figure 5. Phase Noise (Lowest Noise Mode)

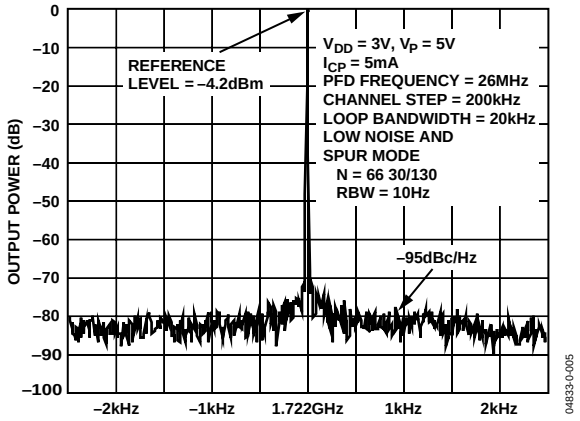

Figure 6. Phase Noise (Low Noise Mode and Spur Mode)

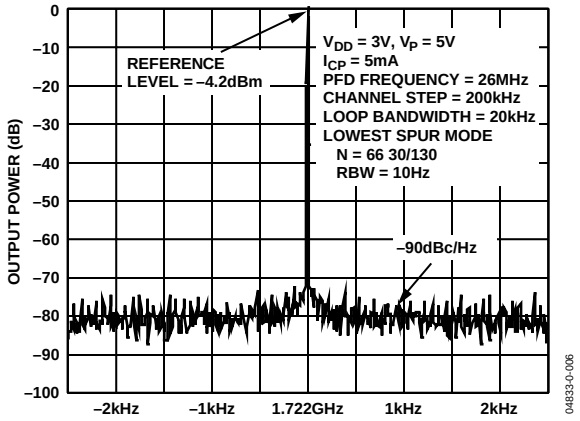

Figure 7. Phase Noise (Lowest Spur Mode)

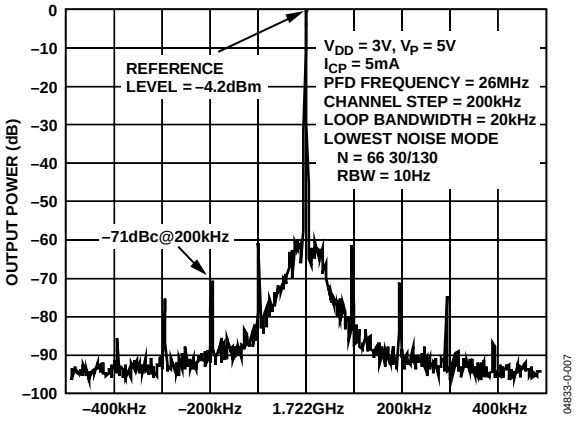

Figure 8. Spurs (Lowest Noise Mode)

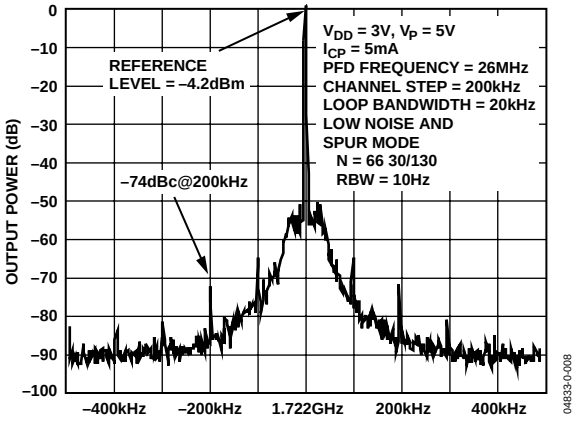

Figure 9. Spurs (Low Noise and Spur Mode)

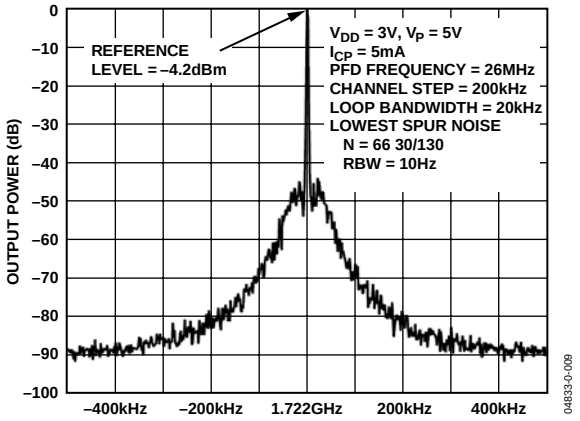

Figure 10. Spurs (Lowest Spur Mode)

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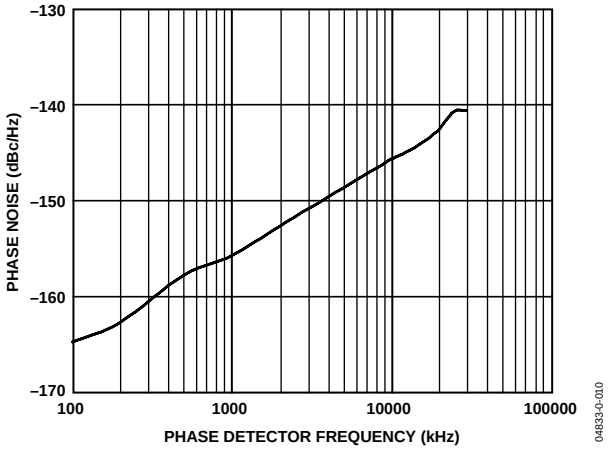

Figure 11. PFD Noise Floor vs. PFD Frequency (Lowest Noise Mode)

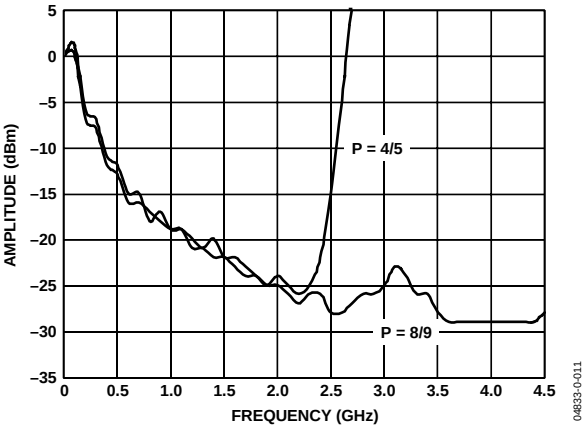

Figure 12. RF Input Sensitivity

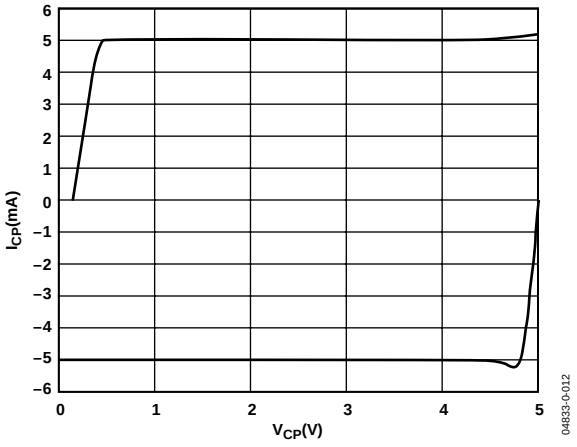

Figure 13. Charge Pump Output Characteristics

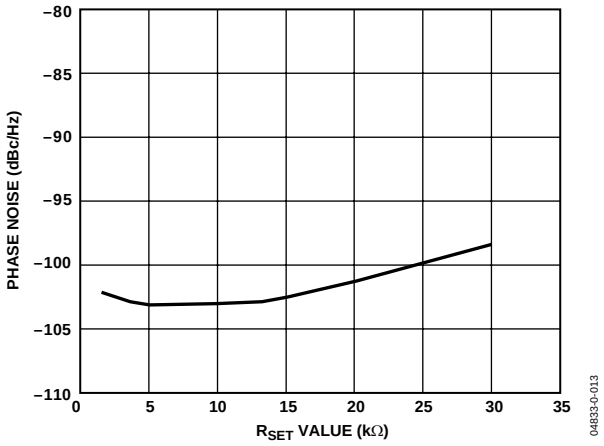

Figure 14. Phase Noise vs. R_{SET}

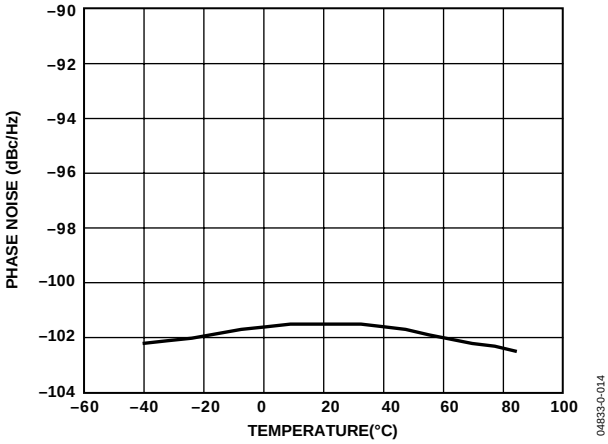

Figure 15. Phase Noise vs. Temperature

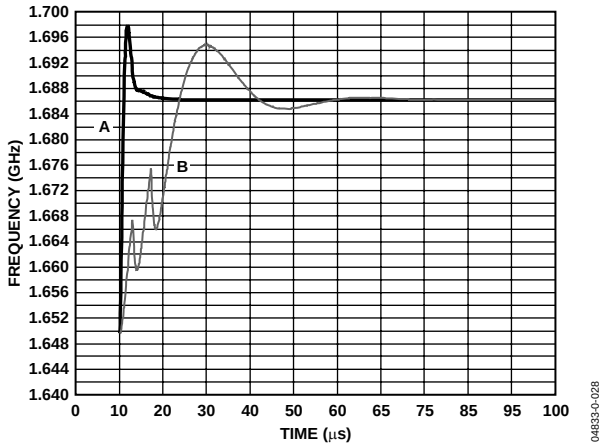

Figure 16. A) Lock Time in Fast-lock Mode. Fast Counter = 150, Low Spur Mode: a 1649.7 MHz to 1686.8 MHz Frequency Jump. Final Loop Bandwidth = 60 kHz
B) Lock Time with the PLL in Normal Mode (Non Fast-lock), Low Spur Mode, a 1649.7 MHz to 1686.8 MHz Frequency Jump. Final Loop Bandwidth = 60 kHz

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CIRCUIT DESCRIPTION

REFERENCE INPUT SECTION

The reference input stage is shown in Figure 17. SW1 and SW2 are normally closed switches. SW3 is normally open. When power-down is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that the REF_{IN} pin is not loaded on power-down.

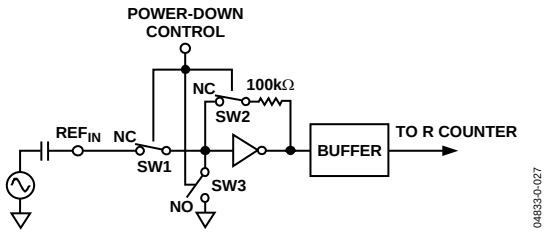

Figure 17. Reference Input Stage

RF INPUT STAGE

The RF input stage is shown in Figure 18. It is followed by a 2-stage limiting amplifier to generate the current mode logic (CML) clock levels needed for the prescaler.

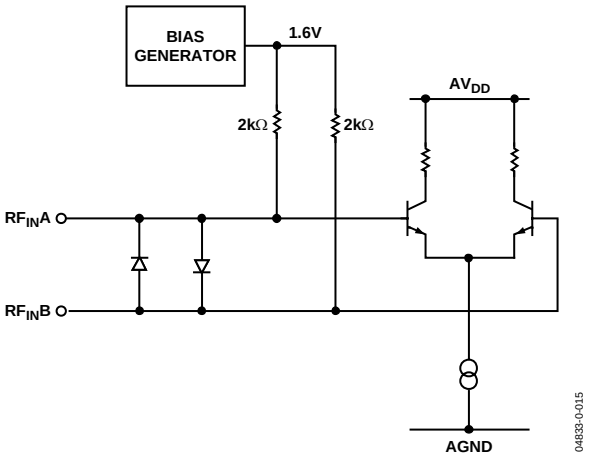

Figure 18. RF Input Stage

RF INT DIVIDER

The RF INT CMOS counter allows a division ratio in the PLL feedback counter. Division ratios from 31 to 511 are allowed.

INT, FRAC, MOD, AND R RELATIONSHIP

The INT, FRAC, and MOD values, in conjunction with the R counter, make it possible to generate output frequencies that are spaced by fractions of the phase frequency detector (PFD). See the RF Synthesizer: A Worked Example section for more information. The RF VCO frequency (RF_{OUT}) equation is

$$RF_{OUT} = F_{PFD} \times (INT + (FRAC/MOD)) \quad (1)$$

where RF_{OUT} is the output frequency of the external voltage controlled oscillator (VCO).

$$F_{PFD} = REF_{IN} \times (1 + D)/R \quad (2)$$

where:

REF_{IN} is the reference input frequency.
D is the REF_{IN} doubler bit.
R is the preset divide ratio of binary 4-bit programmable reference counter (1 to 15).
INT is the preset divide ratio of binary 9-bit counter (31 to 511).
MOD is the preset modulus ratio of binary 12-bit programmable FRAC counter (2 to 4095).
$FRAC$ is the preset fractional ratio of binary 12-bit programmable FRAC counter (0 to MOD).

RF R COUNTER

The 4-bit RF R counter allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the PFD. Division ratios from 1 to 15 are allowed.

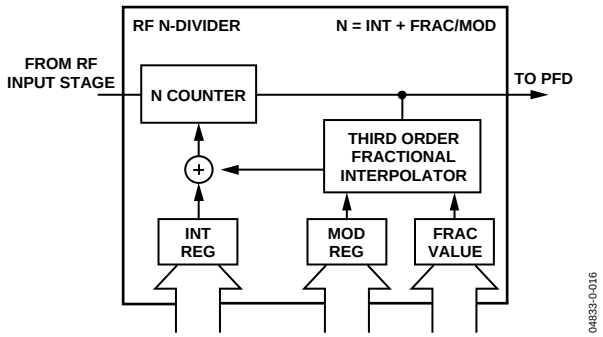

Figure 19. A and B Counters

PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter and produces an output proportional to the phase and frequency difference between them. Figure 20 is a simplified schematic. The PFD includes a fixed delay element that sets the width of the antibacklash pulse, which is typically 3 ns. This pulse ensures that there is no dead zone in the PFD transfer function and gives a consistent reference spur level.

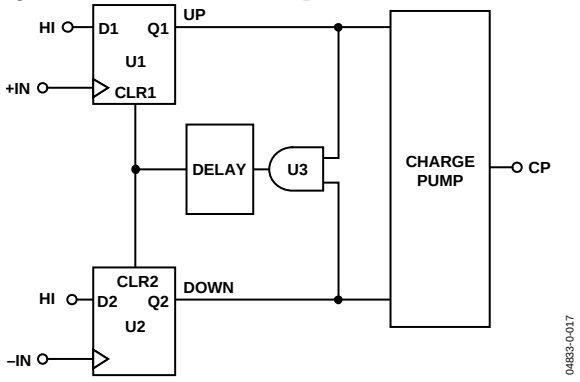

Figure 20. PFD Simplified Schematic

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MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4154 allows the user to access various internal points on the chip. The state of MUXOUT is controlled by M3, M2, and M1 (see Table 9). Figure 21 shows the MUXOUT section in block diagram form.

The N-channel, open-drain, analog lock detect should be operated with an external pull-up resistor of 10 kΩ nominal. When lock has been detected, the lock detect is high with narrow low-going pulses.

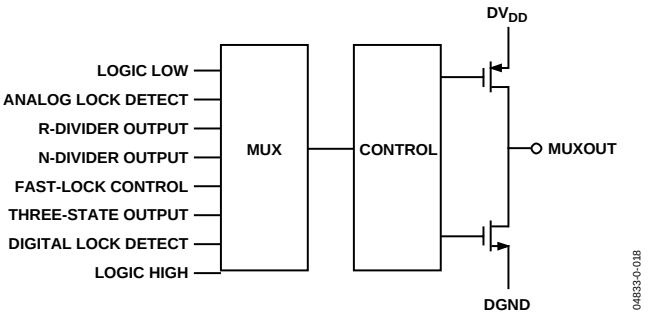

Figure 21. MUXOUT Schematic

INPUT SHIFT REGISTERS

The ADF4154 digital section includes a 4-bit RF R counter, a 9-bit RF N counter, a 12-bit FRAC counter, and a 12-bit modulus counter. Data is clocked into the 24-bit shift register on each rising edge of CLK. The data is clocked in MSB first.

Data is transferred from the shift register to one of four latches on the rising edge of LE. The destination latch is determined by the state of the two control bits (C2 and C1) in the shift register. These are the 2 LSBs, DB1, and DB0, as shown in Figure 2. The truth table for these bits is shown in Table 5. Table 6 shows a summary of how the latches are programmed.

PROGRAM MODES

Table 5 through Table 10 show how to set up the program modes in the ADF4154.

The ADF4154 programmable modulus is double-buffered. This means that two events have to occur before the part uses a new modulus value. First, the new modulus value is latched into the device by writing to the R-divider register. Second, a new write must be performed on the N-divider register. Therefore, whenever the modulus value is updated, the N-divider register must then be written to so that the modulus value is loaded correctly.

Table 5. C2 and C1 Truth Table

Control Bits		
C2	**C1**	**Data Latch**
0	0	N-divider register
0	1	R-divider register
1	0	Control register
1	1	Noise and spur register

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REGISTERS

Table 6. Register Summary

N-DIVIDER REG

FAST-LOCK	9-BIT RF INTEGER VALUE									12-BIT RF FRACTIONAL VALUE												CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
FL1	N9	N8	N7	N6	N5	N4	N3	N2	N1	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	C2 (0)	C1 (0)

R-DIVIDER REG

LOAD CONTROL	MUXOUT			RESERVED	PRESCALER	4-BIT R COUNTER				12-BIT MODULUS												CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P3	M3	M2	M1	P2	P1	R4	R3	R2	R1	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	C2 (0)	C1 (1)

CONTROL REG

RESERVED				REFERENCE DOUBLER	CP/2	CP CURRENT SETTING			PD POLARITY	LDP	POWER-DOWN	CP THREE-STATE	COUNTER RESET	CONTROL BITS	
DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	U6	CP3	CP2	CP1	CP0	U5	U4	U3	U2	U1	C2 (1)	C1 (0)

NOISE AND SPUR REG

RESERVED	NOISE AND SPUR MODE				RESERVED			NOISE AND SPUR MODE	CONTROL BITS	
DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
T9	T8	T7	T6	T5	T4	T3	T2	T1	C2 (1)	C1 (1)

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Table 7. Noise and Spur Register

RESERVED	NOISE AND SPUR MODE				RESERVED			NOISE AND SPUR MODE	CONTROL BITS	
DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
T9	T8	T7	T6	T5	T4	T3	T2	T1	C2 (1)	C1 (1)

DB10, DB5, DB4, DB3	RESERVED
0	RESERVED
THESE BITS MUST BE SET TO 0 FOR NORMAL OPERATION.	

DB9, DB8, DB7, DB6, DB2	NOISE AND SPUR SETTING
00000	LOWEST SPUR MODE
11100	LOW NOISE AND SPUR MODE
11111	LOWEST NOISE MODE

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Table 8. N-Divider Register Map

FAST-LOCK	9-BIT INTEGER VALUE (INT)									12-BIT FRACTIONAL VALUE (FRAC)												CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
FL1	N9	N8	N7	N6	N5	N4	N3	N2	N1	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	C2 (0)	C1 (0)

F12	F11	F10		F3	F2	F1	FRACTIONAL VALUE (FRAC)
0	0	0	.....	0	0	0	0
0	0	0	.....	0	0	1	1
0	0	0	.....	0	1	0	2
0	0	0	.....	0	1	1	3
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	4092
1	1	1	.....	1	0	1	4093
1	1	1	.....	1	1	0	4094
1	1	1	.....	1	1	1	4095

N9	N8	N7	N6	N5	N4	N3	N2	N1	INTEGER VALUE (INT)
0	0	0	0	1	1	1	1	1	31
0	0	0	1	0	0	0	0	0	32
0	0	0	1	0	0	0	0	1	33
0	0	0	1	0	0	0	1	0	34
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	...	.	.	.	.
1	1	1	1	1	1	1	0	1	509
1	1	1	1	1	1	1	1	0	510
1	1	1	1	1	1	1	1	1	511

FL1	FAST-LOCK
0	NORMAL OPERATION
1	FAST-LOCK ENABLED

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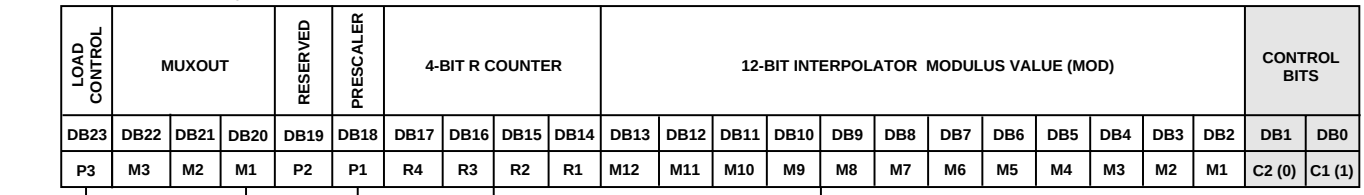
Table 9. R-Divider Register Map



LOAD CONTROL	MUXOUT			RESERVED	PRESCALER	4-BIT R COUNTER				12-BIT INTERPOLATOR MODULUS VALUE (MOD)												CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P3	M3	M2	M1	P2	P1	R4	R3	R2	R1	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	C2 (0)	C1 (1)

P3	LOAD CONTROL
0	NORMAL OPERATION
1	LOAD FAST-LOCK TIMER

P1	PRESCALER
0	4/5
1	8/9

M12	M11	M10		M3	M2	M1	INTERPOLATOR MODULUS VALUE (MOD)
0	0	0	.....	0	1	0	2
0	0	0	.....	0	1	1	3
0	0	0	.....	1	0	0	4
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	4092
1	1	1	.....	1	0	1	4093
1	1	1	.....	1	1	0	4094
1	1	1	.....	1	1	1	4095

R4	R3	R2	R1	RF R-COUNTER DIVIDE RATIO
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

M3	M2	M1	MUXOUT
0	0	0	THREE-STATE OUTPUT
0	0	1	DIGITAL LOCK DETECT
0	1	0	ANALOG LOCK DETECT
0	1	1	N-DIVIDER OUTPUT
1	0	0	LOGIC HIGH
1	0	1	LOGIC LOW
1	1	0	R-DIVIDER OUTPUT
1	1	1	FAST-LOCK SWITCH

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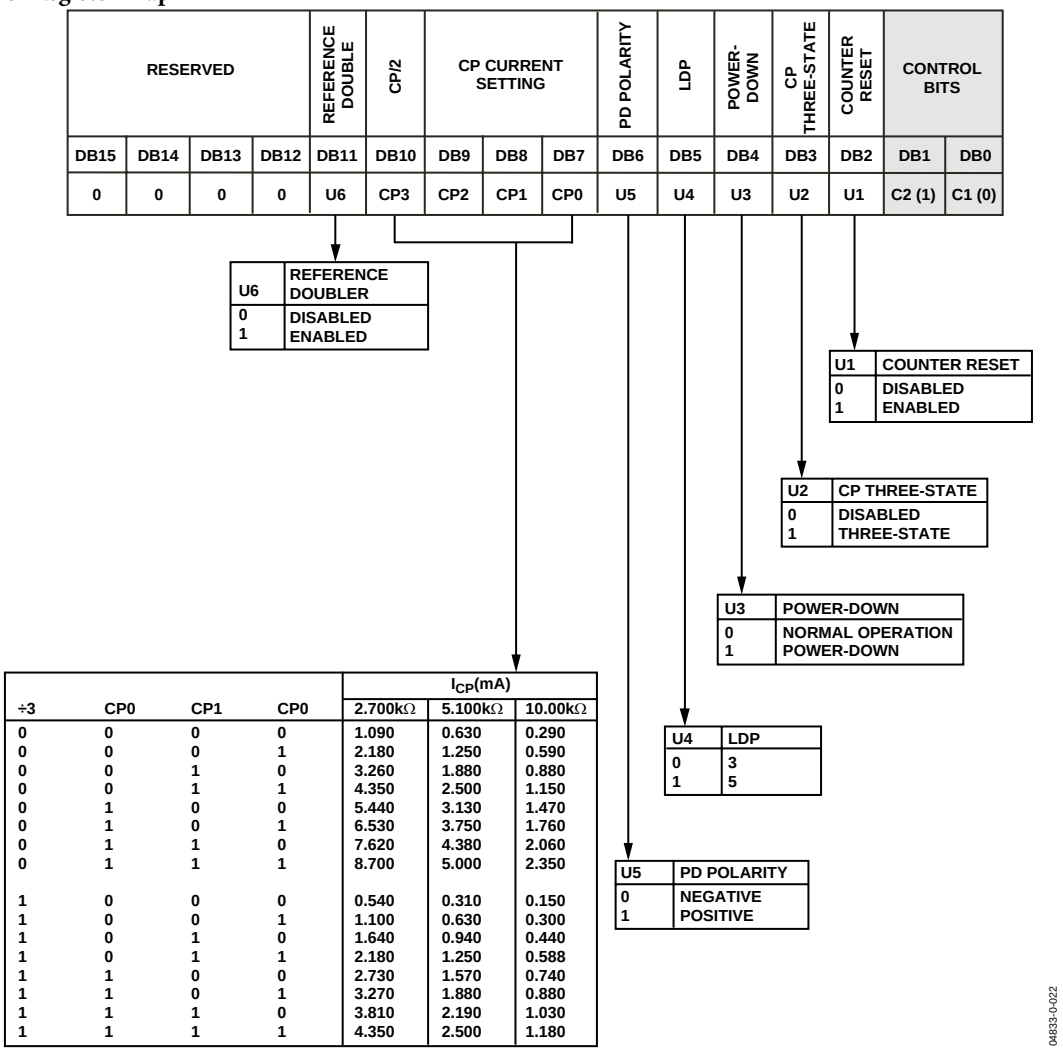
Table 10. Control Register Map



				I_{CP}(mA)		
÷3	CP0	CP1	CP0	2.700kΩ	5.100kΩ	10.00kΩ
0	0	0	0	1.090	0.630	0.290
0	0	0	1	2.180	1.250	0.590
0	0	1	0	3.260	1.880	0.880
0	0	1	1	4.350	2.500	1.150
0	1	0	0	5.440	3.130	1.470
0	1	0	1	6.530	3.750	1.760
0	1	1	0	7.620	4.380	2.060
0	1	1	1	8.700	5.000	2.350
1	0	0	0	0.540	0.310	0.150
1	0	0	1	1.100	0.630	0.300
1	0	1	0	1.640	0.940	0.440
1	0	1	1	2.180	1.250	0.588
1	1	0	0	2.730	1.570	0.740
1	1	0	1	3.270	1.880	0.880
1	1	1	0	3.810	2.190	1.030
1	1	1	1	4.350	2.500	1.180

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REGISTER DEFINITION

N-Divider Register, R0

The on-chip N-divider register is programmed by setting R0[1, 0] to [0, 0]. Table 8 shows the input data format for programming this register.

9-Bit INT Value

These nine bits control what is loaded as the INT value. This is used to determine the overall feedback division factor (see Equation 1).

12-Bit FRAC Value

These 12 bits control what is loaded as the FRAC value into the fractional interpolator. This value helps determine the overall feedback division factor (see Equation 1). The FRAC value must be less than the value loaded into the MOD register.

Fast-Lock

Setting the part to logic high enables fast-lock mode. To use fast-lock, the required time value for wide bandwidth mode needs to be loaded into the R-divider register.

The charge pump current increases from 16× the minimum current and reverts back to 1× the minimum current once the time value loaded has expired.

See the Fast-Lock Timer and Register Sequences section for more information.

R-DIVIDER REGISTER, R1

The on-chip R-divider register is programmed by setting R1[1, 0] to [0, 1]. Table 9 shows the input data format for programming this register.

Load Control

When set to logic high, the value being programmed in the modulus is not loaded into the modulus. Instead, it sets the fast-lock timer. The value of the fast-lock timer/F_{PFD} is the amount of time the PLL stays in wide bandwidth mode.

MUXOUT

The on-chip multiplexer is controlled by R1[22...20] on the ADF4154. Table 9 shows the truth table.

Digital Lock Detect

The digital lock detect output goes high if there are 40 successive PFD cycles with an input error of less than 15 ns. It stays high until a new channel is programmed or until the error at the PFD input exceeds 30 ns for one or more cycles. If the loop bandwidth is narrow compared to the PFD frequency, the error at the PFD inputs may drop below 15 ns for 40 cycles around a cycle slip. Therefore, the digital lock detect may go falsely high for a short period until the error again exceeds 30 ns. In this case, the digital lock detect is reliable only as a loss-of-lock detector.

Prescaler (P/P + 1)

The dual-modulus prescaler (P/P + 1), along with the INT, FRAC, and MOD counters, determines the overall division ratio from the RF_{IN} to the PFD input. Operating at CML levels, it takes the clock from the RF input stage and divides it down for the counters. It is based on a synchronous 4/5 core. When set to 4/5, the maximum RF frequency allowed is 2 GHz. Therefore, when operating the ADF4154 above 2 GHz, this must be set to 8/9. The prescaler limits the INT value.

With P = 4/5, N_{MIN} = 31.
With P = 8/9, N_{MIN} = 91.

The prescaler can also influence the phase noise performance. If INT < 91, a prescaler of 4/5 should be used. For applications where INT > 91, P = 8/9 should be used for optimum noise performance (see Table 9).

4-Bit RF R Counter

The 4-bit RF R counter allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 15 are allowed.

12-Bit Interpolator Modulus/Fast-Lock Timer

Bits DB13–DB2 have two functions depending on the value of the load control bit: modulus or fast lock timer value.

When the load control bit = 0 (DB23), the required modulus may be programmed into the R-divider register (DB13–DB2).

When the load control bit = 1 (DB23), the required fast-lock timer value may be programmed into the R-divider register (DB13–DB2).

This programmable register sets the fractional modulus, which is the ratio of the PFD frequency to the channel step resolution on the RF output. Refer to the RF Synthesizer: A Worked Example section for more information.

The ADF4154 programmable modulus is double-buffered. This means that two events must occur before the part uses a new modulus value. First, the new modulus value is latched into the device by writing to the R-divider register. Second, a new write must be performed on the N-divider register. Therefore, whenever the modulus value is updated, the N-divider register must be written to so that the modulus value is loaded correctly.

CONTROL REGISTER, R2

The on-chip control register is programmed by setting R2[1, 0] to [0, 1]. Table 10 shows the input data format for programming this register.

RF Counter Reset

DB3 is the RF counter reset bit for the ADF4154. When this is 1, the RF synthesizer counters are held in reset. For normal operation, this bit should be 0.

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RF Charge Pump Three-State

This bit puts the charge pump into three-state mode when programmed to 1. It should be set to 0 for normal operation.

RF Power-Down

DB4 on the ADF4154 provides the programmable power-down mode. Setting Bit DB4 to 1 powers down the device. Setting Bit DB4 to 0 returns the synthesizer to normal operation. While in software power-down mode, the part retains all information in its registers. Only when supplies are removed are the register contents lost.

When a power-down is activated, the following events occur:

1. All active dc current paths are removed.
2. The synthesizer counters are forced to their load state conditions.
3. The charge pump is forced into three-state mode.
4. The digital lock detect circuitry is reset.
5. The RF_{IN} input is de-biased.
6. The input register remains active and capable of loading and latching data.

Lock Detect Precision (LDP)

When the LDP bit is programmed to 0, 24 consecutive reference cycles of 15 ns must occur before the digital lock detect is set. When this bit is programmed to 1, 40 consecutive reference cycles of 15 ns must occur before digital lock detect is set.

Phase Detector Polarity

DB6 in the ADF4154 sets the phase detector polarity. When the VCO characteristics are positive, this should be set to 1. When they are negative, it should be set to 0.

Charge Pump Current Setting

DB7, DB8, DB9, and DB10 set the charge pump current, which should be set according to the loop filter design (see Table 10).

REF_{IN} Doubler

Setting the REF_{IN} bit to 0 feeds the REF_{IN} signal directly to the 4-bit RF R counter, which disables the doubler. Setting the REF_{IN} bit to 1 multiplies the REF_{IN} frequency by a factor of 2 before feeding into the 4-bit R counter. When the doubler is disabled, the REF_{IN} falling edge is the active edge at the PFD input to the fractional synthesizer. When the doubler is enabled, both the rising and falling edges of REF_{IN} become active edges at the PFD input.

When the doubler is enabled and the lowest spur mode is chosen, the in-band phase noise performance is sensitive to the REF_{IN} duty cycle. The phase noise degradation can be as much as 5 dB for the REF_{IN} duty cycles outside a 45% to 55% range. The phase noise is insensitive to the REF_{IN} duty cycle in the lowest noise mode and in the lowest noise and spur mode. The phase noise is insensitive to the REF_{IN} duty cycle when the doubler is disabled.

NOISE AND SPUR REGISTER, R3

The on-chip noise and spur register is programmed by setting R3[1, 0] to [1, 1]. Table 7 shows the input data format for programming this register.

Noise and Spur Mode

Noise and spur mode allows the user to optimize a design either for improved spurious performance or for improved phase noise performance. When the lowest spur setting is chosen, dither is enabled. This randomizes the fractional quantization noise so that it looks more like white noise rather than spurious noise. This means that the part is optimized for improved spurious performance. This operation would normally be used when the PLL closed-loop bandwidth is wide for fast-locking applications. A wide-loop bandwidth is seen as a loop bandwidth greater than 1/10 of the RF_{OUT} channel step resolution (f_{RES}). A wide-loop filter does not attenuate the spurs to a level that a narrow-loop bandwidth would. When the low noise and spur setting is enabled, dither is disabled. This optimizes the synthesizer to operate with improved noise performance. However, the spurious performance is degraded in this mode compared to the lowest spurs setting. To further improve noise performance, the lowest noise setting option can be used, which reduces the phase noise. As well as disabling the dither, it ensures that the charge pump operates in an optimum region for noise performance. This setting is extremely useful where a narrow-loop filter bandwidth is available. The synthesizer ensures extremely low noise and the filter attenuates the spurs. The typical performance characteristics give the user an idea of the trade-off in a typical WCDMA setup for the different noise and spur settings.

RESERVED BITS

These bits should be set to 0 for normal operation.

RF SYNTHESIZER: A WORKED EXAMPLE

This equation governs how the synthesizer should be programmed.

$$RF_{OUT} = [INT + (FRAC/MOD)] \times [F_{PFD}] \quad (3)$$

where:

RF_{OUT} is the RF frequency output.
INT is the integer division factor.
$FRAC$ is the fractionality.
MOD is the modulus.

$$F_{PFD} = [REF_{IN} \times (1 = D)/R] \quad (4)$$

where:

REF_{IN} is the reference frequency input.
D is the RF REF_{IN} doubler bit.
R is the RF reference division factor.

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For example, in a GSM 1800 system, where a 1.8 GHz RF frequency output (RF_{OUT}) is required, a 13 MHz reference frequency input (REF_{IN}) is available and a 200 kHz channel resolution (f_{RES}) is required on the RF output.

$$MOD = REF_{IN} / f_{RES}$$
$$MOD = 13\ \text{MHz} / 200\ \text{kHz} = 65$$

From Equation 4,

$$F_{PFD} = [13\ \text{MHz} \times (1 + 0)/1] = 13\ \text{MHz} \quad (5)$$
$$1.8\ G = 13\ \text{MHz} \times (INT + FRAC/65) \geq$$
$$INT = 138;\ \geq FRAC = 30 \quad (6)$$

MODULUS

The choice of modulus (MOD) depends on the reference signal (REF_{IN}) available and the channel resolution (f_{RES}) required at the RF output. For example, a GSM system with 13 MHz REF_{IN} would set the modulus to 65, resulting in the RF output resolution (f_{RES}) of 200 kHz (13 MHz/65) that is necessary for GSM.

REFERENCE DOUBLER AND REFERENCE DIVIDER

The reference doubler on-chip allows the input reference signal to be doubled. This is useful for increasing the PFD comparison frequency. Making the PFD frequency higher improves the noise performance of the system. Doubling the PFD frequency usually results in an improvement in noise performance of 3 dB. It is important to note that the PFD cannot be operated above 32 MHz due to a limitation in the speed of the Σ-Δ circuit of the N divider.

12-BIT PROGRAMMABLE MODULUS

Unlike most other fractional-N PLLs, the ADF4154 allows the user to program the modulus over a 12-bit range. This means that the user can set up the part in many different configurations for the application, when combined with the reference doubler and the 4-bit R counter.

For example, consider an application that requires a 1.75 GHz RF and a 200 kHz channel step resolution. The system has a 13 MHz reference signal.

One possible setup is feeding the 13 MHz directly to the PFD and programming the modulus to divide by 65, which would result in the required 200 kHz resolution.

Another possible setup is using the reference doubler to create 26 MHz from the 13 MHz input signal. The 26 MHz signal is then fed into the PFD, which programs the modulus to divide by 130. This setup also results in 200 kHz resolution and offers superior phase noise performance over the previous setup.

The programmable modulus is also very useful for multistandard applications. If a dual-mode phone requires PDC and GSM 1800 standards, the programmable modulus is a huge benefit. The PDC requires a 25 kHz channel step resolution, whereas the GSM 1800 requires a 200 kHz channel step resolution. A 13 MHz reference signal could be fed directly to the PFD. The modulus would be programmed to 520 when in PDC mode (13 MHz/520 = 25 kHz). The modulus would be reprogrammed to 65 for GSM 1800 operation (13 MHz/65 = 200 kHz). It is important that the PFD frequency remains constant (13 MHz). By keeping the PFD constant, the user can design a one-loop filter that can be used in both setups without running into stability issues. The ratio of the RF frequency to the PFD frequency affects the loop design. Keeping this relationship constant instead of changing the modulus factor results in a stable filter.

SPURIOUS OPTIMIZATION AND FAST-LOCK

The ADF4154 can be optimized for low spurious signals by using the noise and spur register. However, in order to achieve fast-lock time, a wider loop bandwidth is needed. Note that a wider loop bandwidth can lead to notable spurious signals, which cannot be reduced significantly by the loop filter.

Using the fast-lock feature can achieve the same fast-lock time as the noise and spur register, but with the advantage of lower spurious signals, since the final loop bandwidth is reduced by a quarter.

FAST-LOCK TIMER AND REGISTER SEQUENCES

If the fast-lock mode is used, a timer value needs to be loaded into the PLL to determine the time of the wide bandwidth.

When the load control bit = 1, the timer value is loaded via the 12-bit modulus value. To use fast-lock, the PLL must be written to in the following sequence:

1. Load the **R-divider register** with DB23 = 1 and the chosen fast-lock timer value (DB13–DB2) instead of the modulus. Note that the duration of time the PLL remains in wide bandwidth is equal to the fast-lock timer/F_{PFD}.
2. Load the **noise and spur register**.
3. Load the **control register**.
4. Load **R-divider register** with DB23 = 0 and MUXOUT = 110 (DB22–DB20). All the other needed parameters, including the modulus, also need to be loaded.
5. Load the **N-divider register**, including fast-lock = 1 (DB23), to activate fast-lock mode.

Once this procedure is completed, future frequency jumps deploying fast-lock need to repeat only Step 5.

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If fast-lock is not used, then use the following sequence:

1. Load the **noise and spur register**.
2. Load the **control register**.
3. Load the **R-divider register** with DB23 = 0 and other necessary parameters.
4. Load the **N-divider register**, including fast-lock = 0 (DB23) for normal operation.

To change frequency, only Step 4 need be repeated.

FAST-LOCK: A WORKED EXAMPLE

Consider an example in which PLL has reference frequencies of 13 MHz and F_{PFD} = 13 MHz and a required lock time of 50 µs. Therefore, the PLL is set to wide bandwidth for 40 µs.

If the time period chosen for the wide bandwidth is 40 µs, then

Fast-lock timer value = time in wide bandwidth × F_{PFD}
Fast-lock timer value = 40 µs × 13 MHz = 520

Therefore, 520 has to be loaded into the R-divider register in Step 1 of the sequence described in the Fast-Lock Timer and Register Sequences section.

FAST-LOCK: LOOP FILTER TOPOLOGY

To use fast-lock mode, an extra connection from the PLL to the loop filter is needed. The MUXOUT must reduce the damping resistor in the loop filter to ¼ while in wide bandwidth mode. This is required because the charge pump current is increased by 16 while in wide bandwidth mode and stability must be ensured. This can be done with the following two topologies:

1. Divide the damping resistor (R1) into two values (R1 and R1A) of ratio 1:3 (see Figure 22).
2. Use an extra resistor (R1A) and connect it directly from the MUXOUT, as shown in Figure 22. The extra resistor must be chosen such that the parallel combination of an extra resistor and the damping resistor (R1) is reduced to ¼ of the original value of R1 alone (see Figure 23).

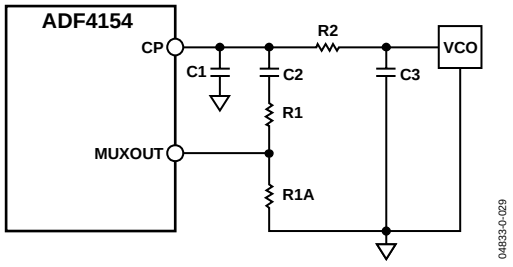

Figure 22 Fast-lock Loop Filter Topology—Topology 1

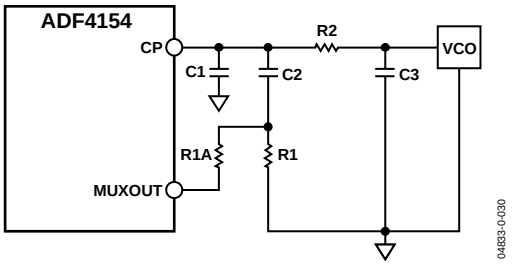

Figure 23. Fast-lock Loop Filter Topology—Topology 2

SPURIOUS SIGNALS

Predicting Where They Appear

As in integer-N PLLs, spurs appear at PFD frequency offsets from the carrier. In a fractional-N PLL, spurs also appear at frequencies equal to the RF_{OUT} channel step resolution (f_{RES}). The third-order fractional interpolator engine of the ADF4154 may also introduce subfractional spurs. If the fractional denominator (MOD) is divisible by 2, spurs appear at ½ f_{RES}. If the fractional denominator (MOD) is divisible by 3, spurs appear at 1/3 f_{RES}. Harmonics of all spurs mentioned also appear. With the lowest spur mode enabled, the fractional and subfractional spurs are attenuated dramatically. The worst-case spurs appear when the fraction is programmed to 1/MOD. For example, in a GSM 900 MHz system with a 26 MHz PFD frequency and an RF_{OUT} channel step resolution (f_{RES}) of 200 kHz, the MOD = 130. PFD spurs appear at 26 MHz offset and fractional spurs appear at 200 kHz offset. Since the MOD is divisible by 2, subfractional spurs are also present at 100 kHz offset.

FILTER DESIGN—ADISIMPLL

A filter design and analysis program is available to help the user implement the PLL design. Visit www.analog.com/pll for a free download of the ADIsimPLL software. The software designs, simulates, and analyzes the entire PLL frequency and time domain response. Various passive and active filter architectures are allowed. Rev. 2 of ADIsimPLL allows analysis of the ADF4154.

INTERFACING

The ADF4154 has a simple, SPI® compatible serial interface for writing to the device. SCLK, SDATA, and LE control the data transfer. When LE (latch enable) is high, the 22 bits that have been clocked into the input register on each rising edge of SCLK are transferred to the appropriate latch. See Figure 2 for the timing diagram and Table 5 for the latch truth table.

The maximum allowable serial clock rate is 20 MHz. This means that the maximum update rate possible for the device is 909 kHz or one update every 1.1 µs. This is more than adequate for systems that have typical lock times in the hundreds of microseconds.

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ADuC812 Interface

Figure 24 shows the interface between the ADF4154 and the ADuC812 MicroConverter®. Since the ADuC812 is based on an 8051 core, this interface can be used with any 8051-based microcontroller. The MicroConverter is set up for SPI master mode with CPHA = 0. To initiate the operation, bring the I/O port driving LE low. Each latch of the ADF4154 needs a 24-bit word, which is accomplished by writing three 8-bit bytes from the MicroConverter to the device. After the third byte is written, the LE input should be brought high to complete the transfer.

When operating in the mode described, the maximum SCLOCK rate of the ADuC812 is 4 MHz. This means that the maximum rate at which the output frequency can be changed is 180 kHz.

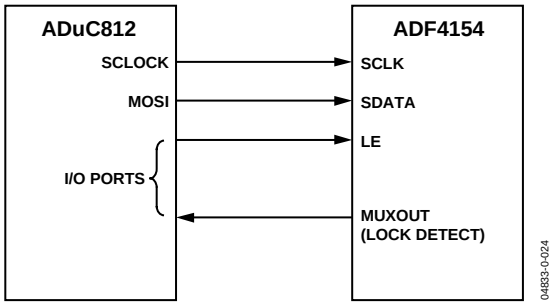

Figure 24. ADuC812 to ADF4154 Interface

ADSP-2181 Interface

Figure 25 shows the interface between the ADF4154 and the ADSP-21xx digital signal processor. As discussed previously, the ADF4154 needs a 24-bit serial word for each latch write. The easiest way to accomplish this using the ADSP-21xx family is to use the autobuffered transmit mode of operation with alternate framing. This provides a means for transmitting an entire block of serial data before an interrupt is generated. Set up the word length for eight bits and use three memory locations for each 24-bit word. To program each 24-bit latch, store each of the three 8-bit bytes, enable the autobuffered mode, and write to the transmit register of the DSP. This last operation initiates the autobuffer transfer.

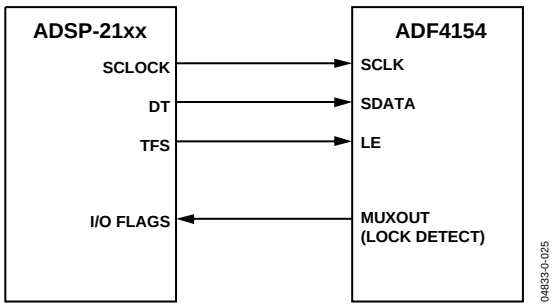

Figure 25. ADSP-21xx to ADF4154 Interface

PCB DESIGN GUIDELINES FOR CHIP SCALE PACKAGE

The lands on the chip scale package (CP-20) are rectangular. The printed circuit board pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land should be centered on the pad. This ensures that the solder joint size is maximized.

The bottom of the chip scale package has a central thermal pad. The thermal pad on the printed circuit board should be at least as large as this exposed pad. On the printed circuit board, there should be a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern to avoid shorting.

Thermal vias may be used on the printed circuit board thermal pad to improve thermal performance of the package. If vias are used, they should be incorporated into the thermal pad at 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm, and the via barrel should be plated with 1 oz. of copper to plug the via.

The user should connect the printed circuit board thermal pad to AGND.

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OUTLINE DIMENSIONS

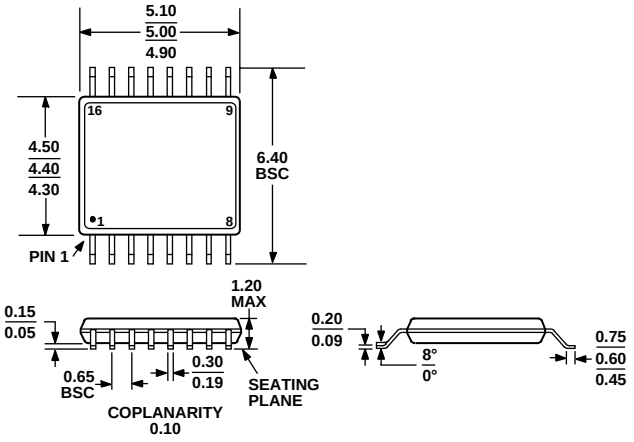

Figure 26. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

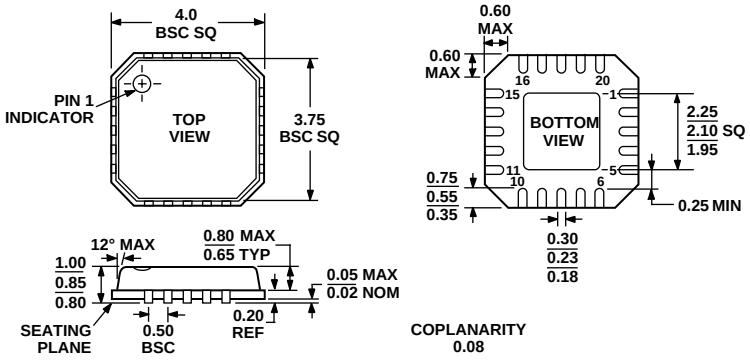

Figure 27. 20-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body, (CP-20)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Description	Temperature Range	Package Option
ADF4154BRU	Thin Shrink Small Outline Package (TSSOP)	−40°C to +85°C	RU-16
ADF4154BRU-REEL	Thin Shrink Small Outline Package (TSSOP)	−40°C to +85°C	RU-16
ADF4154BRU-REEL7	Thin Shrink Small Outline Package (TSSOP)	−40°C to +85°C	RU-16
ADF4154BCP	Lead Frame Chip Scale Package (LFCSP)	−40°C to +85°C	CP-20
ADF4154BCP-REEL	Lead Frame Chip Scale Package (LFCSP)	−40°C to +85°C	CP-20
ADF4154BCP-REEL7	Lead Frame Chip Scale Package (LFCSP)	−40°C to +85°C	CP-20
EVAL-ADF4154EB1			

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