AK2574

156M Laser Diode Driver + APC for Burst Mode

Features

- 156M Laser Diode Driver for burst mode application
- BIAS current switching
- Programmable laser BIAS and modulation current controlled by an on-chip temperature sensor (APC_FF)
- Two current output 8 bit DACs,
  - I-DAC1: 85mA sink for modulation current
  - I-DAC2: 54mA sink for BIAS current
- Power failure alarm (TXACT), CLK failure alarm (CLKALM)
- I²C™ compatible digital I/F
- Duty adjustment
- Single 3.3V +/- 0.2V operation

Applications

ITU-T G.983 ATM-PON ONU

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Description

The AK2574 is a 1chip LDD (Laser Diode Driver) and an APC (Auto Power Control) for burst mode application such as ATM-PON. It contains not only 156M LDD for modulatin current but also BIAS current switching, programmable BIAS and modulation currents, duty adjustment, I²C™ interface, an EEPROM for storing LD characteristics and user information.

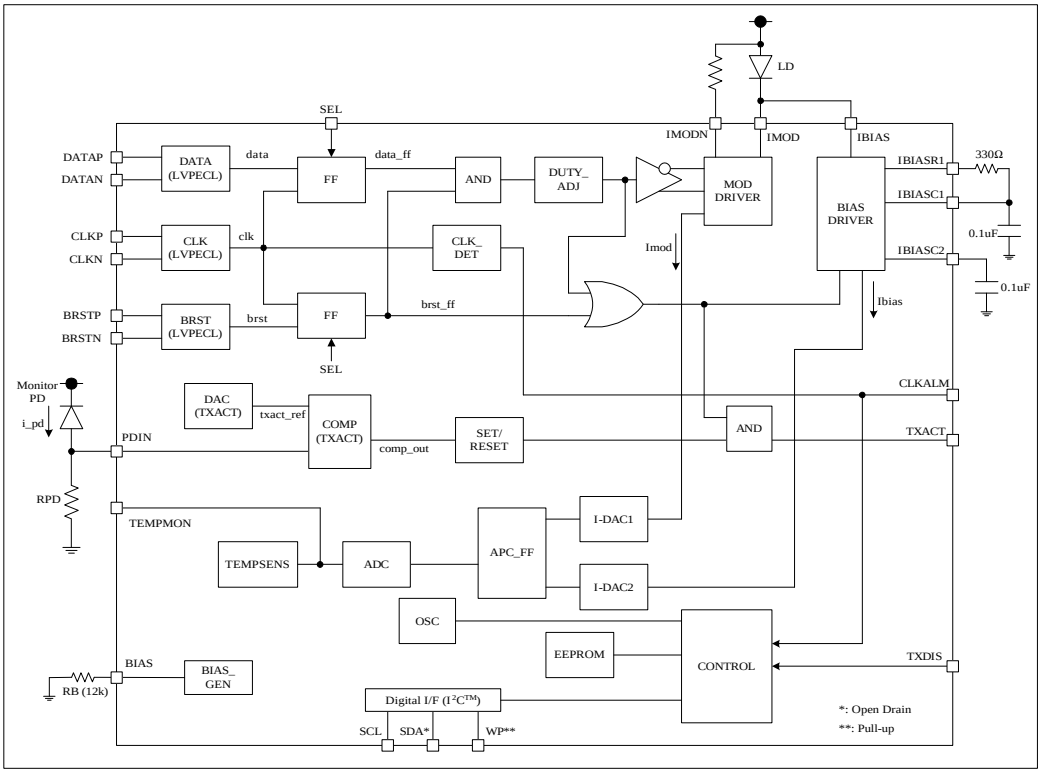
The AK2574 has an APC FF (Feed-forward) function that supplies a programmed current in response to the temperature.

All program and operational functions can be set through the I²C™ compatible interface and stored in the on-chip EEPROM.

Ordering Information

Product Number	PKG
AK2574VB	BCC++48 (7mm * 7mm)

Block Diagram



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Ⅰ. Pin Description

The symbol of I/O column shows below.
Ai: Analog input, Ai_l: LVPECL input, Ao: Analog output
Di: Digital input, Di_pu: Digital input with pulled-up resistor, Do: Digital output,
Dio_od: Digital input / output (open drain)
PWR: Power or VSS

PIN#	Symbol	Function	I/O	Remark
1	SDA	Serial data input / output (Open drain). Connect to VDD with 4.7k to 10kΩ resistor.	Dio_od	AC load ≤ 100pF
2	NC	No Connection. Connect to the VSS (recommended) or leave open.		
3	SCL	Serial clock input. The data (SDA) is shifted in at the rising edge of SCL and is shifted out at the falling edge of SCL.	Di	Do not leave open
4	CLKALM	Sets the alarm when detects 1's or 0's sequential clock input. During CLKALM detection, the AK2574 goes into "TX disable". The detection time is 100ns (typ). The CLKALM is reset when 1 clock is detected. The polarity can be set with EEPROM. When SEL="L", CLKALM is set "non-detected" polarity.	Do	AC load ≤ 30pF
5	TXDIS	TX Disable. The polarity can be set with EEPROM. When set "TX disable", IMOD and IBIAS are Hi-Z. Use 4.7kΩ or more for externally pulled-up or pulled-down.	Di	Do not leave open
6	WP	Write Protect. Internally pulled-up with 20kΩ (typ). "H" sets device address 101000 and only user area of EEPROM can be accessed as read-only. "L" sets device address as 1010 and full of EEPROM can be accessed as read/write.	Di_pu	
7	CLKN	Negative LVPECL clock input. Input Impedance >= 10kΩ. Connect to VSS when SEL = "L".	Ai_l	
8	CLKP	Positive LVPECL clock input. Input Impedance >= 10kΩ. Connect to VDD or leave open when SEL = "L".	Ai_l	
9	SEL	"H" for latched data with clock. DATA (DATAP – DATAN) and BRST (BRSTP – BRSTN) are shifted into the falling edge of CLK. (CLKP – CLKN). "L" for direct data.	Di	Do not leave open
10	DATAN	Negative LVPECL data input. Input Impedance >= 10kΩ	Ai_l	
11	DATAP	Positive LVPECL data input. Input Impedance >= 10kΩ	Ai_l	
12, 13	NC	No Connection. Connect to the VSS or leave open.		
14	TEST6	Test input. Leave open for normal operation.	Do	Leave open
15	BRSTN	Negative LVPECL burst control input. Input Impedance >= 10kΩ	Ai_l	
16	BRSTP	Positive LVPECL burst control input. Input Impedance >= 10kΩ	Ai_l	
17	TEST5	Test input. Connect to VSS for normal operation	Di	Connect to VSS.
18	TEST4	Test input. Connect to VSS for normal operation	Di	
19	TEST3	Test input. Connect to VSS for normal operation	Di	
20	TEST2	Test input. Connect to VSS for normal operation	Di	
21	VSSDR	VSS for MOD driver circuit.	PWR	
22	VDDDR	Power supply for MOD driver circuit.	PWR	
23	VDDMD	Power supply for MOD current circuit.	PWR	
24	VSSMD	VSS for MOD current drive circuit.	PWR	
25, 26	NC	No Connection. Connect to the VSS (recommended) or leave open.		

Pin Description (Continued)

PIN#	Symbol	Function	I/O	Remark
27, 28	IMODN	Negative MOD current output. Sinks MOD current when input data is "L".	Ao	
29, 30	IMOD	Positive MOD current output. Sinks up to 85mA (typ) MOD current when input data is "H". MOD current is adjusted with I-DAC1. IMOD voltage should be (VDD – 1.8V) or more.	Ao	
31	VSSMD	VSS for MOD current drive circuit.	PWR	
32	VSSBI	VSS for BIAS current drive circuit.	PWR	
33, 34	IBIAS	BIAS current output. Sinks up to 54mA (typ) current. BIAS current is adjusted with I-DAC2. IBIAS voltage should be (VDD – 1.8V) or more.	Ao	
35	VSSBI	VSS for BIAS current drive circuit.	PWR	
36	IBIASC1	Connect to VSS with 0.1uF ± 50% (in the operating temerature range) capacitor.	Ao	
37	NC	No Connection. Connect to the VSS (recommended) or leave open.		
38	IBIASC2	Connect to VSS with 0.1uF ± 50% (in the operating temerature range) capacitor.	Ao	
39	IBIASR1	Connect to IBIASSC1 with 330Ω± 1% resistor.	Ao	
40	PDIN	Monitor PD voltage input. Monitor PD current is converted to the voltage with resistor.	Ai	
41	TEMPMON	Temperature sensor monitor output.	Ao	AC load ≤ 30pF DC load ≥ 50kΩ
42	BIAS	BIAS reference for internal circuit. Connect to VSS with 12kΩ± 1% resistor.	Ao	
43	AVDD	Power supply for analog circuit.	PWR	
44	AVSS	VSS for analog circuit.	PWR	
45	TXACT	TXACT is set when PDIN voltage beyond the reference voltage (DACAPC output) and is kept during BRST='H". TXACT is reset when BRST is transient "H"→ "L". The polarity can be set with EEPROM. TXACT is valid within 2ms after power-up.	Do	
46	TEST1	Test input. Connect to VSS for normal operation	Di	Connect to VSS.
47	DVSS	VSS for digital circuit.	PWR	
48	DVDD	Power supply for digital circuit.	PWR	

Center PAD of PKG should be connected to the VSS for good electrical performance and radiation of heat.

Ⅱ. Absolute Maximum Rating

Item	Symbol	Min	Max	Unit	Remarks
Supply Voltage	VDD	-0.3	6.0	V	
GND	VSS	0.0	0.0	V	Reference Voltage
Input voltage	VIN	VSS - 0.3	VDD + 0.3	V	Except VDD
Input Current	IIN	-10	10	mA	Except VDD
Storage Temperature	TSTG	-55	130	℃	Note 1

Stress beyond "Absolute Maximum Range" may cause permanent damage to the device.
Note 1: Except Data retention. Data retention is prescribed at section-Ⅳ 2. EEPROM.

Ⅲ. Recommended Operation Conditions

Item	Symbol	Min	Typ	Max	Unit	Remarks
Operating Ambient	Ta1	-40		85	℃	
Power Supply	VDD1	3.1	3.3	3.5	V	Except AVDD
	VDD2	3.0	3.3	3.5	V	AVDD
	VSS	0.0	0.0	0.0	V	Reference Voltage

Ⅳ. Electrical Characteristics

1. Power Consumption

Item	Symbol	min	typ	max	Unit	Remarks
Supply Current 1 (All VDD)	IDD1	-	8.5	11	mA	Note 1, 2, 4
Supply Current 2 (All VDD)	IDD2		36	41	mA	Note 1, 3, 5
Supply Current 3 (AVDD only)	IDD3	-	10.1	12.5	mA	Note 1, 3, 5

Note 1: without BIAS and modulation current.
Note 2: R_DAC1 = R_DAC2 = 00h, PDIN = 1V.
Note 3: R_DAC1 = R_DAC2 = FFh (Full code), PDIN = 1V.
Note 4: DATAP = BRSTP = "L", DATAN = BRSTP = "H", CLKP = "H", CLKN = "L".
Note 5: 155.52Mbps, PN7, BRSTP="H", BRSTN="L".

2. EEPROM

Item	Min	max	Unit	Remarks
Endurance	10000	-	Write Cycle	Note 1
Data retention	10	-	Year	Junction Temperature = 85℃

Note 1: This parameter is characterized and is not 100% tested.
Important Notice: The AKM factory adjusted data are stored in advance at address location (Device Address = A6h, Address = 60h) for the offset of the on-chip temperature sensor. If such excess temperature stress is to be applied to the AK2574 which exceeds a guaranteed EEPROM data retention conditions (for 10 years at 85℃), it is important to read the pre-determined value in advance and to re-write the same data back into EEPROM after an exposure to the excess temperature environment. Even if the exposure time is shorter than the retention time, any accelerated temperature stress tests (such as baking) are performed, it is recommended to read the pre-set data first and to re-write it after the test. Access to un-used address locations is not functionally guaranteed.
Refer to section-Ⅵ 5.3 for EEPROM map.

3. Digital Input / Output DC Characteristics

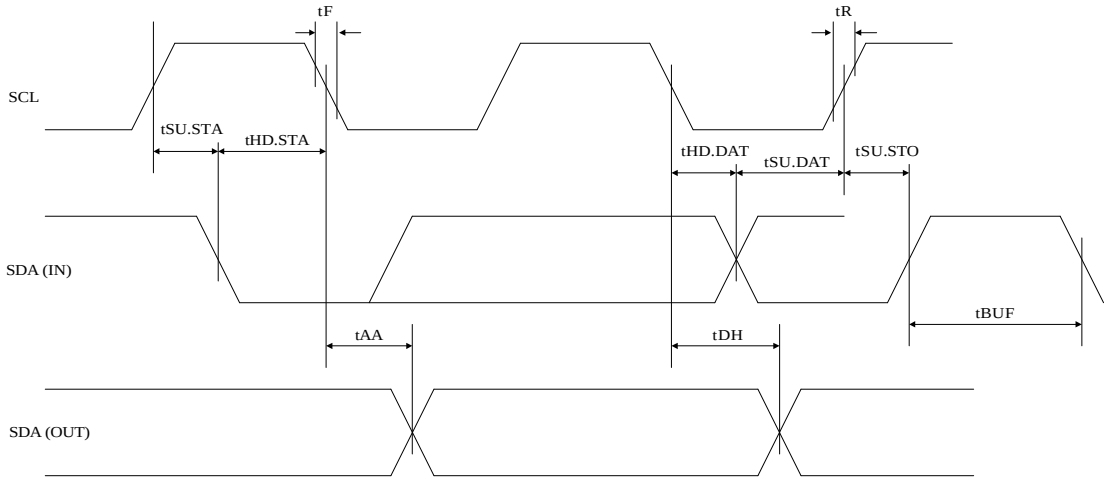
Item	Symbol	min	max	Unit	Conditions
Input High Level	VIH	2.0		V	Note 1
Input Low Level	VIL		0.8	V	
Output High Level	VOH	0.9VDD		V	IOH = -0.2mA
Output Low Level	VOL		0.4	V	IOL = 1mA (SDA) IOL = 0.2mA (Except SDA)
Input Leakage Current 1	IL1		10	uA	except WP pin
Input Leakage Current 2	IL2		350	uA	WP pin

Note 1: except DATAP, DATAN, CLKP, CLKN, BRSTP and BRSTN pins.

4. I²C™ I/F AC Characteristics

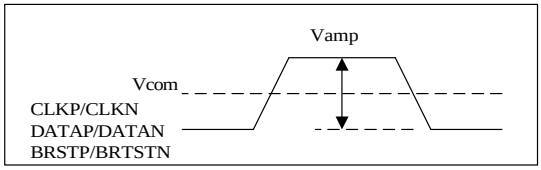
Symbol	Parameter	min	max	Unit	Remark
tSCL	Clock Frequency, SCL		100	kHz	
tLOW	Clock Pulse Width Low	4.7		us	
tHigh	Clock Pulse Width High	4.0		us	
tI	Noise Suppression Time		100	ns	
tAA	Clock Low to Data Out Valid	0.1	4.5	us	
tBUF	Time Before a New Transmission	4.7		us	
tHD.STA	Start Hold Time	4.7		us	
tSU.STA	Start Setup Time	4.0		us	
tHD.DAT	Data Hold Time	0		us	
tSU.DAT	Data Setup Time	200		ns	
tR	Input Rise Time		1.0	us	Note 1
tF	Input Fall Time		0.3	us	Note 1
tSU.STO	Stop Setup Time	4.7		us	
tDH	SDATA Hold Time	100		ns	
tWR	Write Cycle Time		10	ms	

Note 1: This parameter is characterized and is not 100% tested.



5. LVPECL I/F (CLKP, CLKN, DATAP, DATAN, BRSTP, BRSTN)

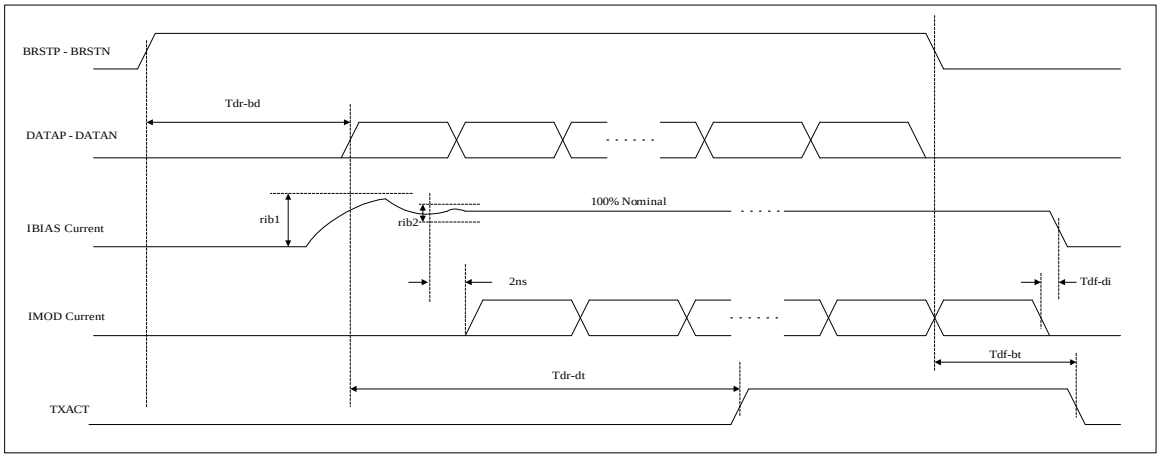
Item	Symbol	min	typ	max	Unit	Remarks
Single-ended Input Voltage Swing	Vamp	0.1		1.2	V	
Common Voltage	Vcom	0.5*VDD		VDD−1.0	V	
BIAS Voltage	Vbias		0.6*VDD		V	
Input Impedance	Zin	10			kΩ	



6. BRST Timing (SEL="L", without CLK)

Item	Symbol	Conditions	min	typ	max	Unit	Remarks
Delay Time of BRST "L"→"H" to First DATA	Tdr-bd		12.8			ns	
Delay Time of Last DATA to IBIAS OFF	Tdf-di	Last Data=1 R_DAC2=0Fh			2	ns	
IBIAS Overshoot	rib1	R_DAC2=0Fh		120	150	%	Note 1
		R_DAC2=2Fh		108		%	
		R_DAC2=FFh		98		%	
IBIAS Error before 2ns of First DATA	rib2	R_DAC2=0Fh			+/-15	%	Note 1
Delay Time of BRST "H"→"L" to TXACT OFF	Tdf-bt	R_DAC2=0Fh			16	ns	
Delay Time of First DATA to TXACT Detection	Tdr-dt		Note 2				

Note 1: This parameter is characterized and is not 100% tested.
Note 2: Depends on TXACT detection level, Monitor PD current, etc. For more information, see "VI. 3.1 TXACT".

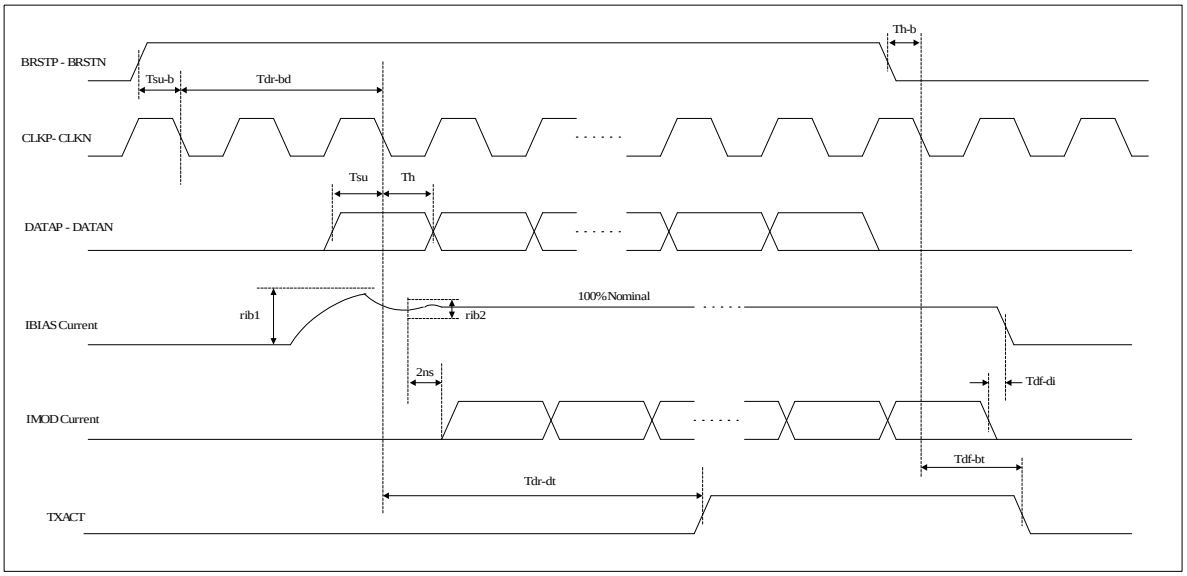


7. BRST Timing (SEL="H", with CLK)

Item	Symbol	Conditions	min	typ	max	Unit	Remarks
DATA Set-up Time	Tsu		1.5				Note 1
DATA Hold Time	Th		1.0				
BRST Set-up Time	Tsu-b		1.5				
BRST Hold Time	Th-b		1.0				
Delay Time of BRST "L"→"H" to First DATA	Tdr-bd		12.8	12.86		ns	
Delay Time of Last DATA to IBIAS OFF	Tdf-di	Last Data=1 R_DAC2=0Fh			2	ns	
IBIAS Overshoot	rib1	R_DAC2=0Fh		120	150	%	Note 1
		R_DAC2=2Fh		108		%	
		R_DAC2=FFh		98		%	
IBIAS Error before 2ns of First DATA	rib2	R_DAC2=0Fh			+/-15	%	Note 1
Delay Time of BRST "H"→"L" to TXACT OFF	Tdf-bt	R_DAC2=0Fh			16	ns	
Delay Time of First DATA to TXACT Detection	Tdr-dt		Note 2				

Note 1: This parameter is characterized and is not 100% tested.

Note 2: Depends on TXACT detection level, Monitor PD current, etc. For more information, see "VI. 3.1 TXACT".



8. I-DAC1

Item	Condition	min	typ	max	Unit	Remark
Resolution			8		bit	
Output Current with Full Code	IMOD = VDD – 1.8V	76	85	94	mA	
Current Supply with Shutdown	IMOD = VDD			100	uA	TXDIS = "1"
1 LSB Current Step	IMOD = VDD – 1.8V		0.333		mA	
DNL	IMOD = VDD – 1.8V	-1		+1	LSB	Code 20h to FFh

9. I-DAC2

Item	Condition	min	typ	max	Unit	Remark
Resolution			8		bit	
Maximum Output Current	IBIAS = VDD – 1.8V R_DAC2=FFh	48	54	60	mA	
Minimum Output Current 1	IBIAS = VDD 1 ≤ R_DAC2 ≤ 5		1.06	1.2	mA	R_DAC2 = 1 to 5
Minimum Output Current 2	IBIAS = VDD R_DAC2 = 0		0		mA	R_DAC2 = 0
Current Supply with Shutdown	IBIAS = VDD			100	uA	TXDIS = "1"
1 LSB Current Step	IBIAS = VDD – 1.8V		0.212		mA	
DNL	IBIAS = VDD – 1.8V	-1		+1	LSB	Code 20h to FFh

10. Duty Cycle Adjustment

Item	Condition	min	typ	max	Unit	Remarks
Maximum Pulse Extended		0.5			ns	Note 1
1 LSB Pulse Extended Step			0.03		ns	32 Steps
Pulse Extended Stability	0.3ns Extended Ta=-40 to 85°C, VDD=3.1～3.5V			0.2	ns	Note 1

Note 1: This parameter is characterized and is not 100% tested.

11. DAC(TXACT)

Item	Condition	min	typ	max	Unit	Remarks
Resolution			3		bit	
Output Voltage	R_CMPTH[2:0]=011	0.86	0.9	0.94	V	
	R_CMPTH[2:0]=010	0.76	0.8	0.84	V	
	R_CMPTH[2:0]=001	0.66	0.7	0.74	V	
	R_CMPTH[2:0]=000	0.56	0.6	0.64	V	
	R_CMPTH[2:0]=100	0.46	0.5	0.54	V	
	R_CMPTH[2:0]=101	0.36	0.4	0.44	V	
	R_CMPTH[2:0]=110	0.26	0.3	0.34	V	
	R_CMPTH[2:0]=111	0.16	0.2	0.24	V	

12. PDIN Capacitance

Item	Condition	min	typ	max	Unit	Remarks
PDIN Capacitance			14	26	pF	

13. BIASGEN

Item	Condition	min	typ	max	Unit	Remark
BIAS pin Voltage			1.2		V	

14. Temperature Sensor

Item	Condition	min	typ	max	Unit	Remark
Voltage Slope	TEMPMON Voltage	-12.14	-11.56	-10.98	mV/°C	Note 1
Offset Adjustment Target	Ta = 35°C		1.215		V	

Note 1: This parameter is characterized and is not 100% tested.

15. ADC

Item	Condition	min	typ	max	Unit	Remark
Resolution			7		bit	
Maximum Input Voltage		2.09	2.2	2.31	V	
Minimum Input Voltage			0		V	
DNL		-1/2		+1/2	LSB	

16. Power On Reset

Item	Condition	min	typ	max	Unit	Remark
Detect Voltage		2.3	2.5	2.7	V	

When detects the voltage drop, the AK2574 goes into shutdown condition.

17. On-chip Oscillator

Item	Condition	min	typ	max	Unit	Remark
Clock Frequency			2.15		MHz	

V. Package Information

(1) Package Type: 48 pin BCC++

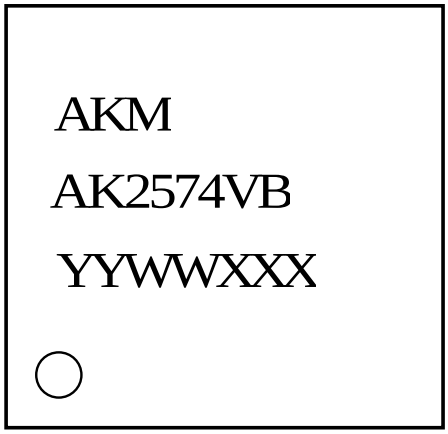
(2) Marking Information:

(a) PIN#1 Indication: ○

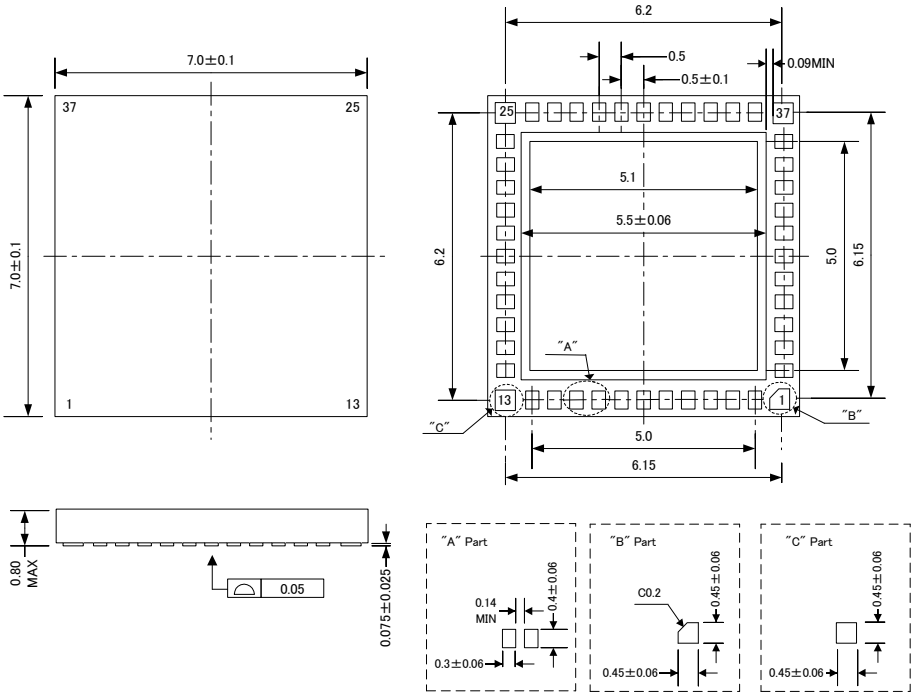
(b) Logo: AKM

(c) Marking Code: AK2574VB

(d) Date Code: YYWWXXX (7 digit)



(3) Package Outline



VI. Circuit Description

1. Parameter Notation

1.1 Parameter Definition

In the AK2574 Circuit Description, in order to distinguish various pre-set parameter sources from EEPROM, Registers or Device pins, "Identifier - Main name" notation is used as shown in Table 1-1. For ease of operational description, small letters sometimes expresses internal signals.

Table 1-1 Parameter Definitions

	Identifier	Main Name	Remark	Example
Register	R_	REGISTER name (All Capital)	Indicates register	R_DAC1
EEPROM	E_	EEPROM name (All Capital))	Indicates EEPROM	E_DAC1
Ether or both Register or /and EEPROM	RE_	REGISTER / EEPROM name (All Capital)	Indicates either register or EEPROM	RE_DAC1
PIN	P_	PIN name (All Capital)		P_PDIN
BLOCK	None	BLOCK name (All Capital))		I-DAC1
Internal Node	None	signal name (small letter)		txact_ref

1.2 Operation Overview

The AK2574 has 3 primary functions; 125M / 156M modulation (MOD) current switching and BIAS current switching part, APC (Automatic Power Control) part, and the Control part to control operation modes of the AK2574 operation.

There are 3 operation modes in the AK2574. Since each adjusting function is controlled through I²C™ Interface, it realizes an automatic parameter adjustment.

(1) Self-running Mode

Self-running mode is ready for normal operation after all adjustments are completed. In this mode, temperature detection, EEPROM access and feeding current are automatically performed using the on-chip oscillator. The AK2574 works in this mode after power-on.

(2) Adjustment Mode

Adjustment mode is designed for training the LD characteristics. The AK2574 operates according to the register settings set through the I²C™ I/F.

(3) EEPROM Mode

EEPROM mode is used for storing LD characteristics into EEPROM via I²C™ I/F.

2. LD Driver

Fig 2-1 illustrates the block diagram of LD driver function.

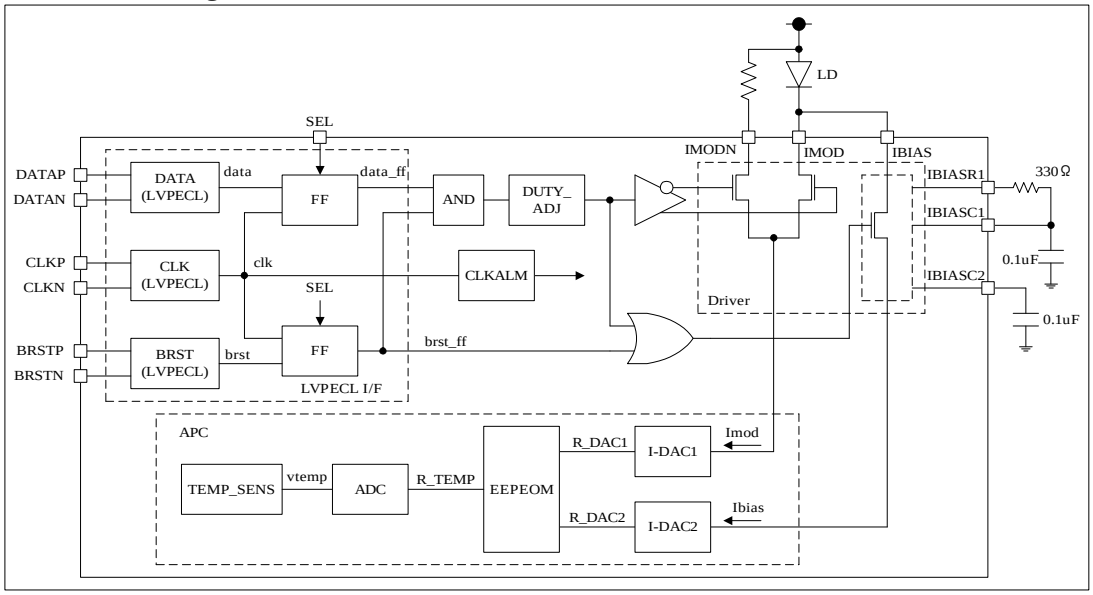
The AK2574 LD driver contains a Driver part, an APC part, a LVPECL I/F part and a programmable duty adjustment.

The driver part is composed of 156M MOD current switching controlled by DATA, and BIAS current switching controlled by BRST.

APC part is composed of a programmable BIAS and MOD currents in response to the temperature (APC_FF), an on-chip temperature sensor, and 2 current DACS (I-DAC1 and I-DAC2).

The LVPECL I/F part is composed of LVPECL I/F for data, clock and the burst control signal (BRST).

Fig 2-1 Driver Block Diagram



2.1 Driver

The 156M MOD driver is composed of the differential current switches, and it sinks the MOD current from IMOD pin when DATA (DATAP – DATAN) = 1 and sinks the current from IMODN when DATA = 0. DATA is set "0" when BRST (BRSTP – BRSTN) = 0.

The BIAS driver is composed of the single-end current switch, and it sinks the BIAS current from IBIAS when BRTS=1. To protect the last LD current at BRST 1→0, BIAS current turned off timing is delayed for a duty extended when the last DATA=1.

2.2 LVPECL I/F (DATAP, DATAN, CLKP, CLKN, BRSTP, BRTSN)

The AK2574 supports direct data or latched data input (see Table 2-1). Connect CLKP = VDD or leave open and CLKN = VSS when SEL = "L".

Table 2-1 Data input

SEL (CMOS)	
"L"	Direct data
"H"	Latched data with clock

2.2.1 LVPECL Input Characteristics

Table 2-2 shows LVPECL input characteristics. The AK2574 LVPECL input, which is biased to 0.6 * VDD with 10k Ω or more impedance respectively.

Table 2-2 LVPEL Interface characteristics

Item	Symbol	min	typ	max	Unit	Reference	Remarks
Single-ended Input Voltage Swing	|Vamp|	0.1		1.2	V	Fig 2-2	
Common Voltage	Vcom	0.5*VDD		VDD−1.0	V	Fig 2-2	
BIAS Voltage	Vbias		0.6*VDD		V	Fig 2-3	
Input Impedance	Zin	10			kΩ	Fig 2-3	
Set-up Time	tsu	1.5			ns	Fig 2-4	Note 1
Hold Time	th	1.0			ns	Fig 2-4	

Note 1: This parameter is characterized and is not 100% tested.

Fig 2-2 DATA/CLK/BRST Input Level

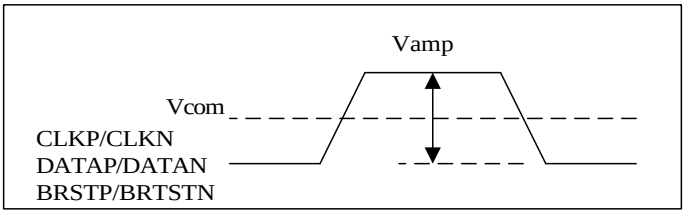


Fig 2-3 LVPECL input circuit

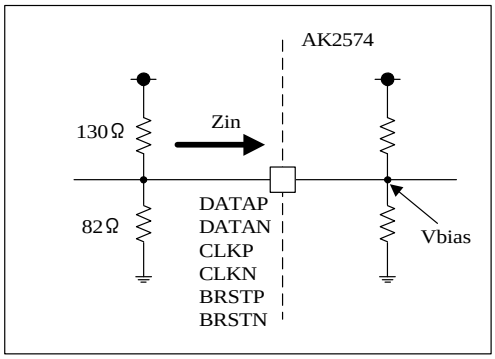
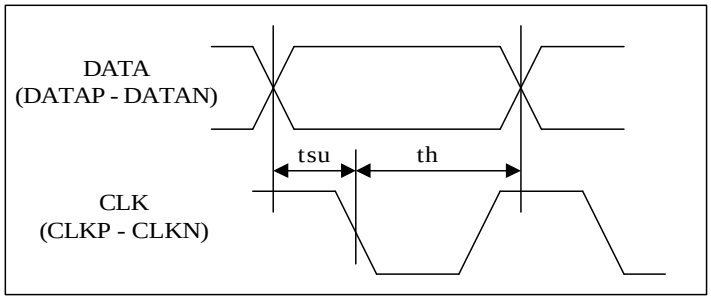


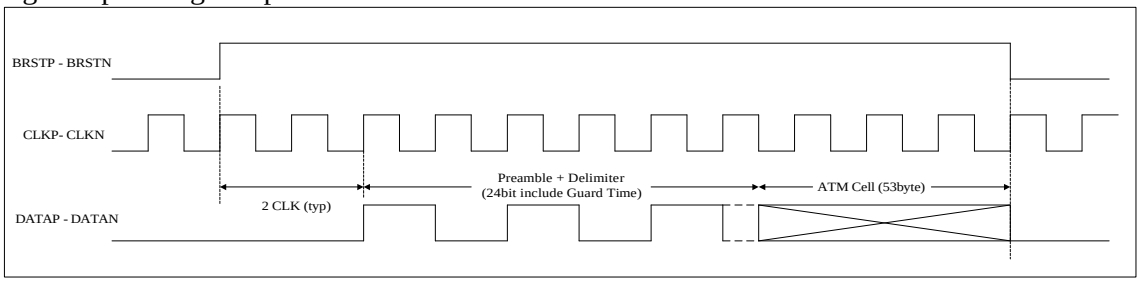
Fig 2-4 Set-up & Hold Time



2.2.2 Input Timing (SEL="H", in the case of the latched DATA with CLK)

BRST (BRSTP – BRSTN) and DATA (DATAP – DATAN) are shifted into AK2574 at the falling edge of CLK (CLKP – CLKN). BIAS driver is turned on within 2 clock (12.8ns max) when BRST = 1. DATA input should be 2 clock (= 12.8ns min) behind BRST = 1. Fig 2-5 illustrates the timing example.

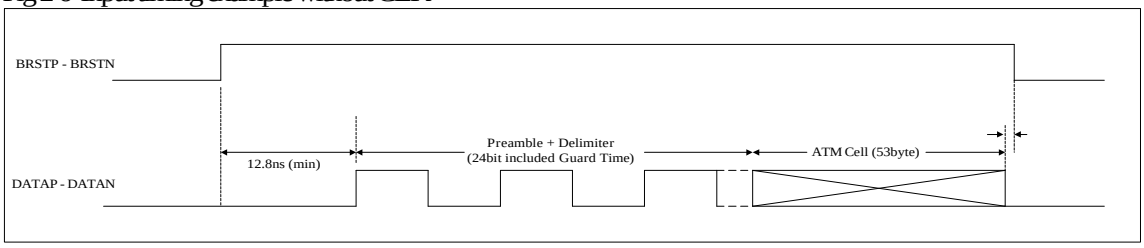
Fig 2-5 Input timing example with CLK



2.2.3 Input Timing (SEL="L", in the case of direct DATA)

AK2574 operates without CLK when SEL="L". DATA input should be 12.8ns or more behind BRST = 0 → 1 transition. To protect the last DATA, BRST 1→0 transition should be behind the last DATA input. Fig 2-6 illustrates the timing example.

Fig 2-6 Input timing example without CLK



2.3 Duty Adjustment

AK2574 supplies a programmed duty adjustment in response to the temperature from an on-chip temperature sensor (every 6℃, Duty data is stored in E_DUTY_TC, see Table 6-3 for more information). Write same data into E_DUTY_TC for constant duty adjustment. Table 2-3 and 2-4 show the characteristics of duty adjustment function.

Table 2-3 Duty Adjustment characteristics

Item	Symbol	min	typ	max	Unit	Remarks
Maximum Pulse Extended	Td	0.5			ns	Note 1
1 LSB Pulse Extended Step	Tstep		0.03		ns	32 Steps
Pulse Extended Stability	Tsta			0.2	ns	Ta=-40 to 85℃, VDDDR=3.1～3.5V 0.3ns Extended (Note 1)

Note 1: This parameter is characterized and is not 100% tested.

Table 2-4 Pulse Extended

R_DUTY	Pulse Extended (typ) [ns]	Remark
0	0	
1	0.03	
2	0.06	
. .	. .	
30	0.90	
31	0.93	

2.4 APC

AK2574 provides the APC (Auto Power Control) function for the burst mode application. APC is composed of a programmable BIAS and MOD currents in response to the temperature (APC_FF), an on-chip temperature sensor, and 2 current DACs (I-DAC1 and I-DAC2).

2.4.1 APC_FF

Fig 2-7 illustrates the APC_FF functions. The operation is as follows:

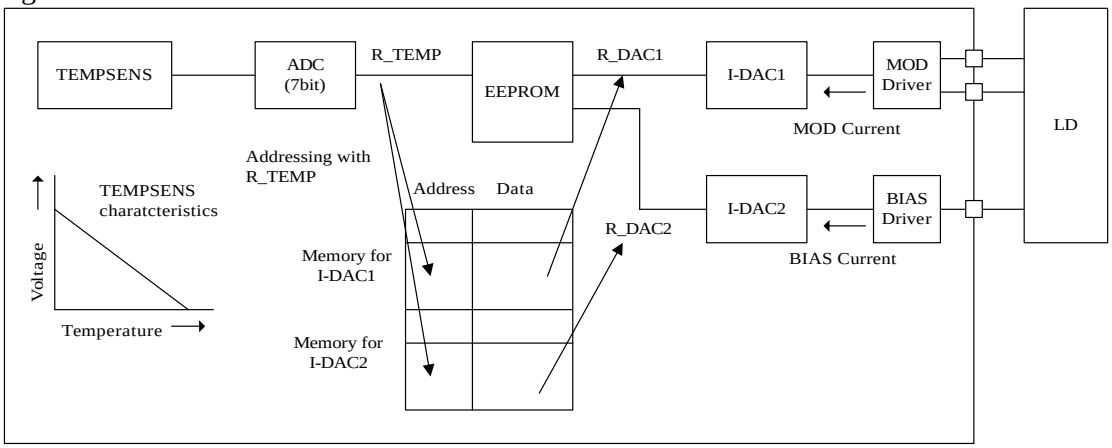
(1) Analog to digital conversion of the voltage (7 bit) that reflects the temperature for every temperature detection period (128ms typ).

(2) Read the 8 bit current data (address is indicated by the ADC data) from EEPROM and set this value to the I-DACs.

If the current data over temperature is set to each EEPROM address, the compensated current is supplied to the LD automatically.

To use this function, current data should be stored in EEPROM in advance. The temperature sensor covers –40℃ to +115℃ and EEPROM is prepared with 1.5℃ steps.

Fig 2-7 APC FF function



2.4.2 I-DAC

AK2574 has two current output 8 bit DACs; I-DAC1 and I-DAC2.

I-DAC1 is 85mA @Full code sink type current DAC for MOD current and I-DAC2 is 54mA @Full code sink type current DAC for BIAS current.

Table 2-5 shows I-DAC1 characteristics and Table 2-6 shows I-DAC2 characteristics.

Table 2-5 I-DAC1 Characteristics

Item	Condition	min	typ	max	Unit	Remark
Resolution			8		bit	
Output Current with Full Code	IMOD = VDD – 1.8V	76	85	94	mA	
1 LSB Current Step	IMOD = VDD – 1.8V		0.333		mA	
DNL	IMOD = VDD – 1.8V	-1		+1	LSB	Code 20h to FFh

Table 2-6 I-DAC2 Characteristics

Item	Condition	min	typ	max	Unit	Remark
Resolution			8		bit	
Maximum Output Current	IBIAS = VDD – 1.8V R_DAC2=FFh	48	54	60	mA	
Minimum Output Current 1	IBIAS = VDD 1 ≤ R_DAC2 ≤ 5		1.06	1.2	mA	See 2.4.3
Minimum Output Current 2	IBIAS = VDD R_DAC2 = 0		0		mA	
1 LSB Current Step	IBIAS = VDD – 1.8V		0.212		mA	
DNL	IBIAS = VDD – 1.8V	-1		+1	LSB	Code 20h to FFh

2.4.3 I-DAC2 Minimum Current Output

Table 2-7 shows the relationship between EEPROM setting (E_DAC2_TC) and I-DAC2 code (R_DAC2). The data to be set to I-DAC2 (R_DAC2) is limited to 5 or more for BIAS current circuit stability. From 1 to 5 code is changed to 5 and is set to I-DAC2. In the case of 0 code, BIAS driver is turned off and IBIAS pin is Hi-Z.

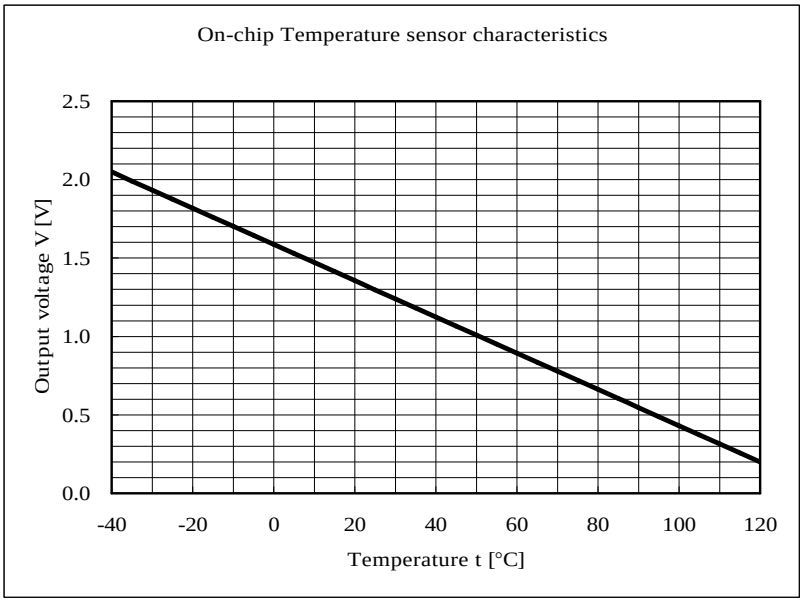
Table 2-7 I-DAC2 Code Setting

E_DAC2_TC	R_DAC2 (I-DAC2 code)	Remarks
0	BIAS Driver = OFF	IBIAS = Hi-Z
1～4	5	Code 1 to 4 is forced to be 5
5 or more	E_DAC2_TC	No modification

2.4.4 Temperature Sensor (TEMPSENS)

Fig 2-8 shows an on-chip temperature sensor characteristics and Table 2-8 shows the relationship between detected temperature and ADC code.

Fig 2-8 On-chip Temperature Sensor Characteristics



(1) Slope: -11.56mV/°C (typ)

(2) V(t) = -0.01156 * t + 1.62 [V] (typ)

(3) AD_code = int(V(t) / 2.2 * 127 +0.5) = int(-0.667*t + 94.0)

(4) Temperature step @ AD_code=1LSB: 1.49°C/LSB

Note: Temperature sensor detects the junction temperature, not LD or ambient temperature.

Table 2-8 AD code and detected temperature [typ]

AD code	Temp [℃]	AD code	Temp [℃]	AD code	Temp [℃]	AD code	Temp [℃]
0	140.1	32	92.2	64	44.2	96	-3.7
1	138.6	33	90.7	65	42.7	97	-5.2
2	137.1	34	89.2	66	41.2	98	-6.7
3	135.6	35	87.7	67	39.7	99	-8.2
4	134.1	36	86.2	68	38.2	100	-9.7
5	132.6	37	84.7	69	36.7	101	-11.2
6	131.1	38	83.2	70	35.2	102	-12.7
7	129.6	39	81.7	71	33.7	103	-14.2
8	128.2	40	80.2	72	32.2	104	-15.7
9	126.7	41	78.7	73	30.7	105	-17.2
10	125.2	42	77.2	74	29.2	106	-18.7
11	123.7	43	75.7	75	27.7	107	-20.2
12	122.2	44	74.2	76	26.3	108	-21.7
13	120.7	45	72.7	77	24.8	109	-23.2
14	119.2	46	71.2	78	23.3	110	-24.7
15	117.7	47	69.7	79	21.8	111	-26.2
16	116.2	48	68.2	80	20.3	112	-27.7
17	114.7	49	66.7	81	18.8	113	-29.2
18	113.2	50	65.2	82	17.3	114	-30.7
19	111.7	51	63.7	83	15.8	115	-32.2
20	110.2	52	62.2	84	14.3	116	-33.7
21	108.7	53	60.7	85	12.8	117	-35.2
22	107.2	54	59.2	86	11.3	118	-36.7
23	105.7	55	57.7	87	9.8	119	-38.2
24	104.2	56	56.2	88	8.3	120	-39.7
25	102.7	57	54.7	89	6.8	121	-41.2
26	101.2	58	53.2	90	5.3	122	-42.7
27	99.7	59	51.7	91	3.8	123	-44.2
28	98.2	60	50.2	92	2.3	124	-45.7
29	96.7	61	48.7	93	0.8	125	-47.2
30	95.2	62	47.2	94	-0.7	126	-48.7
31	93.7	63	45.7	95	-2.2	127	-50.2

3. Alarm

AK2574 has 2 alarm functions as shown in Table 3-1.

Table 3-1 Alarm function

ALM	Detection condition	Release condition	Detected Time
TXACT	When the PDIN voltage (monitor PD current) is beyond the reference voltage (txact_ref). TXACT is kept once TXACT detection until BRST="L".	BRST="L"	Depens on the condition. See "3.1 TXACT" for more information
CLKALM	When the detected 0s or 1s sequential CLK input (100ns typical). When detected CLKALM, AK2574 goes into "Shutdwon".	Polarity of CLK is changed	100ns (typ) 200ns (max)

3.1 TXACT

Fig 3-1illustrates TXACT block diagram. TXACT is detected when the PDIN voltage is beyond the reference voltage (txact_ref), and TXACT is held during BRST = "H". The txact_ref is set with RE_DAC_TXACT. TXACT detection time depends on the Monitor PD current (i_pd) and capacitance (CMPD), external resistor (RPD), AK2574 PDIN capactance (CPDIN) and txact_ref voltage (see Fig 3-2 for the reference).

Table 3-2 shows the PDIN capacitance (CPDIN) and Table 3-3 shouws the relationship between txact_ref and RE_DAC_TXACT. The polarity of TXACT can be set by RE_TXACT_POL (0: "H" at detection, 1: "L" at detection).

The TXACT detection time (t_act) is estimated under the 50% mark data input and average monitor current as follows:

$$t\_act = -RPD * (CMPD + CPDIN) * LN(1 - \frac{txact\_ref}{RPD * i\_pd / 2})$$

Note: TXACT detection time varies with input data pattern.

Fig 3-1 TXACT block diagram

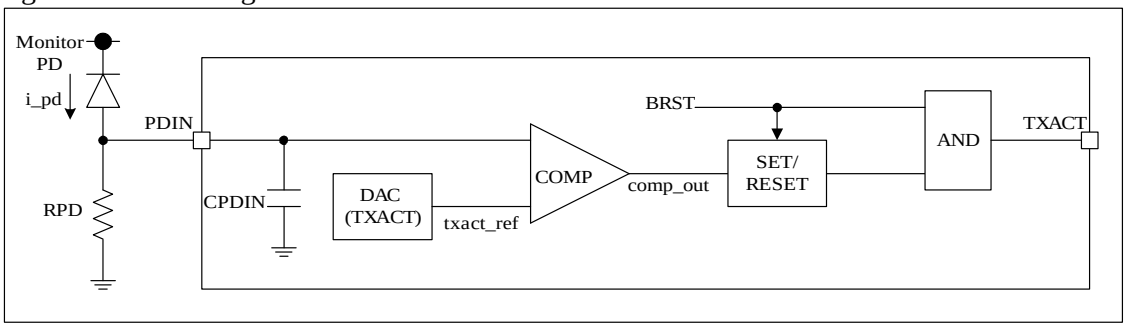


Fig 3-2 Reference figures for TXACT detection time

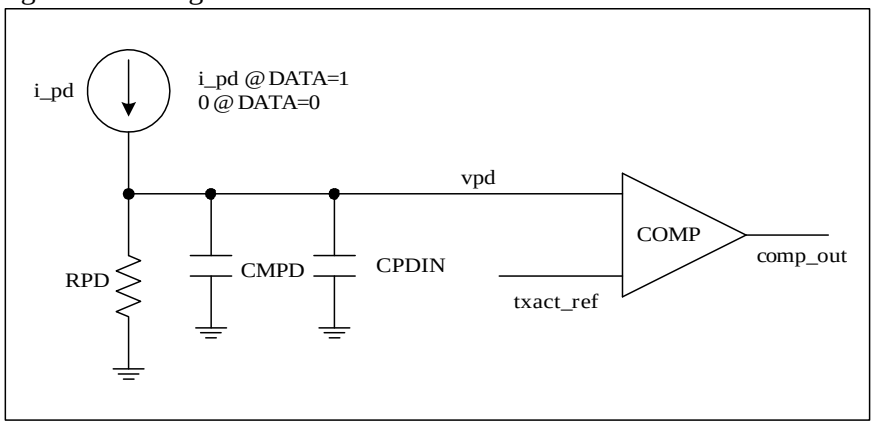


Table 3-2 PDIN capacitance (CPDIN)

Item	min	typ	max	Unit	Remark
PDIN Capacitance (CPDIN)		14	26	pF	

Table 3-3 TXACT Reference Voltage

RE_DAC_TXACT	txact_ref				Remarks
	min	typ	max	unit	
011	0.86	0.9	0.94	V	
010	0.76	0.8	0.84	V	
001	0.66	0.7	0.74	V	
000	0.56	0.6	0.64	V	
100	0.46	0.5	0.54	V	
101	0.36	0.4	0.44	V	
110	0.26	0.3	0.34	V	
111	0.16	0.2	0.24	V	

3.2 CLKALM

CLKALM is detected when input CLK is 0's or 1's fixed more than 100ns (typ). The polarity of CLKALM can be set by RE_CLKALM_POL (0: "H" at detection, 1: "L" at detection). AK2574 goes into "shutdown" (see 4. Shutdown) when CLKALM is detected.

4. Shutdown

Table 4-1 shows the shutdown condition and Table 4-2 shows AK2574 operation at shutdown. AK2574 goes into "Shutdown" when TXDIS request from TXDIS pin or CLKALM detection. The polarity of TXDIS can be set by RE_TXDIS_POL (0: "H" shutdown, 1: "L" shutdown).

Table 4-1 Shutdown Condition

TXDIS (Note1)	CLKALM (Note2)	Operation	Remarks
1	X	Shutdown	Shutdown by pin
0	0	Normal Operation	
0	1	Shutdown	Shutdown by CLKALM detection

Note 1: 1 means shutdown request from TXDIS pin.

Note 2: 1 means CLKALM detection.

Table 4-2 AK2574 operation at shutdown

Function	Operation	Remarks
I-DAC1/2 output	High-Z (0mA output)	
APC_FF	Normal Operation	
MOD Driver	DATA=0	
BIAS Driver	OFF (BRST=0)	
CLKALM	Normal Operation	
TXACT	Hold non-detected polarity	

5. I²C™ I/F

5.1 Memory Map

Table 5-1 shows the EEPROM / Register address map. Access to memory (EEPROM / registers) is done via the I²C™ I/F format.

WP (Write Protect) may limit the access of memory as shown in Table 5-2.

Table 5-1 Memory map

Device Address	Device Address-1	Device Address-2	Address	Data
A0h	1010	000	00000000 to 01111111	User Area (EEPROM, 1kbit)
A0h	1010	000	10000000 to 11111111	No memory
A2h	1010	001	00000000 to 11111111	No memory
A4h	1010	010	00000000 to 11111111	Adjustment data (EEPROM, 3kbit)
A6h	1010	011	00000000 to 01111111	
A6h	1010	011	10000000 to 11111111	No memory
A8h	1010	100	00000000 to 00010011	Registers
A8h	1010	100	00010011 to 11111110	No memory
A8h	1010	100	11111111	AK2574 Operation mode change

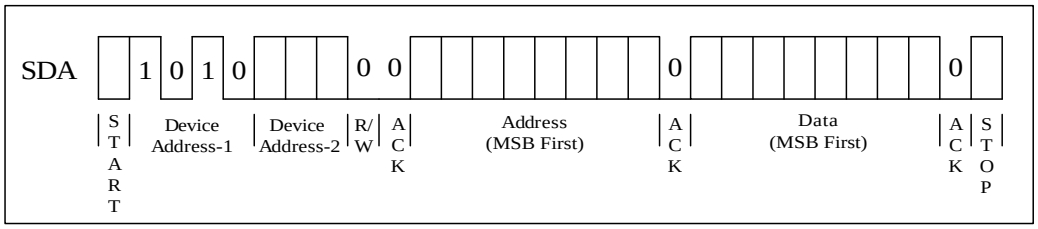
Table 5-2 Memory access limitation with WP

Item	WP = "L"	WP = "H"
Device Address	1010xxx	1010000
ACK (Note 1)	when receive device address	when receive device address
EEPROM / Register Access	Full access	User area only (read only)
Operating mode	Full	Self running mode only
Page Write	16 byte (without registers)	-
Sequential Read	from 00000000000 to 01111111111	from 00000000 to 01111111
Registers Access	Random access only	-

Note 1: During EEPROM Write operation, no ACK is generated.

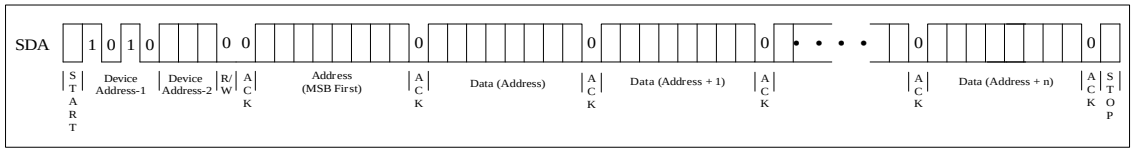
5.2 Read/Write Operation

5.2.1 Byte Write



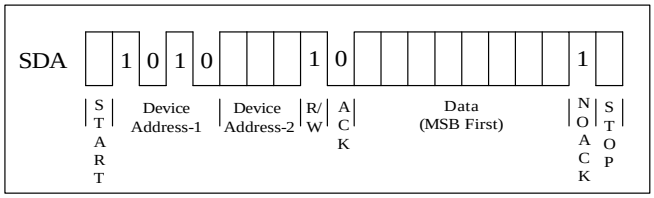
5.2.2 Page Write

AK2574 is capable of 16-byte page write.



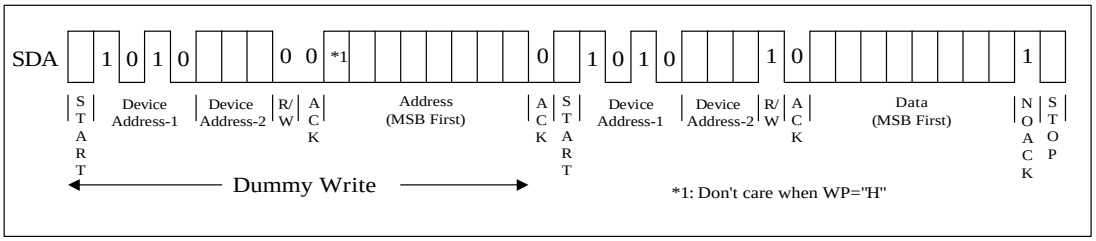
5.2.3 Current Address Read

The internal address counter maintains the last address accessed during the last read or write operation, incremented by one. The roll over address is changed WP setting. Refer to Table 5-2 in detail.



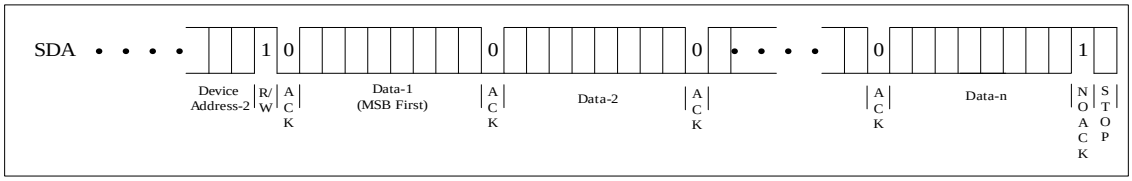
5.2.4 Random Read

A random read requires a "dummy" byte write sequence to specified "Address". After receive the ACK from AK2574, perform "current address read" (see 5.2.2).



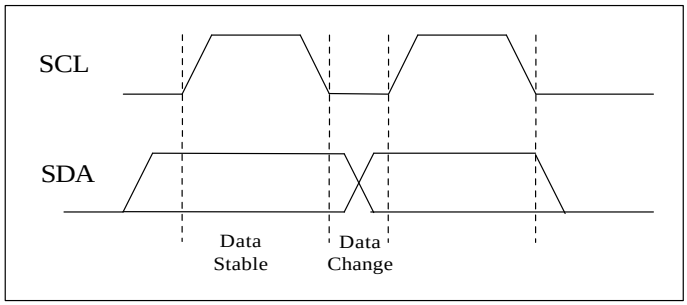
5.2.5 Sequential Read

Sequential read can be initiated as ether "Current Address Read" or "Random Read". After issuing either of them, the AK2574 continues to output data for each ACK received.



5.2.6 Data Change

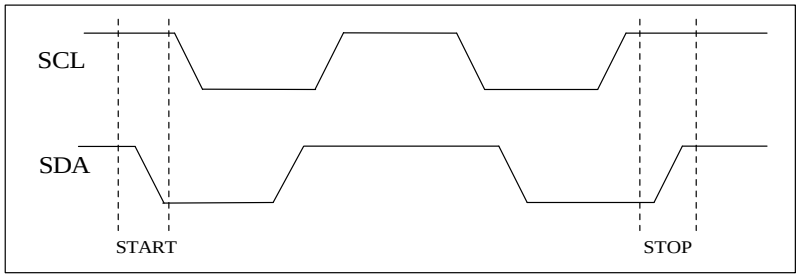
The SDA pin is normally pulled high with 4.7k to 10kΩ. Data on the SDA pin may change only during SCL low time period. Data changes during SCL high periods will indicate a start or stop condition.



5.2.7 Start / Stop Condition

Start Condition: A high-to-low transition of SDA with SCL high is a start condition that must precede any other command.

Stop Condition: A low-to-high transition of SDA with SCL high is a stop condition.



5.3 EEPROM

EEPROM memory map is shown in Table 5-3, 5-4 and 5-5.

EEPROM access is limited with WP pin and Operation mode (refer to Table 6-1, for more information).

WP = "L": Full access

WP = "H": User area only with read only

(Note) The AKM factory adjusted data are stored in advance at address (Device Address = A6h, Address = 60h) for the offset of the on-chip temperature sensor. If such excess temperature stress is to be applied to this device which exceeds a guaranteed EEPROM data retention conditions (for 10 years at 85°C), it is important to read the pre-determined value in advance and to re-write the same data back into EEPROM after an exposure to the excess temperature environment. Even if the exposure time is shorter than the retention time, any accelerated temperature stress tests (such as baking) are performed, it is recommended to read the pre-set data first and to re-write it after the tests.

Table 5-3 EEPROM Address MAP

Device Address	Address	DATA (D7-D0)	Initial Value	Remark
A0h	00h (0) ～ 7Fh (127)	User Area (1kbit)	00h	
A0h	80h (128) ～ FFh (255)	No Memory		
A2h	00h (0) ～ FFh (255)			
A4h	00 h(0) ～ 7F h(127)	E_DAC1_TC Temperature data for I-DAC1 (1kbit)	00h	Addressing with R_TEMP (1.5℃ step)
A4h	80h (128) ～ FFh (255)	E_DAC2_TC Temperature data for I-DAC2 (1kbit)	00h	Addressing with R_TEMP (1.5℃ step)
A6h	00h (0) ～ 1Fh(31)	E_DUTY_TC (256bit) Temperature data for Duty Adjustment	00h	Addressing with MSB 5bit of R_TEMP (6℃ step)
A6h	20h (32) ～ 5Fh (95)	Reserved	00h	
A6h	60h (96) ～ 7Fh (255)	Adjustment data (256bit)	see Table 5-4 and 5-5	

Table 5-4 Adjustment Data Area (Device Address = A6h)

EEPROM 名	Address	Function	Bit	Initial Value	Remark
E_VREFTRIM[7:4]	60h	Oscillator Frequency	4	Factory Setting	
E_TEMP_OFFSET [3:0]	60h	Temperature sensor offset	4		
E_TXDIS_POL[2]	61h	TXDIS Polarity	1	0	0: Shutdown at "H" 1: Shutdown at "L"
E_TXACT_POL[1]	61h	TXACT Polarity	1	0	0: "H" at TXACT detection 1: "L" at TXACT detection
E_CLKALM_POL[0]	61h	CLKALM Polarity	1	0	0: "H" at CLKALM detection 1: "L" at CLKALM detection
E_DAC_TXACT	62h	TXACT Reference Voltage	3	000	see Table 3-2
E_AKM_SET[1:0]	6Dh	AKM 初期設定値	2	00	

Table 5-5 EEPROM Map (Adjustment Data Area)

Address	D7	D6	D5	D4	D3	D2	D1	D0
60h	VREFTRIM				TEMP_OFFSET			
61h						TXDIS_ POL	TXACT_ POL	CLKALM_ POL
62h						DAC_TXACT		
63h-6Ch								
6Dh							AKM_SET	
6Eh-FFh	Reserved							

5.4 Register

Register memory map is shown in Table 5-6 and 5-7. Register access is limited with WP pin and Operation mode (refer to Fig 6-1, for more information).

Table 5-6 Register (Device Address = A8h)

Register	Address	Function	Bit	R/W (Note 1)	Remark
R_VREFTRIM[7:4]	00h	Oscillator Frequency	4	R/W	
R_TEMP_OFFSET [3:0]	00h	Temperature sensor offset	4	R/W	
R_TXDIS_POL[2]	01h	TXDIS Polarity	1	R/W	0: Shutdown at "H" 1: Shutdown at "L"
R_TXACT_POL[1]	01h	TXACT Polarity	1	R/W	0: "H" at TXACT detection 1: "L" at TXACT detection
R_CLKALM_POL[0]	01h	CLKALM Polarity	1	R/W	0: "H" at CLKALM detection 1: "L" at CLKALM detection
R_DAC_TXACT[2:0]	02h	DAC(TXACT)	3	R/W	see Table 3-2
R_TXACT_THRU[0]	04h	TXACT Hold	1	R/W	0: TXACT Hold (Normal Operation) 1: TXACT (Real-Time)
R_DAC1[7:0]	05h	I-DAC1 Current Setting	8	R/W	see Table 2-5
R_DAC2[7:0]	06h	I-DAC2 Current Setting	8	R/W	see Table 2-6
R_DUTY[4:0]	07h	Duty Adjustment	5	R/W	see Table 2-4
R_MODE[3:0]	08h	Operation Mode Status	4	R	see Table 6-3
R_TEMP[6:0]	0Ch	Detected Temperature	7	R	see Table 2-8
AKM Test	0Dh - 13h	Test for AKM (Reserved)		NA	Reserved

Note 1:

R: Read Only.

R/W: Read/Write, Write data is hold unless re-writing or operation mode changing. All adjustment would be done by R/W registers.

Table 5-7 Register Map

Address	D7	D6	D5	D4	D3	D2	D1	D0
00h	VREFTRIM				TEMP_OFFSET			
01h						TXDIS_POL	TXACT_POL	CLKALM_POL
02h						DAC_TXACT		
03h								
04h								TXACT_THRU
05h	DAC1							
06h	DAC2							
07h				DUTY				
08h					MODE			
09h								
0Ah								
0Bh								
0Ch		TEMP						
0Dh – 13h	Reserved (AKM Test)							

6. Operation Mode

The AK2574 has 3 operating modes: Self-running, Adjustment and EEPROM mode.

6.1 Self-running Mode

Self-running mode is ready for normal operation after all adjustments are completed. In this mode, temperature detection, EEPROM access and feeding current are automatically performed using the on-chip oscillator. The AK2574 works in this mode after power-on.

6.2 Adjustment Mode

Adjustment mode is designed for training the LD characteristics. The AK2574 operates according to the register settings set through the I²C™ I/F.

6.3 EEPROM Mode

EEPROM mode is used for storing LD characteristics into EEPROM. Transition from EEPROM mode to Adjustment mode is prohibition.

6.4 MODE Control

The AK2574 operation modes are changed through the I²C™ interface. Table 6-1 shows the access limitation of each operation mode and Table 6-2 shows the command to change operation mode.

Note: The I²C™ interface access is prohibited for 2ms after power-on or mode transfer to self-running mode.

Table 6-1 Access limitation of each operation mode

	EEPROM Access		Register Access	
Operation mode	Read	Write	Read	Write
Self-running mode (WP='L')	○	×	○	× (except mode-change command)
Adjustment mode (WP='L')	○	×	○	○
EEPROM mode (WP='L')	○	○	○	× (except mode-change command)
WP = 'H' Self-running mode only	○ (User Area Only)	×	×	×

Table 6-2 Operation mode change

Device Address	R/W	Address	Data	Operation mode
1010100	W	11111111	10100000	Self-running mode
1010100	W	11111111	10100111	Adjustment mode
1010100	W	11111111	10101110	EEPROM mode

6.5 Operation Mode Protection

When set WP = 'H', only self-running mode is selected.

6.6 Operation Mode Status

Operation mode is stored in R_MODE register. Table 6-3 shows the relationship between the Operation mode and R_MODE. When set WP = 'H', access to R_MODE is prohibition.

Table 6-3 R_MODE

Operation mode	R_MODE[3:0]
Self-running mode	0000
Adjustment mode	0111
EEPROM mode	1110

7. Module Adjustment Example

Table 7-1 shows the module adjustment example.

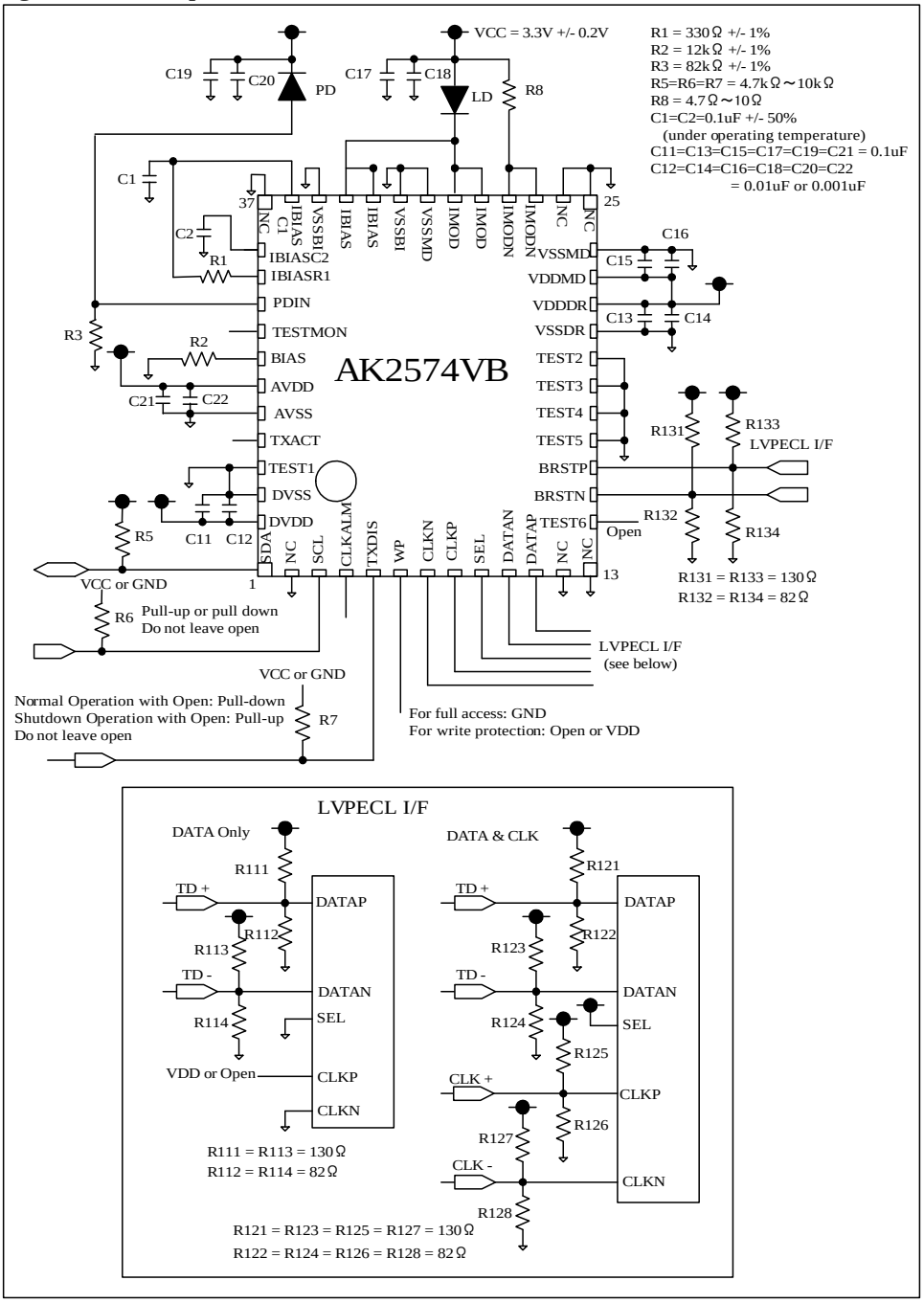
Table 7-1 Module Adjustment Example

No.	Item	Contents
1	Go to Adjustment mode	Issues "Changing to Adjustment mode command" (see Table 5-2) via I²C™ I/F.
2	Continuous operation	Set BRST="H" to operate AK2574 as a continuous operation.
3	LD current adjustment	Adjust R_DAC1 for modulation current and R_DAC2 for BIAS current of LD.
4	Duty adjustment	Adjust R_DUTY for 50% duty of LD power, if necessary. After duty adjustment, tune MOD and BIAS current by R_DAC1 and R_DAC2, if necessary.
5	TXACT adjustment	Adjust LD power by R_DAC1 and R_DAC2 to 3dB down of minimum LD power that you would like to detect TXACT. Input the burst control signal and adjust R_DAC_TXACT for tunning TXACT detection time. For more information, see "3.1 TXACT".
6	Verification of TXACT	Set R_DAC1 and R_DAC2 back to normal power. Confirm TXACT detection time.
7	Read temperature data	Read R_TEMP (on-chip temperature sensor detection temperature).
8	Estimate LD temperature characteristics	(1) 2 or more temperature adjustment Do step 2 to 8 with different temperature and estimate LD current data of look-up table. (2) Single point adjustment Calculate LD current data of look-up table with on-chip temperature sensor gain (-1.49°C/LSB), R_TEMP and LD characteristics.
9	Write adjustment data to EEPROM	(1) Make the data for EEPROM. (2) Issue mode change command to EEPROM. (3) Write adjustment data to EEPROM. (4) Read EEPROM data and verify it.
10	Self running mode	Issue mode change command to self-running. AK2574 operates temperature detection, feed current in response to temperature, and a feedback operation automatically according to the data in EEPROM.

Ⅶ. Circuit Example

Fig-A illustrates circuit example of AK2574.

Fig-A Circuit Example



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