AK2573A

125M / 156M Laser Diode Driver + APC

Features

- 1 chip 125M / 156M Laser Diode Driver (LDD) + Digital APC (APC_FF and APC_FB)
- Programmable laser BIAS and modulation current controlled by an on-chip temperature sensor (APC_FF)
- Digital feedback circuit for APC (APC FB)
- Two current output 8 bit DACs,
  - I-DAC1: 85mA sink for modulation current
  - I-DAC2: 54mA sink for BIAS current
- TXFAULT detection and 1kbit ID Field (EEPROM) for SFP (Small Form-factor Pluggable) support
- I²C™ compatible digital I/F
- Duty adjustment
- Power failure alarm (OPTALM), Over current alarm (CURRALM), Temperature alarm (TEMPALM), Data alarm (DATAALM) and TXFAULT for failure alarm
- BIAS and modulation current monitors (*0.0095)
- Single 3.3V +/- 0.2V operation

Applications

STM-1 / OC-3 (156Mbps) Optical Interface Module
TS–1000 (125Mbps) Optical Interface Module

Description

The AK2573A is a 1chip LDD (Laser Diode Driver) and an APC (Auto Power Control) for laser direct modulation application. It contains up to 156M LDD, programmable duty adjustment, BIAS and modulation currents, a digital feedback circuit, BIAS and modulation current monitors, failure alarms, I²C™ interface, an EEPROM for storing LD characteristics and user information, and TXFAULT detection for SFP application. The AK2573A has two APC functions; APC FF (Feed-forward) and APC FB (Feedback). APC FF supplies a programmed current in response to the temperature. APC FB provides a stable auto power control function with an internal digital feedback algorithm.

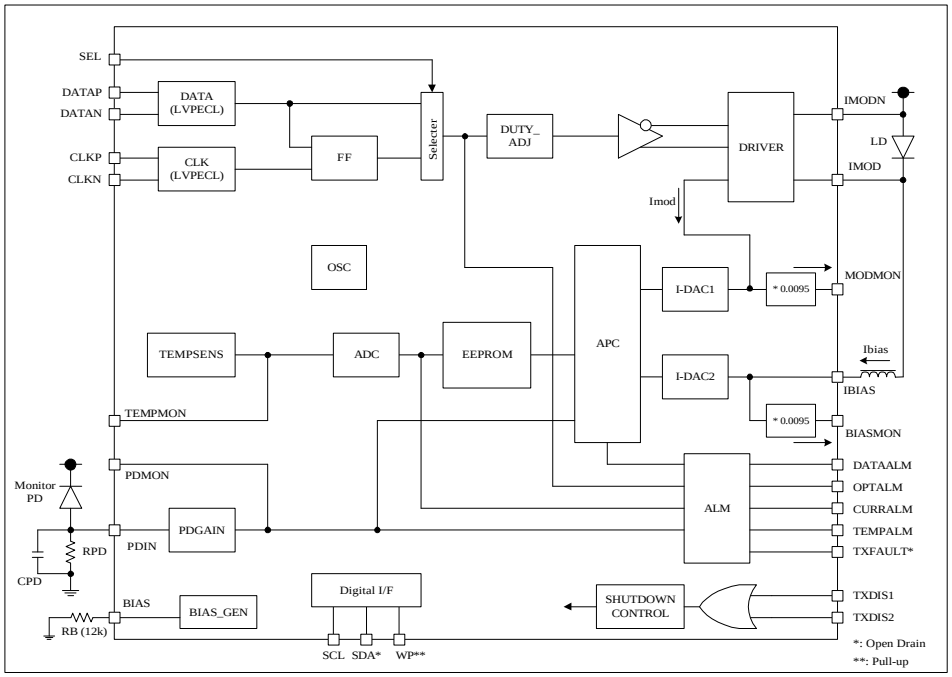
All program and operational functions can be set through the I²C™ compatible interface and stored in the on-chip EEPROM.

Ordering Information

Product Number	PKG
AK2573AVB	BCC++48 (7mm * 7mm)

I²C™ is a trademark of Philips Corporation.

Block Diagram



-Contents-

Ⅰ. Pin Description

The symbol of I/O row shows below.
Ai: Analog input, Ai_l: LVPECL input, Ao: Analog output
Di: Digital input, Di_pu: Digital input with pulled-up resistor, Do: Digital output, Dio: Digital input / output,
Do_od: Digital output (open drain), Dio_od: Didital input / output (open drain)
PWR: Power or VSS

PIN#	Symbol	Function	I/O	Remark
1	NC	No Connection. Connect to the VSS or leave open.		
2	DATAP	Positive LVPECL data input. Input Inpedance >= 10kΩ	Ai_l	
3	DATAN	Negative LVPECL data input. Input Indedance >= 10kΩ	Ai_l	
4	SEL	"H" for latched data with clock. "L" for direct data.	Di	Do not leave open
5	CLKP	Positive LVPECL clock input. Connect to VSS when SEL = "L".	Ai_l	
6	CLKN	Negative LVPECL clock input. Connect to VDD or leave open when SEL = "L".	Ai_l	
7	WP	Write Protect. Internally pulled-up with 20kΩ (typ). "H" sets device address 101000 and only user area of EEPROM can access as read-only. "L" sets device address as 1010 and full of EEPROM can access as read/write. For more information, see Table 8-2 and 9-1.	Di_pu	
8	TXDIS1	TX Disable. "H" for disable MOD and BIAS current. TXDIS1 and TXDIS2 are ORed internally. Use 4.7kΩ or more for externally pulled-up or pulled-down.	Di	Do not leave open
9	TXDIS2			
10	DVDD	Power supply for digital circuit.	PWR	
11	TXFAULT	TX Fault detection output (Open drain). Connect to VDD with 4.7kΩ to 10kΩ resistor. Set "H" when detect TEMPALM, CURRALM, OPTALM or DATAALM. When set RE_SFP=1 and detect the ALM, TXFAULT is kept "H" until receiving disable request at TXDIS1 or TXDIS2.	Do_od	AC load ≤ 100pF
12	NC	No Connection. Connect to the VSS or leave open.		
13	SDA	Serial data input / output (Open drain). Connect to VDD with 4.7k to 10k resistor.	Dio_od	AC Load ≤ 100pF Do not leave open
14	SCL	Serial clock input. The data (SDA) is shifted in at the rising edge of SCL and is shifted out at the falling edge of SCL.	Di	Do not leave open
15	DVSS	VSS for digital circuit.	PWR	
16	NC	No Connection. Connect to the VSS or leave open.		
17	DATAALM	Sets the alarm when detects 1's or 0's sequential data input. The detection time is 4.5us (typ). The polarity can be set with EEPROM.	Do	AC Load ≤ 30pF
18	OPTALM	Sets the alarm when detects monitor PD current drop. The polarity can be set with EEPROM.	Do	AC Load ≤ 30pF
19	CURRALM	Sets the alarm when detects the over current of I-DAC1 or I-DAC2. Alarm level can be set every 6℃. The polarity can be set with EEPROM.	Do	AC Load ≤ 30pF

Pin Description (Continued)

PIN#	Symbol	Function	I/O	Remark
20	TEMPALM	Sets the alarm when detects the over temperature. The polarity can be set with EEPROM.	Do	AC Load ≤ 30pF
21	TEMPMON	Temperature sensor monitor output.	Ao	AC load ≤ 30pF DC load ≥ 50kΩ
22	BIAS	BIAS reference for internal circuit. Connect to VSS with 12k +/- 1% resistor.	Ao	
23	PDMON	PDIN regulated output. Adjust PDGAIN to PDMON = 1V (typ).	Ao	AC load ≤ 30pF DC load ≥ 50kΩ
24	AVSS	VSS for analog circuit.	PWR	
25	AVDD	Power supply for analog circuit. Connect to the power supply through R-C LPF (R=10Ω, C=1uF is recommended).	PWR	
26	PDIN	Monitor PD voltage input. Monitor PD current is converted to the voltage with resistor and capacitor that has 1kHz to 10kHz cut-off frequency.	Ai	
27	VSSBI	VSS for BIAS current drive circuit.	PWR	
28 29	IBIAS	BIAS current output. Sinks up to 54mA (typ) current. BIAS current is adjusted with I-DAC2. IBIAS voltage should be (VDD – 1.8V) or more.	Ao	
30	VSSBI	VSS for BIAS current drive circuit.	PWR	
31	VSSMD	VSS for MOD current drive circuit.	PWR	
32 33	IMOD	Positive MOD current output. Sinks up to 85mA (typ) MOD current when input data is "H". MOD current is adjusted with I-DAC1. IMOD voltage should be (VDD – 1.8V) or more.	Ao	
34 35	IMODN	Negative MOD current output. Sinks MOD current when input data is "L".	Ao	
36	VSSMD	VSS for MOD current drive circuit.	PWR	
37	VDDMD	Power supply for MOD current circuit.	PWR	
38	NC	No Connection. Connect to the VSS or leave open		
39	VDDDR	Power supply for MOD driver circuit.	PWR	
40	VSSDR	VSS for MOD driver circuit.	PWR	
41	BIASMON	BIAS monitor current output. Sources 0.0095 times current of I-DAC2 (BIAS) current. BIASMON voltage should be 1.3V or less.	Ao	
42	MODMON	MOD Monitor current output. Sources 0.0095 times current of I-DAC1 (modulation) current. BIASMON voltage should be 1.3V or less.	Ao	
43	TEST1	Test input. Connect to VSS for normal operation	Di	Connect to VSS.
44	TEST2	Test input. Connect to VSS for normal operation	Di	
45	TEST3	Test input. Connect to VSS for normal operation	Di	
46	TEST4	Test input. Connect to VSS for normal operation	Di	
47	TEST5	Test input. Connect to VSS for normal operation	Di	
48	TEST6	Test input. Leave open for normal operation.	Do	Leave open

Center PAD of PKG should be connected to the VSS for good electrical performance and radiation of heat.

Ⅱ. Absolute Maximum Rating

Item	Symbol	Min	Max	Unit	Remarks
Supply Voltage	VDD	-0.3	6.0	V	
GND	VSS	0.0	0.0	V	Reference Voltage
Input voltage	VIN	-0.3	VDD+0.3	V	Except VDD
Input Current	IIN	-10	10	mA	Except VDD
Storage Temperature	TSTG	-55	130	℃	Note 1

Stress beyond "Absolute Maximum Range" may cause permanent damage to the device.
Note 1: Except Data retention. Data retention is prescribed at section-Ⅳ (2) EEPROM.

Ⅲ. Recommended Operation Conditions

Item	Symbol	Min	Typ	Max	Unit	Remarks
Operating Ambient	Ta1	-40		85	℃	
Power Supply	VDD1	3.1	3.3	3.5	V	Except AVDD
	VDD2	3.0	3.3	3.5	V	AVDD
	VSS	0.0	0.0	0.0	V	Reference Voltage

Ⅳ. Electrical Characteristics

1. Power Consumption

Item	Symbol	min	typ	max	Unit	Remarks
Supply Current 1 (All VDD)	IDD1	-	7.8	9.4	mA	Note 1, 2, 3
Supply Current 2 (All VDD)	IDD2		15	20	mA	Note 1, 2, 4
Supply Current 3 (AVDD only)	IDD3	-	-	5	mA	Note 1, 5

Note 1: without BIAS and modulation current
Note 2: I-DAC1 = 0, I-DAC2 = 0, Gain = 1, PDGAIN = 0dB, PDIN = 1V
Note 3: DATAP = CLKP = "L", DATAN=CLKN = "H"
Note 4: 155.52Mbps, PN7
Note 5: I-DAC1 = I-DAC2 = FFh (Full code), Gain = 1, PDGAIN = 0dB, PDIN = 1V

2. EEPROM

Item	min	max	Unit	Remarks
Endurance	10000	-	Write Cycle	Note 1
Data retention	10	-	Year	Junction Temperature = 85℃

Note 1: This parameter is characterized and is not 100% tested.
Important Notice: The AKM factory adjusted data are stored in advance at address location (Device Address = A6h, Address = 60h) for the offset of the on-chip temperature sensor. If such excess temperature stress is to be applied to the AK2573A which exceeds a guaranteed EEPROM data retention conditions (for 10 years at 85C), it is important to read the pre-determined value in advamce and to re-write the same data back into EEPROM after an exposure to the excess temperature environment. Even if the exposure time is shorter than the retention time, any accelerated temperature stress tests (such as baking) are performed, it is recommended to read the pre-set data first and to re-write it after the test. Access to un-used address locations is not functionally guaranteed.
Refer to section-Ⅵ 8.3 for EEPROM map.

3. Digital Input /Output DC Characteristics

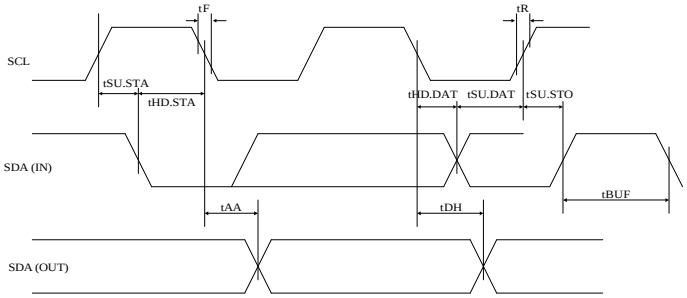
Item	Symbol	min	max	Unit	Conditions
Input High Level	VIH	2.0		V	Note 1
Input Low Level	VIL		0.8	V	
Output High Level	VOH	0.9VDD		V	IOH = -0.2mA
Output Low Level	VOL		0.4	V	IOL = 1mA (Note 2) IOL = 0.2mA (Note 3)
Input Leakage Current 1	IL1		10	uA	except WP pin
Input Leakage Current 2	IL2		350	uA	WP pin

Note 1: except DATAP, DATAN, CLKP and CLKN pins.
Note 2: SDA and TXFAULT pins
Note 3: except SDA and TXFAULT pins

4. I²C™ I/F AC Characteristics

Symbol	Parameter	min	max	Unit	Remark
tSCL	Clock Frequency, SCL		100	kHz	
tLOW	Clock Pulse Width Low	4.7		us	
thigh	Clock Pulse Width High	4.0		us	
tI	Noise Suppression Time		100	ns	
tAA	Clock Low to Data Out Valid	0.1	4.5	us	
tBUF	Time Before a New Transmission	4.7		us	
tHD.STA	Start Hold Time	4.7		us	
tSU.STA	Start Setup Time	4.0		us	
tHD.DAT	Data Hold Time	0		us	
tSU.DAT	Data Setup Time	200		ns	
tR	Input Rise Time		1.0	us	Note 1
tF	Input Fall Time		0.3	us	Note 1
tSU.STO	Stop Setup Time	4.7		us	
tDH	SDATA Hold Time	100		ns	
tWR	Write Cycle Time		10	ms	

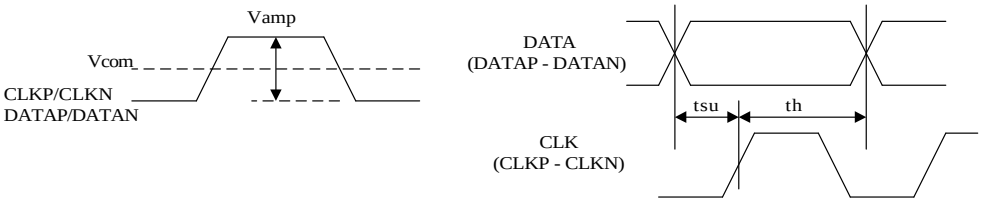
Note 1: This parameter is characterized and is not 100% tested.



5. LVPECL I/F

Item	Symbol	min	typ	max	Unit	Remarks
Single-ended Input Voltage Swing	Vamp	0.1		1.2	V	
Common Voltage	Vcom	0.5*VDD		VDD−1.0	V	
BIAS Voltage	Vbias		0.6*VDD		V	
Input Impedance	Zin	10			kΩ	
Set-up Time	tsu	1.5			ns	SEL="H"
Hold Time	th	1.5			ns	Note 1

Note 1: This parameter is characterized and is not 100% tested.



6. I-DAC1

Item	Condition	min	typ	max	Unit	Remark
Resolution			8		bit	
Output Current with Full Code 1	IMOD=1.3V	76	85	94	mA	RE_DAC1_GAIN=1
Output Current with Full Code 2	IMOD=1.3V	38	43	50	mA	RE_DAC1_GAIN=0
Current Supply with Shutdown	IMOD=VDD			100	uA	TXDISx="H"
1 LSB Current Step 1	IMOD=1.3V		0.333		mA	RE_DAC1_GAIN=1
1 LSB Current Step 2	IMOD=1.3V		0.169		mA	RE_DAC1_GAIN=0
DNL	IMOD=1.3V	-1		+1	LSB	Code 20h to FFh

7. I-DAC2

Item	Condition	min	typ	max	Unit	Remark
Resolution			8		bit	
Output Current with Full Code 1	IMOD=1.3V	48	54	60	mA	RE_DAC2_GAIN=1
Output Current with Full Code 2	IMOD=1.3V	24	27	30	mA	RE_DAC2_GAIN=0
Current Supply with Shutdown	IMOD=VDD			100	uA	TXDISx="H"
1 LSB Current Step 1	IMOD=1.3V		0.212		mA	RE_DAC2_GAIN=1
1 LSB Current Step 2	IMOD=1.3V		0.106		mA	RE_DAC2_GAIN=0
DNL	IMOD=1.3V	-1		+1	LSB	Code 20h to FFh

8. Duty Cycle Adjustment

Item	min	typ	max	Unit	Remarks
Maximum Pulse Extended	0.5			ns	Note 1
1 LSB Pulse Extended Step		0.03		ns	32 Steps
Pulse Extended Stability			0.2	ns	Ta=-40 to 85°C, VDDDR=3.1~3.5V, 0.3ns Extended (Note 1)

Note 1: This parameter is characterized and is not 100% tested.

9. Current Monitor

Item	Condition	min	typ	max	Unit	Remark
MODMON to I-DAC1 Gain	MODMON=1.3V Full Code	0.008	0.0095	0.011	A/A	
BIASMON to I-DAC2 Gain	BIASMON=1.3V Full Code	0.008	0.0095	0.011	A/A	

10. PDGAIN

Item	条件	min	typ	max	Unit	Remark
PDIN Input Range	PDMON=1V±10%	0.08		2.5	V	
PDGAIN Gain Error	PDIN→PDMON	-0.5		+0.5	dB	

11. DACAPC

Item	Condition	min	typ	max	Unit	Remark
Maximum Output Voltage	Test Mode	1.135	1.195	1.255	V	
Minimum Output Voltage	Test Mode	0.752	0.792	0.832		
DNL	Test Mode	-1		+1	LSB	

12. BIASGEN

Item	Condition	min	typ	max	Unit	Remark
BIAS pin Voltage			1.2		V	

13. Temperature Sensor

Item	Condition	min	typ	max	Unit	Remark
Voltage Slope	TEMPMON Voltage	-12.14	-11.56	-10.98	mV/℃	Note-1
Offset Adjustment Target	Ta = 35℃		1.215		V	

Note 1: This parameter is characterized and is not 100% tested.

14. ADC

Item	Condition	min	typ	max	Unit	Remark
Resolution			7		bit	
Maximum Input Voltage		2.09	2.2	2.31	V	
Minimum Input Voltage			0		V	
DNL		-1/2		+1/2	LSB	

15. Power On Reset

Item	Condition	min	typ	max	Unit	Remark
Detect Voltage		2.3	2.5	2.7	V	

16. On-chip Oscillator

Item	Condition	min	typ	max	Unit	Remark
Clock Frequency	Test Mode		2.15		MHz	

17. OPTALM Detect Level

項目	Condition	min	typ	max	Unit	Remark
OPTALM Detect Level	1/3 Setting, PDGAIN=0dB	1/3.2	1/3	1/2.8		
	1/4 Setting, PDGAIN=0dB	1/4.3	1/4	1/3.7		
	1/6 Setting, PDGAIN=0dB	1/6.4	1/6	1/5.6		
	1/7 Setting, PDGAIN=0dB	1/7.5	1/7	1/6.5		

18. TXDIS Release Time

Item	Condition	min	typ	max	Unit	Remark
TXDIS Release Time				500	us	Note 1

Note 1: This parameter is characterized and is not 100% tested.

V. Package Information

(1) Package Type: 48 pin BCC++

(2) Marking Information:

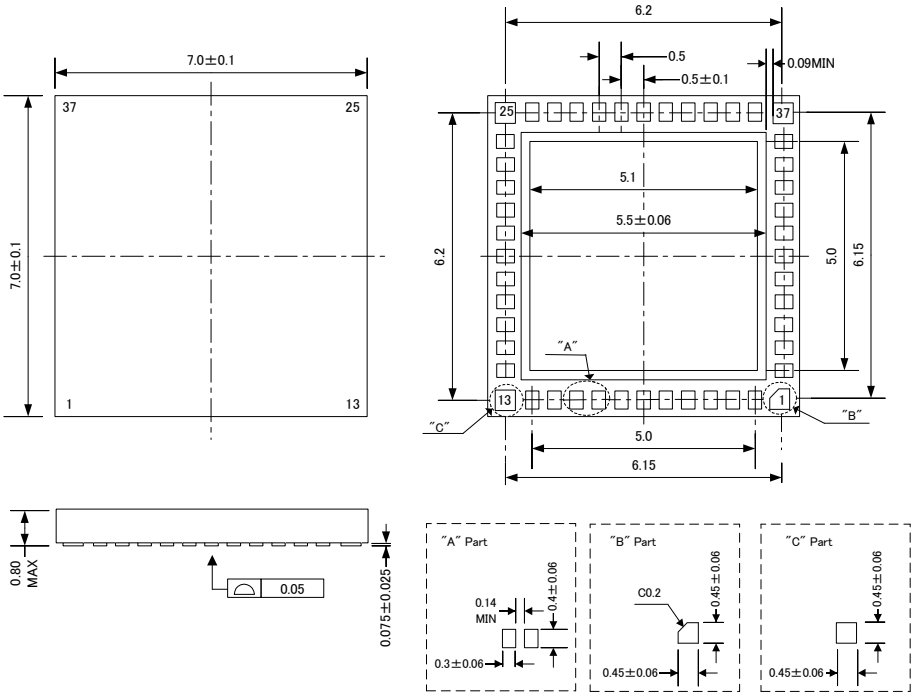
(a) PIN#1 Indication: ○

(b) Logo: AKM

(c) Marking Code: AK2573AVB

(d) Date Code: YYWWXXX (7 digit)

(3) Package Outline



VI. Circuit Description

1. Parameter Notation

1.1 Parameter Definition

In the AK2573A Circuit Description, in order to distinguish various pre-set parameter sources from EEPROM, Registers or Device pins, "Identifier - Main name" notation is used as shown in Table 1-1. For ease of operational description, small letters sometimes expresses internal signals.

Table 1-1 Parameter Definitions

	Identifier	Main Name	Remark	Example
Register	R_	REGISTER name (All Capital)	Indicates register	R_APC_FB R_DAC1
EEPROM	E_	EEPROM name (All Capital))	Indicates EEPROM	E_PDGAIN E_DAC1_FF_TC
Ether or both Register or /and EEPROM	RE_	REGISTER / EEPROM name (All Capital)	Indicates either register or EEPROM	RE_DAC1_GAIN RE_APC_TRGT
PIN	P_	PIN name (All Capital)		P_PDMON
BLOCK	None	BLOCK name (All Capital))		I-DAC1 APC_COMP
Internal Node	None	signal name (small letter)		vpd

1.2 Operation Overview

The AK2573A has 3 primary functions; 125M / 156M Laser diode driver part, APC (Automatic Power Control) part which supplies adequate bias current and modulation current to a Laser Diode, and the Control part to control operation modes of the AK2573A operation.

There are 3 operation modes in the AK2573A. Since each adjusting function is controlled through I²C™ Interface, it realizes an automatic parameter adjustment.

(1) Self-running Mode

Self-running mode is ready for normal operation after all adjustments are completed. In this mode, temperature detection, EEPROM access and feeding current are automatically performed using the on-chip oscillator. The AK2573A works in this mode after power-on.

(2) Adjustment Mode

Adjustment mode is designed for training the LD characteristics. The AK2573A operates according to the register settings set through the I²C™ I/F.

(3) EEPROM Mode

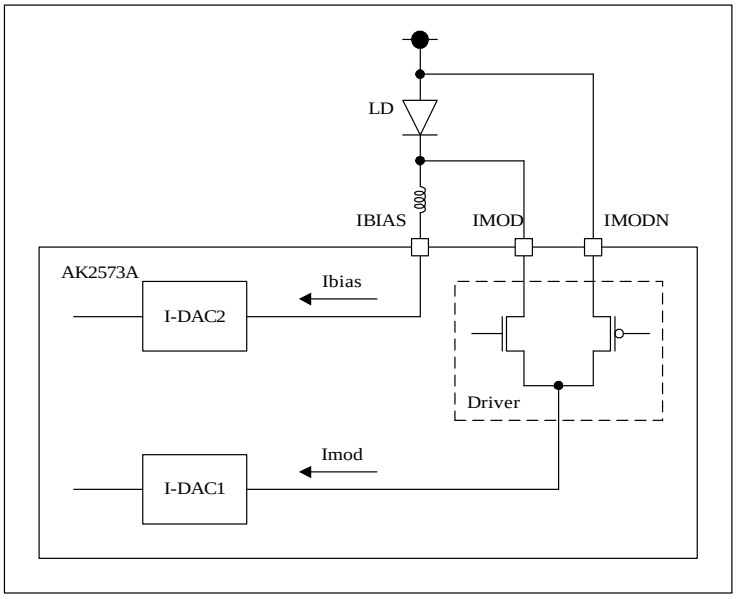
EEPROM mode is used for storing LD characteristics into EEPROM via I²C™ I/F.

2. Driver

Fig 2-1 illustrates the block diagram of the driver function.

AK2573A has two current DACs, I-DAC1 and I-DAC2. I-DAC1 is for modulation current and I-DAC2 is for bias current. Table 1-1 and 1-2 show I-DAC1, I-DAC2 characteristics.

Fig 2-1 Driver Block Diagram



(1) I-DAC1 (Table 2-1)

RE_DAC1_ GAIN	DAC1_GAIN	Output current @ Full code (typ)	Output Current Range (typ)	Current step / LSB (typ)
1	1	85 mA	0 to 85 mA	0.333 mA
0	1/2	43 mA	0 to 43 mA	0.169 mA

(2) I-DAC2 (Table 2-2)

RE_DAC2_ GAIN	DAC2_GAIN	Output current @ Full code (typ)	Output Current Range (typ)	Current step / LSB (typ)
1	1	54 mA	0 to 54 mA	0.212 mA
0	1/2	27 mA	0 to 27 mA	0.106 mA

(3) I-DAC1 / I-DAC2 Common Characteristics

Resolution: 8bit

DNL: +/- 1 LSB@ code = 20h to FFh

3. DATA / CLK I/F (LVPECL)

The AK2573A supports direct data or latched data input (see Table 3-1). Connect CLKP = VSS, and connect CLKN = VDD or leave open when SEL = "L".

Table 3-1 Data input

SEL (CMOS)	
"L"	Direct data
"H"	Latched data with clock

3.1 LVPECL Input (DATAP/DATAN/CLKP/CLKN)

Table 3-2 shows LVPECL input characteristics. The AK2573A LVPECL input, which is biased to 0.6 * VDD with 10kΩ or more inpedance respectively, supports both AC and DC coupling. Fig 3-2 illustrates LVPECL input with AC coupling and Fig3-3 illustrates with DC coupling respectively.

Table 3-2 LVPEL Interface characteristics

Item	Symbol	min	typ	max	Unit	Remarks
Single-ended Input Voltage Swing	| Vamp|	0.1		1.2	V	see Fig 3-1
Common Voltage	Vcom	0.5*VDD		VDD−1.0	V	
BIAS Voltage	Vbias		0.6*VDD		V	see Fig 3-2 and 3-3
Input Impedance	Zin	10			kΩ	
Set-up Time	tsu	1.5			ns	see Fig 3-4
Hold Time	th	1.5			ns	Note 1

Note 1: This parameter is characterized and is not 100% tested.

Fig 3-1 DATA/CLK Input Level

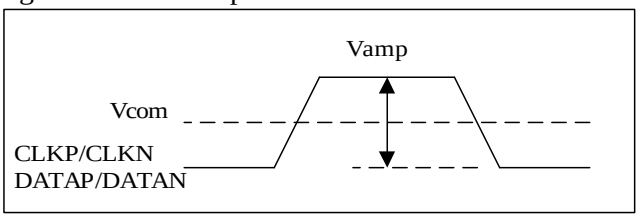


Fig 3-2 LVPECL input with AC coupling

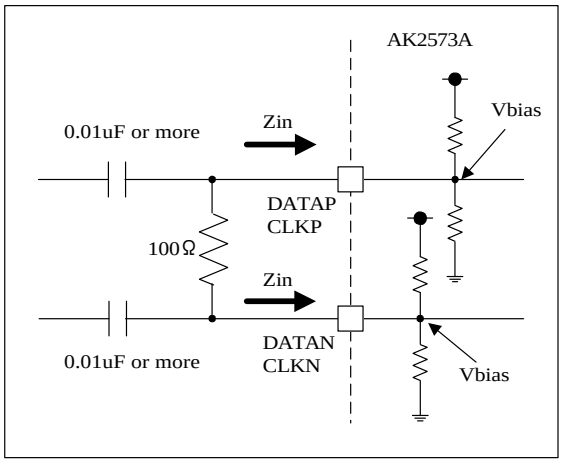


Fig3-3 LVPECL input with DC coupling

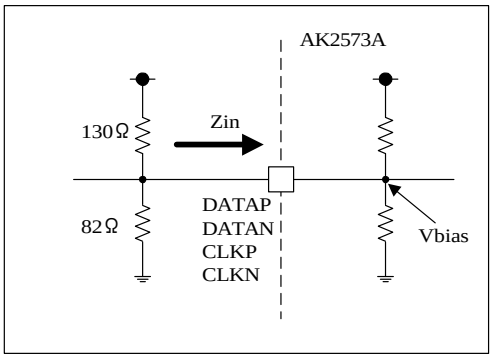
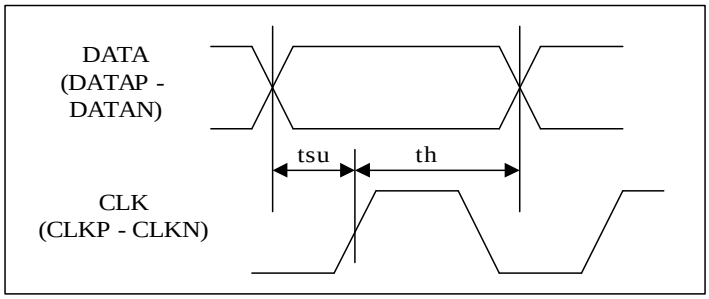


Fig 3-4 Set-up & Hold Time



3.2 Duty Adjustment

AK2573A supplies a programmed duty adjustment in response to the temperature from an on-chip temperature sensor (every 6℃, Duty data is stored in E_DUTY_TC, see Table 8-3 for more information). Write same data into E_DUTY_TC for constant duty adjustment. Table 3-3 and 3-4 show the characteristics of duty adjustment function.

Table 3-3 Duty Adjustment characteristics

Item	Symbol	min	typ	max	Unit	Remarks
Maximum Pulse Extended	Td	0.5			ns	Note 1
1 LSB Pulse Extended Step	Tstep		0.03		ns	32 Steps
Pulse Extended Stability	Tsta			0.2	ns	Ta=-40 to 85℃, VDD=3.1～3.5V, 0.3ns Extended (Note 1)

Note 1: This parameter is characterized and is not 100% tested.

Table 3-4 Pulse Extended

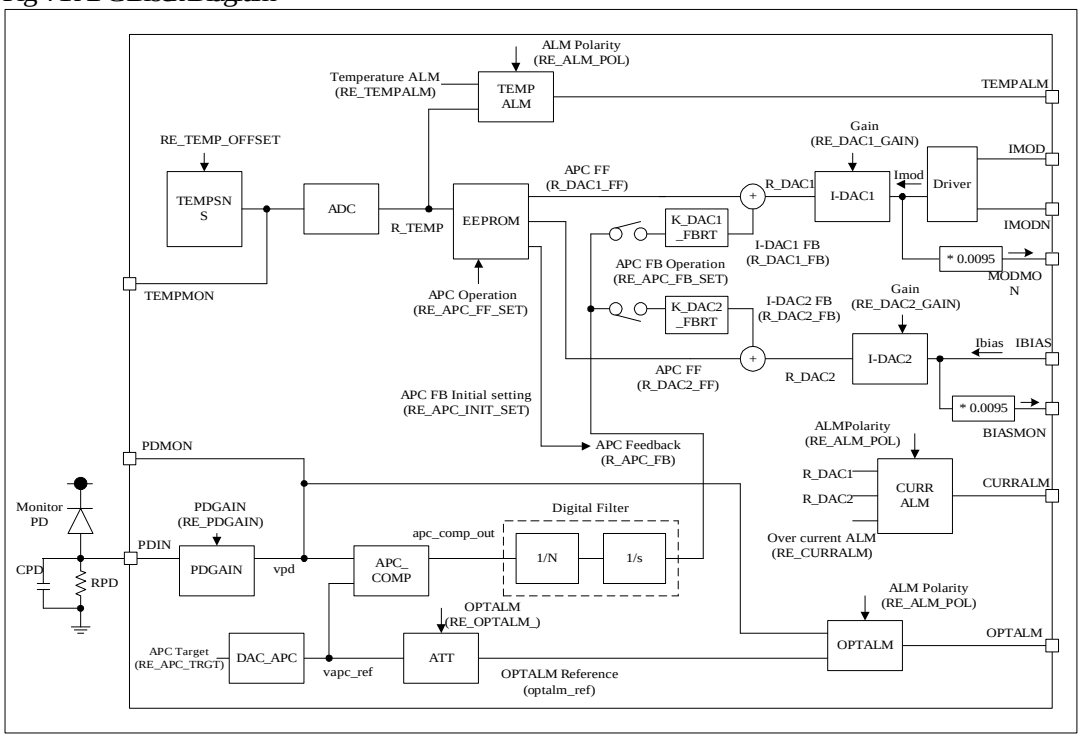
R_DUTY	Pulse Extended (typ) [ns]	Remark
0	0	
1	0.03	
2	0.06	
. .	. .	
30	0.90	
31	0.93	

4. APC

The AK2573A has two APC functions, APC FF (Feed-forward) and APC FB (Feedback).

APC FF supplies a programmed current in response to the temperature from an on-chip temperature sensor. APC_FB provides stable a power control function using a digital feedback algorithm. The APC_FF and APC_FB is user programmable. Fig4-1 illustrates APC block diagram.

Fig 4-1 APC Block Diagram



4.1 APC_FF Function

Fig 4-2 illustrates the APC FF functions. The operation is as follows:

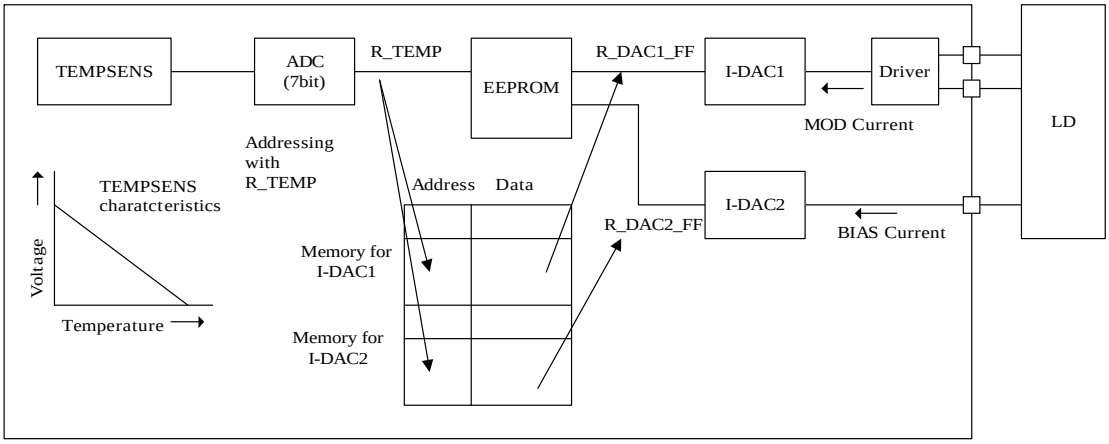
(1) Analog to digital conversion of the voltage (7 bit) that reflects the temperature for every temperature detection period (128ms typ).

(2) Read the 8 bit current data (address is indicated by the ADC data) from EEPROM and set this value to the I-DACs.

If the current data over temperature is set to each EEPROM address, the compensated current is supplied to the LD automatically.

To use this function, current data should be stored in EEPROM in advance. The temperature sensor is cover –40°C to 115°C and EEPROM is prepared with 1.5°C steps.

Fig 4-2 APC FF function



4.2 APC_FB Function

Fig 4-3 shows APC_FB functions. It operates as follows:

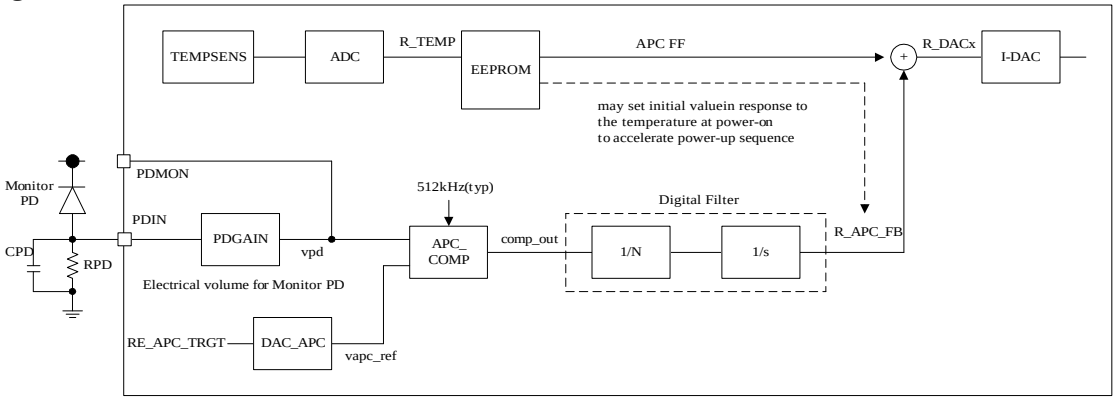
(1) APC_COMP compares vpd and vapc_ref.

(2) The digital filter calculates the compensation current (R_APC_FB) to equalize vpd with vapc_ref to keep LD power constant.

The vapc_ref (RE_APC_TRGT) can be changed over temperature automatically. Temperature compensation procedure is as same as APC FF (data of DAC_APC is read out EEPROM in response to the temperature).

For the stable operation, the cut-off frequency of RPD and CPD should be 1kHz to 10kHz.

Fig 4-3 APC FB function



4.2.1 PDGAIN

PD monitor current is converted to the average voltage with RPD and CPD and input to PDIN. PDIN voltage may be gained at PDGAIN and monitored at PDMON. PDGAIN should be adjusted to PDMON = 1V typ. The gain range of PDGAIN is –8.0dB to 23.5dB with 0.5dB steps (6-bits). PDGAIN is set via the I²C™ interface. Table 4-1 shows PDIN input range and Table 4-2 shows the relationship between PDGAIN and EEPROM setting.

Table 4-1 PDIN input range

Parameter	min	max	Remark
PDIN Input range	0.08V	2.5V	

Table 4-2 PDGAIN

RE_PDGAIN_SET	Gain (typ) [dB]	Remark
000000 (0)	23.5	0.5dB step
000001 (1)	23.0	
:	:	
111110 (62)	-7.5	
111111 (63)	-8.0	

4.2.2 DACAPC

DACAPC generates the reference voltage of APC (vapc_ref). AK2573A supplies a programmed APC reference in response to the temperature from an on-chip temperature sensor (every 6℃, APC reference data is stored in E_APC_TRGT_TC, see Table 8-3 for more information). Write same data into E_APC_TRGT_TC for constant APC reference. Table 4-3 shows the relationship between APC reference voltage (vapc_ref) and EEPROM setting.

Table 4-3 DACAPC

E_APC_TRGT_TC (R_APC_TRGT)	DACAPC (vapc_ref) (typ) [V]	Remark
00000(0)	0.792	13mV step
:		
01111 (15)	0.987	
10000 (16)	1.0	
10001 (17)	1.013	
:		
11111 (31)	1.195	

4.2.3 Example of APC Setting

Table 4-4 shows the typical setting of APC function (APC_FF and APC_FB). The combination of APC is set by RE_APC_FF and RE_APC_FB. Fig 4-5 shows the EEPROM area for MOD current (E_DAC1_TC) and BIAS current (E_DAC2_TC). The data should be stored in E_DAC1_TC and E_DAC2_TC is determined by RE_APC_FF and RE_APC_FB. Table 4-7 and 4-8 shows all combination of APC function.

RE_APC_FF is 2bit data to be assigned I-DAC for APC_FF operation. MSB is for I-DAC2 and LSB for I-DAC1.

RE_APC_FB is 2bit data to be assigned I-DAC for APC_FB operation. MSB is for I-DAC2 and LSB for I-DAC1.

In the case of RE_APC_FB=11(binary), AK2573A is in "Dual Feedback" (see Fig 4-9, 4-10 and Table 4-6).

Table 4-4 Example of APC FF and APC FB combination

RE_APC_FF_SET	RE_APC_FB_SET	BIAS (I-DAC2)	MOD (I-DAC1)	Remarks	Reference
01	10	FB	FF	The initial value of APC FB according to the temperature can be set to accelerate power up time.	Fig 4-4
10	01	FF	FB	The initial value of APC FB according to the temperature can be set to accelerate power up time.	Fig 4-5
11	00	FF	FF	Both BIAS and MOD current are detrmined by APC_FF. APC_FB is not work.	Fig 4-6
11	01	FF	FF+FB	Both BIAS and MOD current are detrmined by APC_FF. APC_FB is set to MOD for LD aging.	Fig 4-7
11	10	FF+FB	FF	Both BIAS and MOD current are detrmined by APC_FF. APC_FB is set to BIAS for LD aging.	Fig 4-8
01	11	FB	FF+FB	Dual Feedback function. BIAS current is determined by APC_FB. MOD current is determined by APC_FF and APC_FB. The initial value of APC_FB according to the temperature can be set to accelerate power up time.	Fig 4-9
10	11	FF+FB	FB	Dual Feedback function. MOD current is determined by APC_FB. BIAS current is determined by APC_FF and APC_FB. The initial value of APC_FB according to the temperature can be set to accelerate power up time.	Fig 4-10
00	11	-	-	Prohibit	
11	11	-	-	Prohibit	

RE_APC_FF_SET (Register or EEPROM) is composed of 2-bits. MSB shows BIAS (I-DAC2) and LSB shows MOD (I-DAC1), and "1" indicates APC Feed-forward function is selected.
RE_APC_FB_SET (Register or EEPROM) is composed of 2-bits. MSB shows BIAS (I-DAC2) and LSB shows MOD (I-DAC2), and "1" indicates APC Feedback function is selected.

Fig 4-4 APC example-1 (MOD=FF, BIAS=FB)

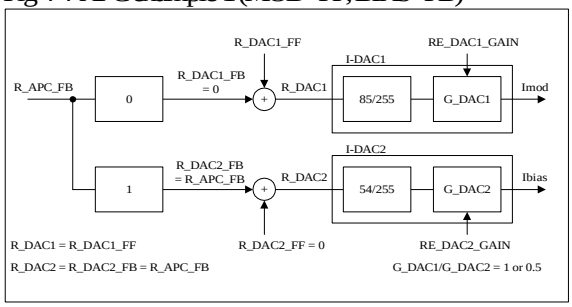


Fig 4-5 APC example-2 (MOD=FB, BIAS=FF)

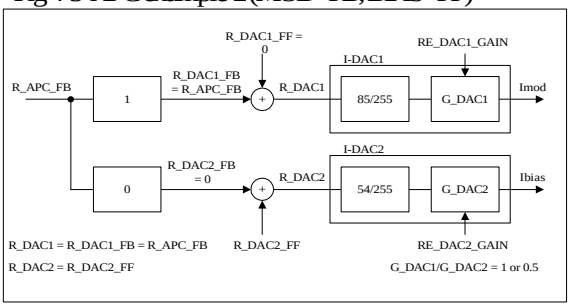


Fig 4-6 APC example-3 (MOD=FF, BIAS=FF)

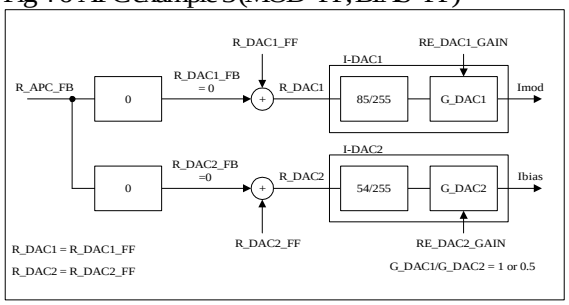


Fig 4-7 APC example-4 (MOD=FF+FB, BIAS=FF)

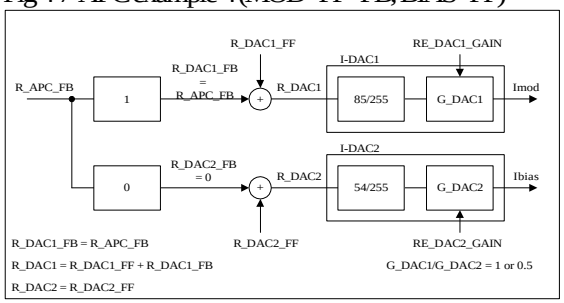


Fig 4-8 APC example-5 (MOD=FF, BIAS=FF+FB)

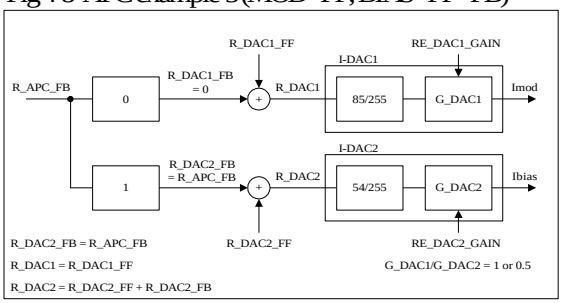


Fig 4-9 APC example-6 (MOD=FF+FB, BIAS=FB)

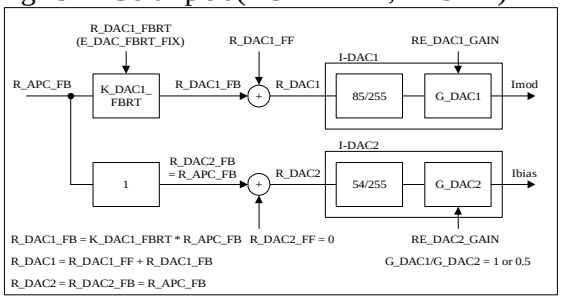


Fig 4-10 APC example-7 (MOD=FB, BIAS=FF+FB)

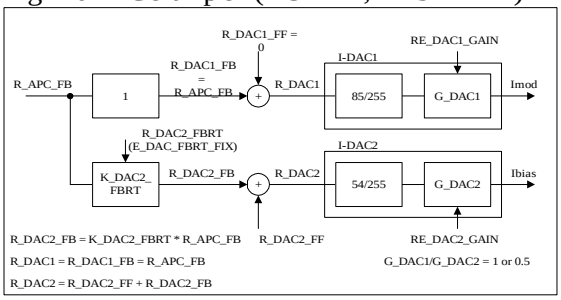


Table 4-5 EEPROM Assignments for typical operation

RE_APC_ FF_SET	RE_APC_ FB_SET	RE_APC_ INIT_SET	E_DAC2_TC	E_DAC1_TC	I-DAC2 (BIAS)	I-DAC1 (MOD)
01	10	0	-	E_DAC1_FF_TC	FB	FF
		1	E_APC_INIT_TC	E_DAC1_FF_TC	FB	FF
10	01	0	E_DAC2_FF_TC	-	FF	FB
		1	E_DAC2_FF_TC	E_APC_INIT_TC	FF	FB
11	00	x	E_DAC2_FF_TC	E_DAC1_FF_TC	FF	FF
11	01	x	E_DAC2_FF_TC	E_DAC1_FF_TC	FF	FF+FB
11	10	x	E_DAC2_FF_TC	E_DAC1_FF_TC	FF+FB	FF
01	11	0	-	E_DAC1_FF_TC	FB	FF+FB
01	11	1	E_APC_INIT_TC	E_DAC1_FF_TC	FB	FF+FB
10	11	0	E_DAC2_FF_TC	-	FF+FB	FB
10	11	1	E_DAC2_FF_TC	E_APC_INIT_TC	FF+FB	FB
00	11	x	Prohibit			
11	11	x				

E_DAC1_FF_TC: I-DAC1 current data (temperature compensated)

E_DAC2_FF_TC: I-DAC2 current data (temperature compensated)

E_APC_INIT_TC: R_APC_FB initial data (temperature compensated)

Table 4-6 APC FB Operation

RE_APC_ FB_SET	RE_APC_ FF_SET	K_DAC1_FBRT	K_DAC2_FBRT	Remark
00	XX	0	0	No FB
01	XX	1	0	FB for MOD
10	XX	0	1	FB for BIAS
11	00	-	-	Prohibit
	01	R_DAC1_FBRT*1.25/64/G_DAC1	1	R_DAC1_FBRT=E_DAC_FBRT
	10	1	R_DAC2_FBRT/32/G_DAC2	R_DAC2_FBRT=E_DAC_FBRT
	11	-	-	Prohibit

Table 4-7 APC and EEPROM assignment (Self-running mode)

RE_APC_FB_SET	RE_APC_FF_SET	RE_APC_INIT_SET	R_DAC1_FF	R_DAC2_FF	R_APC_FB	Initial setting R_APC_FB	K_DAC1_FBRT	K_DAC2_FBRT	MOD (R_DAC1)	BIAS (R_DAC2)	E_DAC1_TC	E_DAC2_TC	Remarks
00	00	X	0	0	0	0	0	0	0	0	-		
	01	X	E_DAC1_TC	0	0	0	0	0	FF	0	FF	-	
	10	X	0	E_DAC2_TC	0	0	0	0	0	FF	-	FF	
	11	X	E_DAC1_TC	E_DAC2_TC	0	0	0	0	FF	FF	FF	FF	
01	00	0	0	0	FB	0	1	0	FB	0	-	-	
	00	1	0	0	FB	E_DAC1_TC	1	0	FB	0	FB_INIT	-	
	01	X	E_DAC1_TC	0	FB	0	1	0	FF+FB	0	FF	-	
	10	0	0	E_DAC2_TC	FB	0	1	0	FB	FF	-	FF	
	10	1	0	E_DAC2_TC	FB	E_DAC1_TC	1	0	FB	FF	FB_INIT	FF	
	11	X	E_DAC1_TC	E_DAC2_TC	FB	0	1	0	FF+FB	FF	FF	FF	
10	00	0	0	0	FB	0	0	1	0	FB	-	-	
	00	1	0	0	FB	E_DAC2_TC	0	1	0	FB	-	FB_INIT	
	01	0	E_DAC1_TC	0	FB	0	0	1	FF	FB	FF	-	
	01	1	E_DAC1_TC	0	FB	E_DAC2_TC	0	1	FF	FB	FF	FB_INIT	
	10	X	0	E_DAC2_TC	FB	0	0	1	0	FF+FB	-	FF	
	11	X	E_DAC1_TC	E_DAC2_TC	FB	0	0	1	FF	FF+FB	FF	FF	
11	00	X	-	-	-	-	-	-	-	-	-	-	Prohibit
	01	0	E_DAC1_TC	0	FB	0	See Table 4-6	1	FF+FB	FB	FF	-	
	01	1	E_DAC1_TC	0	FB	E_DAC2_TC	See Table 4-6	1	FF+FB	FB	FF	FB_INIT	
	10	0	0	E_DAC2_TC	FB	0	1	See Table 4-6	FB	FF+FB	-	FF	
	10	1	0	E_DAC2_TC	FB	E_DAC1_TC	1	See Table 4-6	FB	FF+FB	FB_INIT	FF	
	11	X	-	-	-	-	-	-	-	-	-	-	Prohibit

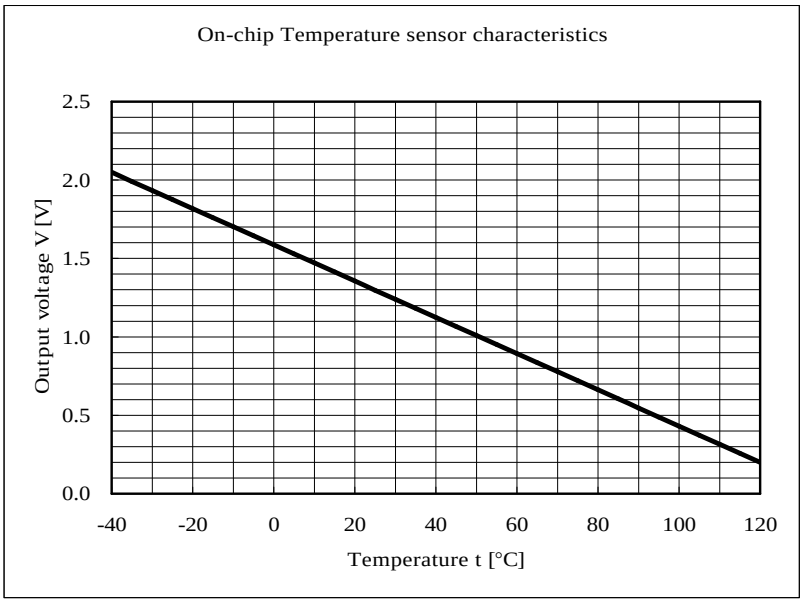
Table 4-8 APC and EEPROM assignment (Adjustment mode)

RE_APC_FB_SET	RE_APC_FF_SET	RE_APC_INIT_SET	R_DAC1_FF	R_DAC2_FF	R_APC_FB	R_DAC1_FBRT	R_DAC2_FBRT	K_DAC1_FBRT	K_DAC2_FBRT	MOD (R_DAC1)	BIAS (R_DAC2)	Remarks
00	XX	X	I/F	I/F	0	N/A	N/A	0	0	FF	FF	
01	XX	X	0	I/F	FB	N/A	N/A	1	0	FB	FF	
10	XX	X	I/F	0	FB	N/A	N/A	0	1	FF	FB	
11	00	X	-	-	-	-	-	-	-	-	-	Prohibit
	01	X	I/F	0	FB	I/F	N/A	See Table 4-6	1	FF+FB	FB	
	10	X	0	I/F	FB	N/A	I/F	1	See Table 4-6	FB	FF+FB	
	11	X	-	-	-	-	-	-	-	-	-	Prohibit

4.3 Temperature Sensor (TEMPSENS)

Fig 4-11 shows an on-chip temperature sensor characteristics and Table 4-9 shows the relationship between detected temperature and ADC code.

Fig 4-11 On-chip Temperature Sensor Characteristics



(1) Slope: -11.56mV/°C (typ)
(2) V(t) = -0.01156 * t + 1.62 [V] (typ)
(3) AD_code = int(V(t) / 2.2 * 127 +0.5) = int(-0.667*t + 94.0)
(4) Temperature step @ AD_code=1LSB: 1.49°C/LSB

*Temperature sensor detects the junction temperature, not LD or ambient temperature.

Table 4-9 AD code and detected temperature [typ]

AD code	Temp [℃]	AD code	Temp [℃]	AD code	Temp [℃]	AD code	Temp [℃]
0	140.1	32	92.2	64	44.2	96	-3.7
1	138.6	33	90.7	65	42.7	97	-5.2
2	137.1	34	89.2	66	41.2	98	-6.7
3	135.6	35	87.7	67	39.7	99	-8.2
4	134.1	36	86.2	68	38.2	100	-9.7
5	132.6	37	84.7	69	36.7	101	-11.2
6	131.1	38	83.2	70	35.2	102	-12.7
7	129.6	39	81.7	71	33.7	103	-14.2
8	128.2	40	80.2	72	32.2	104	-15.7
9	126.7	41	78.7	73	30.7	105	-17.2
10	125.2	42	77.2	74	29.2	106	-18.7
11	123.7	43	75.7	75	27.7	107	-20.2
12	122.2	44	74.2	76	26.3	108	-21.7
13	120.7	45	72.7	77	24.8	109	-23.2
14	119.2	46	71.2	78	23.3	110	-24.7
15	117.7	47	69.7	79	21.8	111	-26.2
16	116.2	48	68.2	80	20.3	112	-27.7
17	114.7	49	66.7	81	18.8	113	-29.2
18	113.2	50	65.2	82	17.3	114	-30.7
19	111.7	51	63.7	83	15.8	115	-32.2
20	110.2	52	62.2	84	14.3	116	-33.7
21	108.7	53	60.7	85	12.8	117	-35.2
22	107.2	54	59.2	86	11.3	118	-36.7
23	105.7	55	57.7	87	9.8	119	-38.2
24	104.2	56	56.2	88	8.3	120	-39.7
25	102.7	57	54.7	89	6.8	121	-41.2
26	101.2	58	53.2	90	5.3	122	-42.7
27	99.7	59	51.7	91	3.8	123	-44.2
28	98.2	60	50.2	92	2.3	124	-45.7
29	96.7	61	48.7	93	0.8	125	-47.2
30	95.2	62	47.2	94	-0.7	126	-48.7
31	93.7	63	45.7	95	-2.2	127	-50.2

4.4 Current Monitor

AK2573A has MOD current and BIAS current monitor, MODMON and BIASMON respectively. MODMON is 0.0095 times of I-DAC1 output (source type) and BIASMON is 0.0095 times of I-DAC2 output (source type).

5. Alarm

AK2573A has 5 alarm functions as shown in Table 5-1.

Table 5-1 Alarm function

ALM	Detection condition	Polarity	Detected Time
OPTALM	When monitor PD current is below the OPTALM level.	Programmable	5us (typ) (Note 1)
CURRALM	When R_DAC1 or R_DAC2 is beyond CURRALM level or equal to full code.	Programmable	every 125us (typ)
TEMPALM	When the detected temperature is beyond TEMPALM level.	Programmable	every 128ms (typ)
DATAALM	When the detected 0s or 1s sequential data input (4.5us typical).	Programmable	4.5us (typ)
TXFAULT	When one or more alarm detected.	"H"	depends on detected ALM

Note 1: Not include delay time by RPD and CPD.

5.1 OPTALM

OPTALM level (optalm_ref) is selectable among 1/3, 1/4, 1/6 and 1/7 of APC FB reference voltage (vapc_ref) by RE_OPTALM.

OPTALM is detected when vpd < optalm_ref.

APC FB keeps R_APC_FB during OPTALM detection in the "Self running mode".

5.2 CURRALM

CURRALM is detected when

R_DAC1(MSB 4bit) > R_CURRALM_DAC1 or R_DAC2(MSB 4bit) > R_CURRALM_DAC2

R_CURRALM_DAC1 and 2 can be set every 6°C.

CURRALM is clear when receiving disable request (TX_DIS1 or TX_DIS2 is set "H").

5.3 TEMPALM

TEMPALM is detected when R_TEMP < R_TEMPALM.

R_TEMP has negative slope compared to the temperature, TEMPALM is detected when the detected temperature beyond R_TEMPALM.

5.4 DATAALM

DATAALM is detected when input DATA is 0's or 1's fixed more than 4.5us (typ).

APC FB keeps R_APC_FB during DATAALM detection in the "Self running mode".

DATAALM detection is ignored when RE_DATAALM_MASK= "1".

5.5 TXFAULT

TXFAULT function is shown in Table 5-2.

Table 5-2 TXFAULT

RE_SFP	Shutdown request (TXDIS 1, 2)	ORed ALM	TXFAULT	I-DAC output
0	0	0	0	Normal Operation
0	0	1	1	Normal Operation
0	1	X	ORed ALM	Shutdown
1	0	0	0	Normal Operation
1	0	1	1 (Hold)	Shutdown
1	1	X	0 or 1 (Hold)	Shutdown

RE_SFP = 0 operation

Set "H" when OPTALM, CURRALM, TEMPALM or DATAALM is detected

Set "L" when no ALM detected.

RE_SFP=1 operation

Support TX_FAULT of the SFP (Small Form-factor Pluggable) requirement.

Set and hold "H" when detected OPTALM, CURRALM, TEMPALM or DATAALM and go into shutdown mode.

Reset to "L" when TXDIS1 or TXDIS2 is "H"→"L". Refer to "6. Shutdown" for more information.

During "Adjustment mode", TXFAULT detection is ignored.

6. Shutdown

6.1 Shutdown Operation

Fig 6-1 shows the shutdown operation. The AK2573A supports the SFP (Small Form-factor Pluggable) requirement.

Fig 6-1 Shutdown Operation

TXDIS1	TXDIS2	RE_SFP	TXFAULT	Operation	Remarks
1	X	X	X	Shutdown	Shutdown with pin
X	1	X	X	Shutdown	Shutdown with pin
0	0	0	X	Normal Operation	
0	0	1	0	Normal Operation	
0	0	1	1	Shutdown	SFP TXFAULT Operation

Fig 6-2 Shutdown Condition

Function	Operation	Remarks
I-DAC1/2 output	High-Z (0mA output)	
APC_FF	Normal Operation.	
APC_FB	Keep the data at shutdown request.	
ALM	Normal Operation	
TXFAULT	R_SFP=0: Normal Operation R_SFP=1: Keep the data at shutdown request.	

6.2 Temperature Comparison between Shutdown Request and Release

The AK2573A keeps the temperature data at shutdown request and compares it with temperature at release request to avoid over-current conditions at the LD. When the AK2573A detects a temperature difference between at shutdown request and the release request, the APC FB data is set to 0 or to initial values in response to the temperature at the release request. The temperature difference is programmable.

When the AK2573A does not detect a temperature difference, it keeps the APC FB data, resulting in faster operation.

This function works at release request as follows:

if (ABS(R_TEMP_STDW − R_TEMP)) > R_TEMP_WIN)

R_APC_FB = 0 or reset to the initial value in response to the R_TEMP

where, R_TEMP_STDW is a temperature at shutdown request

R_TEMP is a temperature at release request

R_TEMP_WIN is a temperature difference (user programmable)

APC FF continues to operate during shutdown for fast performance when a release request is received. However, the I-DAC current stays at 0mA.

Table 6-3 Operation at shutdown release

RE_SFP	TXFAULT at Shutdown request	RE_TEMP_ DET	Temp Difference result	R_APC_FB	Remark
0	X	0	X	Initial value	
0	X	1	0	Hold data	
0	X	1	1	Initial value	
1	0	0	X	Initial value	
1	0	1	0	Hold data	
1	0	1	1	Initial value	
1	1	X	X	Initial value	

7. Power-up / down Timing

7.1 Delay Time of TXFAULT Detection with OPTALM

In correspond to the delay time caused by RPD and CPD to get the moniter PD average current, the delay time of TXFAULT detection with OPTALM is set when RE_SFP="1" (SFP support). AK2573A has 2 delay time when RE_SFP="1": normal delay and accelerated delay. Accelerated delay may be selected when both I-DAC1 and I-DAC2 are set to APC_FF or APC_FB with an initial value setting.

Table 7-1 shows the delay time of TXFAULT detection with OPTALM and Fig 7-1 illustrated block diagram.

Note: When accelerated delay is selected with RE_SFP="1", APC_FF data or initial data of APC_FB should be suitable, otherwise AK2573A might go into shutdown by detection of OPTALM after delay time.

Fig 7-1 APC_FB Block Diagram

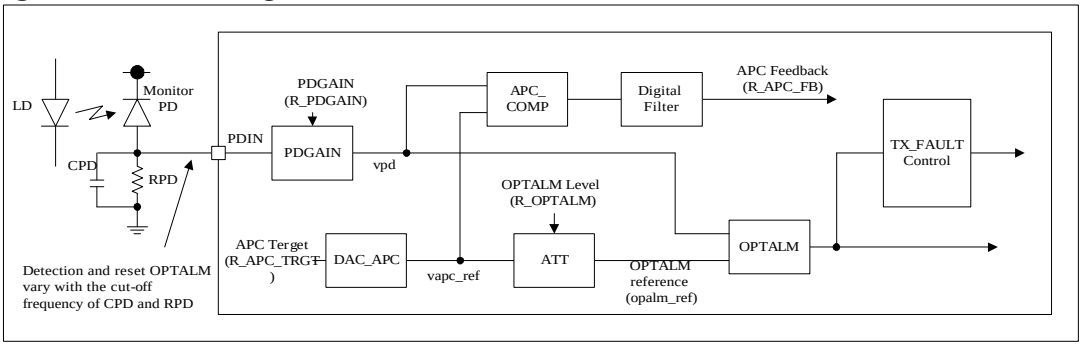
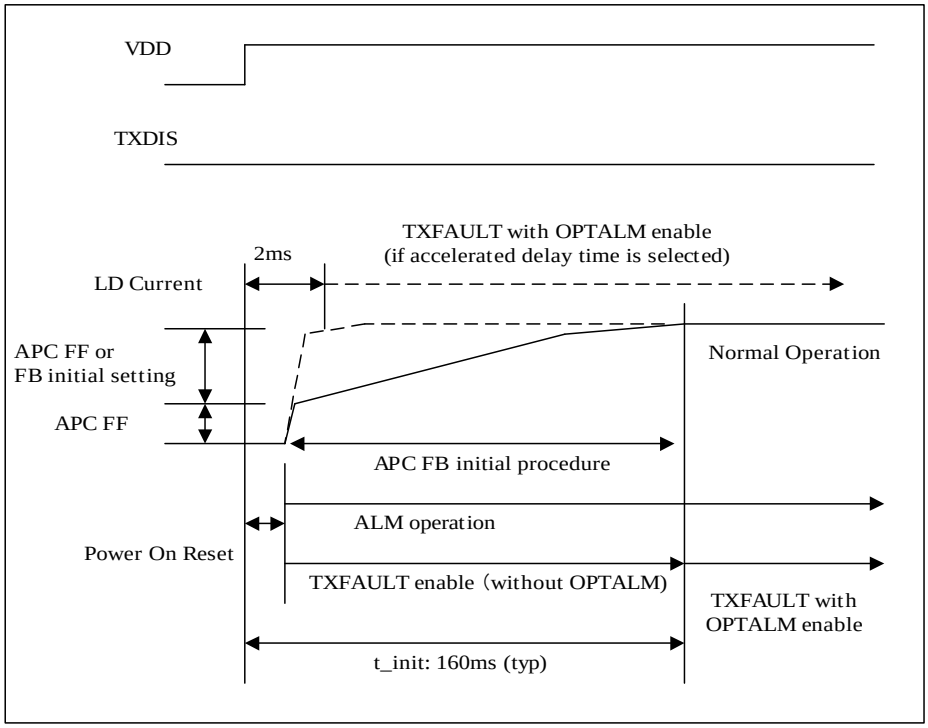


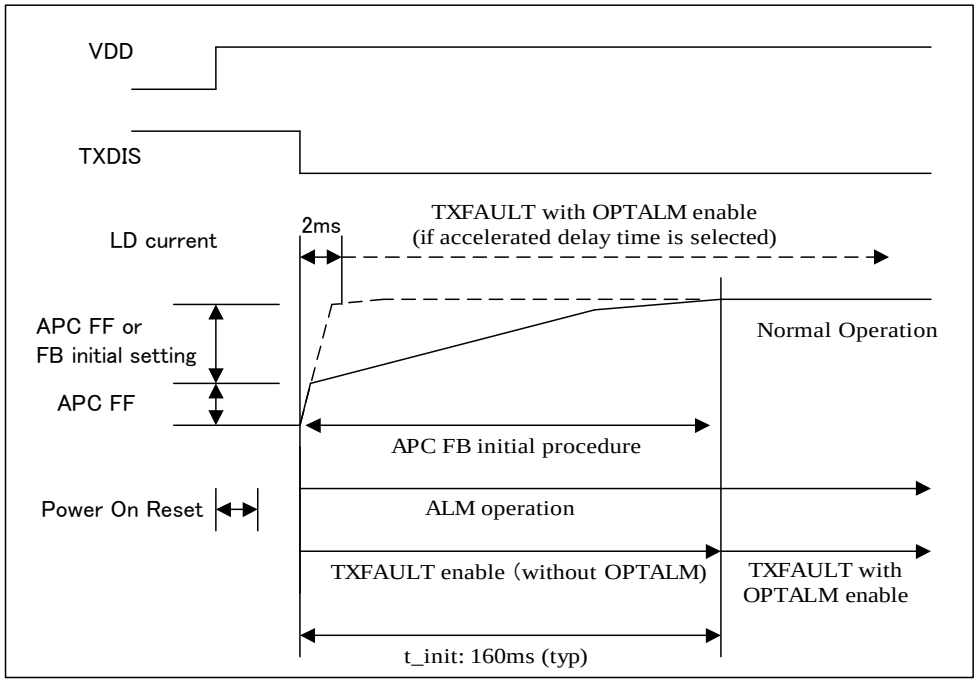
Table 7-1 Delay time of TXFAULT detection with OPTALM

RE_SFP	R_TIMER_ OPTALM	R_APC_ INIT_SET	R_APC_ FF_SET	Delay Time of TXFAULT detection with OPTALM	Remarks
0	X	X	X	0 ms	disable TXFAULT detection
1	0	X	X	160 ms (typ)	
1	1	0	00 01 10	160 ms (typ)	
1	1	X	11	2 ms (typ)	Acceleration power-up
1	1	1	X	2 ms (typ)	

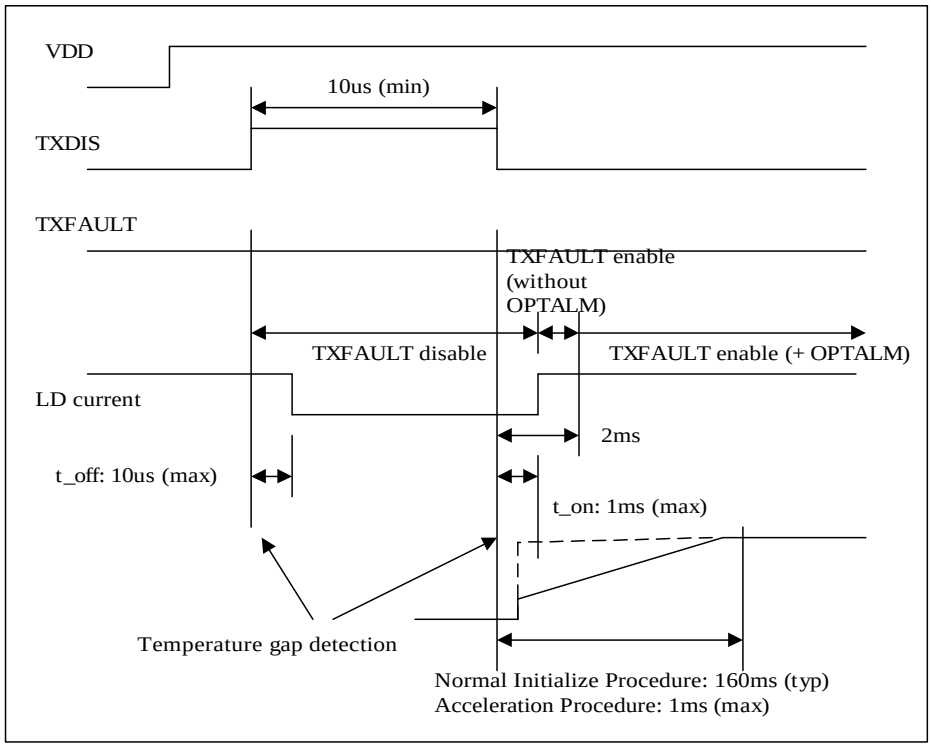
7.2 Power on Initialization Procedure without Shutdown Request (TXDIS=L)



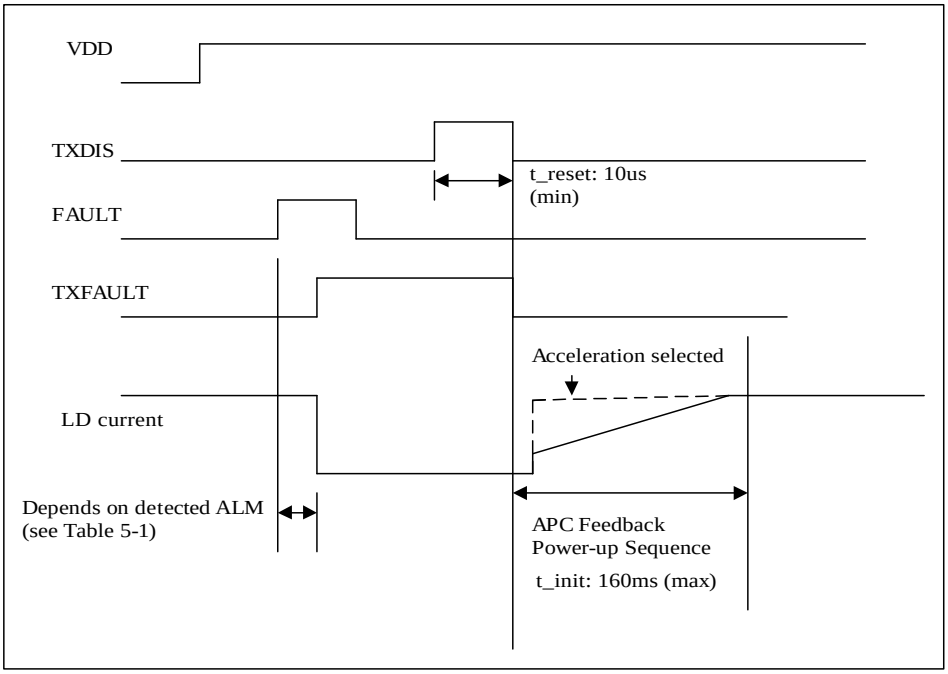
7.3 Power on Initialization Procedure with Sh utdown request (TXDIS=H)



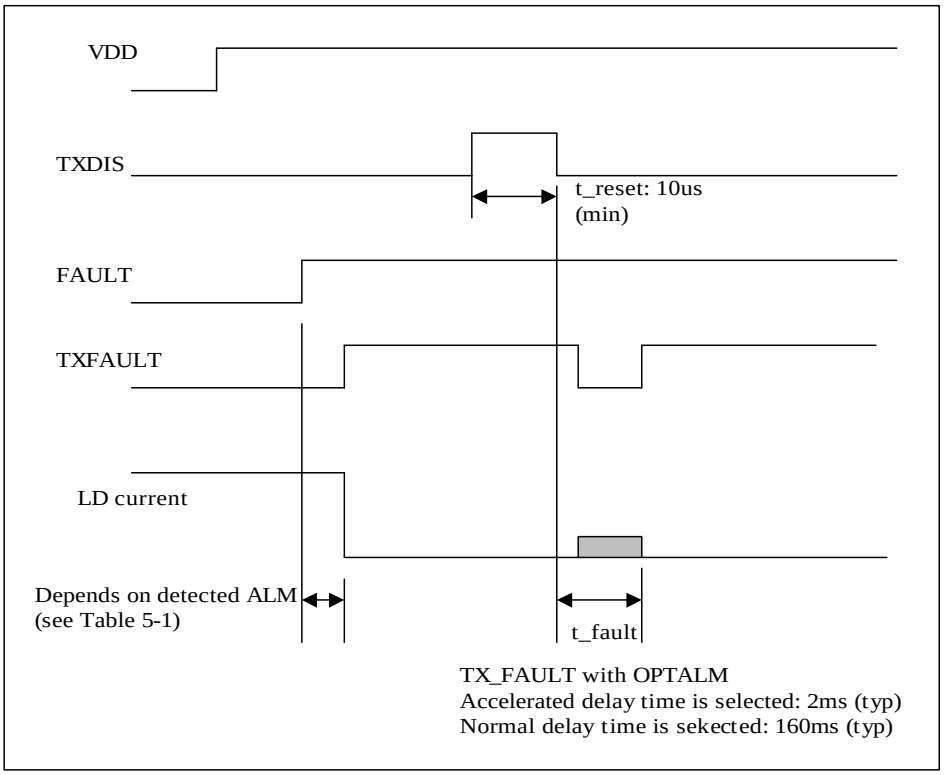
7.4 TXDIS Timing during Normal Operation



7.5 TXFAULT Detection / Reset with Recovery



7.6 TXFAULT Detection / Reset without Recovery



8. I²C™ I/F

8.1 Memory Map

Table 8-1 shows the EEPROM / Register address map. Access to memory (EEPROM / registers) is done via the I²C™ I/F format.

WP (Write Protect) may limit the access of memory as shown in Table 8-2.

Table 8-1 Memory map

Device Address	Device Address-1	Device Address-2	Address	Data
A0h	1010	000	00000000 to 01111111	User Area (EEPROM, 1kbit)
A0h	1010	000	10000000 to 11111111	No memory
A2h	1010	001	00000000 to 11111111	No memory
A4h	1010	010	00000000 to 11111111	Adjustment data (EEPROM, 3kbit)
A6h	1010	011	00000000 to 01111111	
A6h	1010	011	10000000 to 11111111	No memory
A8h	1010	100	00000000 to 00011001	Registers
A8h	1010	100	00011010 to 11111110	No memory
A8h	1010	100	11111111	AK2573A Operation mode change

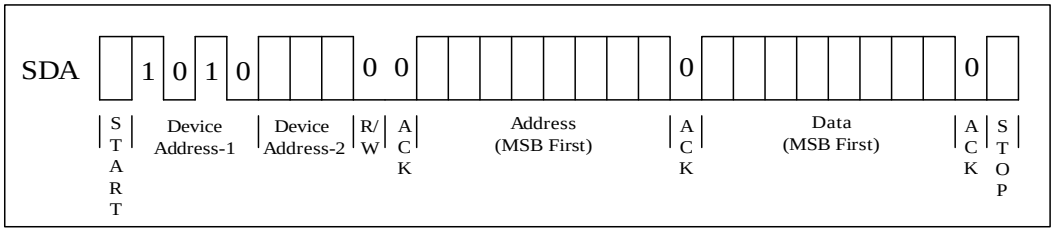
Table 8-2 Memory access limitation with WP

Item	WP = "L"	WP = "H"
Device Address	1010xxx	1010000
ACK (Note 1)	when receive device address	when receive device address
EEPROM / Register Access	Full access	User area only (read only)
Operating mode	Full	Self runnig mode only
Page Write	16 byte (without registers)	-
Sequential Read	from 00000000000 to 01111111111	from 00000000 to 01111111
Registers Access	Random access only	-

Note 1) During EEPROM Write operation, no ACK is generated.

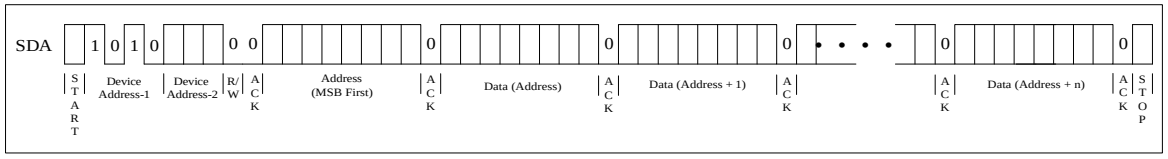
8.2 Read/Write Operation

8.2.1 Byte Write



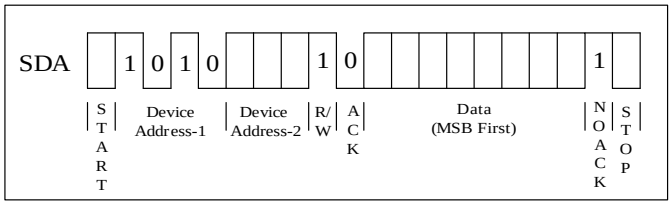
8.2.2 Page Write

AK2573A is capable of 16-byte page write.



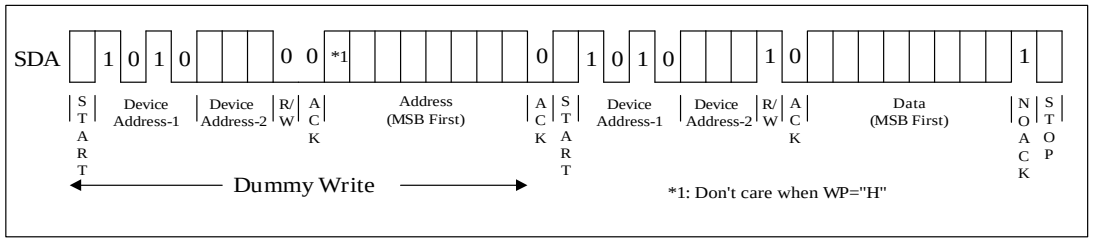
8.2.3 Current Address Read

The internal address counter maintains the last address accessed during the last read or write operation, incremented by one. The roll over address is changed WP setting. Refer to Table 7-2 in detail.



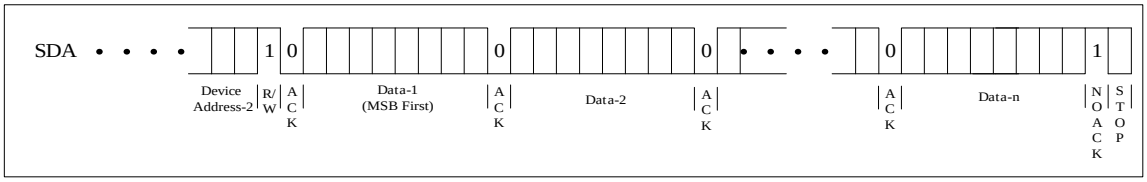
8.2.4 Random Read

A random read requires a "dummy" byte write sequence to specified "Address". After receive the ACK from AK2573A, perform "current address read" (see 8.2.2).



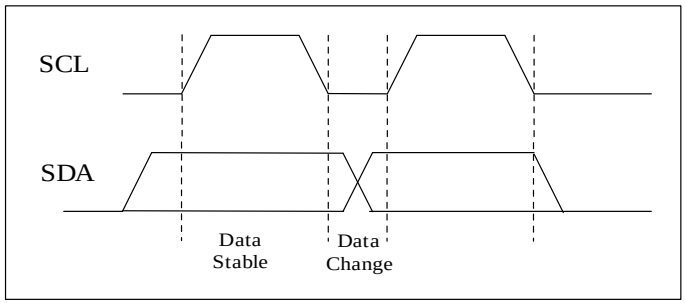
8.2.5 Sequential Read

Sequential read can be initiated as ether "Current Address Read" or "Random Read". After issuing either of them, the AK2573A continues to output data for each ACK received.



8.2.6 Data Change

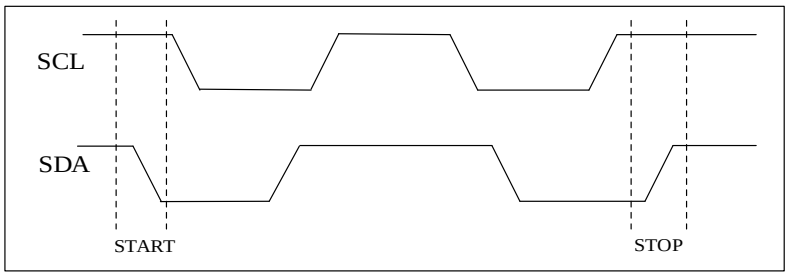
The SDA pin is normally pulled high with 4.7k to 10kΩ. Data on the SDA pin may change only during SCL low time period. Data changes during SCL high periods will indicate a start or stop condition.



8.2.7 Start / Stop Condition

Start Condition: A high-to-low transition of SDA with SCL high is a start condition that must precede any other command.

Stop Condition: A high-to-low transition of SDA with SCL high is a stop condition.



8.3 EEPROM

EEPROM memory map is shown in Table 8-3, 8-4 and 8-5.

EEPROM access is limited with WP pin and Operation mode (refer to Table 9-1, for more information).

WP = "L": Full access

WP = "H": User area only with read only

(Note) The AKM factory adjusted data are stored in advance at address (Device Address2 = 011, Address=60h) for the offset of the on-chip temperature sensor. If such excess temperature stress is to be applied to this device which exceeds a guaranteed EEPROM data retention conditions (for 10 years at 85℃), it is important to read the pre-determined value in advance and to re-write the same data back into EEPROM after an exposure to the excess temperature environment. Even if the exposure time is shorter than the retention time, any accelerated temperature stress tests (such as baking) are performed, it is recommended to read the pre-set data first and to re-write it after the tests.

Table 8-3 EEPROM Address MAP

Device Address	Address	DATA (D7-D0)	Initial Value	Remark
A0h	00h (0) ～ 7Fh (127)	User Area (1kbit)	00h	
A0h	80h (128) ～ FFh (255)	No Memory		
A2h	00h (0) ～ FFh (255)			
A4h	00 h(0) ～ 7F h(127)	E_DAC1_TC Temperature data for I-DAC1 (1kbit)	00h	Addressing with R_TEMP (1.5℃ step)
A4h	80h (128) ～ FFh (255)	E_DAC2_TC Temperature data for I-DAC2 (1kbit)	00h	Addressing with R_TEMP (1.5℃ step)
A6h	00h (0) ～ 1Fh(31)	E_DUTY_TC (5bit) Temperature data for Duty Adjustment (256bit)	00h	Addressing with MSB 5bit of R_TEMP (6℃ step)
A6h	20h (32) ～ 3Fh (63)	E_APC_TRGT_TC (5bit) Temperature data for APC FB reference (R_APC_TARGT) (256bit)	00h	Addressing with MSB 5bit of R_TEMP (6℃ step)
A6h	40h (64) ～ 5Fh (95)	MSB 4bit: E_CURRALM_DAC1_TC LSB 4bit: E_CURRALM_DAC2_TC Temperature data for CURRALM (256bit)	FFh	Addressing with MSB 5bit of R_TEMP (6℃ step)
A6h	60h (96) ～ 7Fh (255)	Adjustment data (256bit)	see Table 8-4 and 8-5	

Table 8-4 Adjustment Data Area (Device Address-2 = 011)

EEPROM	Address	Function	Bit	Initial Value	Remark
E_VRFTRIM[7:4]	60h	Oscillator Frequency	4	Factory Setting	
E_TEMP_OFFSET[3:0]	60h	Temperature sensor offset	4	Factory Setting	
E_APC_FF_SET[7:6]	61h	APC FF Setting	2	00	see Table 4-4
E_APC_FB_SET[5:4]	61h	APC FB Setting	2	00	see Table 4-4
E_APC_INIT_SET[3]	61h	APC FB Initial Setting	1	0	0: No Initial Setting 1: Initial Setting
E_SFP[2]	61h	SFP Setting	1	0	0: No SFP Support 1: SFP Support
E_DAC1_GAIN[1]	61h	I-DAC1 Gain	1	0	0: Gain = 1/2 1: Gain = 1
E_DAC2_GAIN[0]	61h	I-DAC2 Gain	1	0	0: Gain = 1/2 1: Gain = 1
E_TEMP_DET[5]	62h	Temperature compensation at shutdown release ON/OFF	1	1	0: OFF 1: ON
E_TIMER_OPTALM[4]	62h	Delay time of TXFAULT detection with OPTALM	1	0	0: 160ms 1: 2ms
E_ALM_POL[3]	62h	ALM Polarity	1	0	0: "H" 1: "L"
E_OPTALM[1:0]	62h	OPTALM Reference Level	2	00	00: 1/3, 01: 1/4 10: 1/6, 11: 1/7
E_TEMP_WIN[6:0]	63h	Temperature Difference Detection Level	7	00h	see section 6.2
E_DAC_FBRT_FIX[6:0]	65h	APC FB Dual Feedback Ratio	7	00h	see section 4.3
E_DATAALM_MASK[0]	67h	DATAALM mask	1	0	0: DATAALM Valid 1: DATAALM Invalid
E_PDGAIN[5:0]	68h	PDGAIN	6	00h	see Table 4-2
E_TEMPALM[6:0]	6Ch	TEMPALM Level	7	00h	see Table 4-9

Table 8-5 EEPROM Map (Adjustment Data Area)

Address	D7	D6	D5	D4	D3	D2	D1	D0
60h	VREFTRIM				TEMP_OFFSET			
61h	APC_FF_SET		APC_FB_SET		APC_INIT_SET	SFP	DAC1_GAIN	DAC2_GAIN
62h			TEMP_DET	TIMER_OPTALM	ALM_POL		OPTALM	
63h		TEMP_WIN						
64h								
65h		DAC_FBRT_FIX						
66h								
67h								DATAALM_MASK
68h			PDGAIN					
69h								
6Ah								
6Bh								
6Ch		TEMPALM						
6Dh – 7Fh	Reserved (for AKM Test)							

8.4 Register

Register memory map is shown in Table 8-6 and 8-7. Register access is limited with WP pin and Operation mode (refer to Fig 9-1, for more information).

Table 8-6 Register (Device Address = A8h)

Register	Address	Function	Bit	Type	R/W	Remark
R_VRFTRIM[7:4]	00h	Oscillator Frequency	4	U	R/W	
R_TEMP_OFFSET[3:0]	00h	Temperature sensor offset	4	U	R/W	
R_APC_FF_SET[7:6]	01h	APC FF Setting	2	U	R/W	see Table 4-4
R_APC_FB_SET[5:4]	01h	APC FB Setting	2	U	R/W	see Table 4-4
R_APC_INIT_SET[3]	01h	APC FB Initial Setting	1	U	R/W	0: No initial Setting 1: Initial Setting
R_SFP[2]	01h	MSA(SFP) Setting	1	U	R/W	0: No SFP Support 1: SFP Support
R_DAC1_GAIN[1]	01h	I-DAC1 Gain	1	U	R/W	0: Gain = 1/2 1: Gain = 1
R_DAC2_GAIN[0]	01h	I-DAC2 Gain	1	U	R/W	0: Gain = 1/2 1: Gain = 1
R_TEMP_DET[5]	02h	Temperature compensation at shutdown release ON/OFF	1	U	R/W	0: OFF 1: ON
R_TIMER_OPTALM[4]	02h	Delay time of TXFAULT detection with OPTALM	1	U	R/W	0: 160ms 1: 2ms
R_ALM_POL[3]	02h	ALM Polarity	1	U	R/W	0: "H" 1: "L"
R_OPTALM[1:0]	02h	OPTALM Reference Level	2	U	R/W	00: 1/3, 01: 1/4 10: 1/6, 11: 1/7
R_TEMP_WIN[6:0]	03h	Temperature Difference Detection Level	7	U	R/W	see section 6.2
R_DAC1_FBRT[6:0]	05h	APC FB Ratio for I-DAC1	7	U	R/W	see section 4.3
R_DATAALM_MASK[0]	06h	DATAALM Mask	1	U	R/W	0: DATAALM Valid 1: DATAALM Invalid
R_DAC2_FBRT[6:0]	07h	APC FB Ratio for I-DAC2	7	U	R/W	see section 4.3
R_PDGAIN[5:0]	08h	PDGAIN	6	U	R/W	see Table 4-2
R_TEMPALM[6:0]	09h	TEMPALM Level	7	U	R/W	see Table 4-9
R_TEMP[6:0]	0Ah	Detected Temperature	7	U	R(W)	see Table 4-9
R_TEMP_STDW[6:0]	0Bh	Temperature at Shutdown request	7	U	R(W)	see section 6.2
R_DAC1_FF[7:0]	0Ch	I-DAC1 FF	8	U	R/W	Note 2
R_DAC2_FF[7:0]	0Dh	I-DAC2 FF	8	U	R/W	Note 3
R_APC_FB[8:0]	0Eh	APC FB	9	S	R(W)	Note 1
R_DAC1_FB[8:0]	11h	I-DAC1 FB	9	S	R(W)	Note 1
R_DAC2_FB[8:0]	12h	I-DAC2 FB	9	S	R(W)	Note 1
R_DAC1[7:0]	13h	I-DAC1	8	U	R(W)	Note 2
R_DAC2[7:0]	14h	I-DAC2	8	U	R(W)	Note 3
R_APC_TRGT[4:0]	15h	APC Reference	5	U	R/W	see Table 4-3
R_CURRALM_DAC1[7:4]	16h	CURRALM for I-DAC1	4	U	R/W	see section 5.2
R_CURRALM_DAC2[3:0]	16h	CURRALM for I-DAC2	4	U	R/W	see section 5.2
R_DUTY[4:0]	17h	Duty Adjust	5	U	R/W	
AKM Test	18h-1Dh	Test for AKM	-	-	-	

Note 1: The data format of read / write via I²C™ (8bit) is shown in Fig 8-1.
Note 2: R_DAC1 = R_DAC1_FF + R_DAC1_FB, R_DAC1>=0,
Note 3: R_DAC2 = R_DAC2_FF + R_DAC2_FB, R_DAC2 >= 0

Note 4:

(1) R/W

R: Read Only.

R/(W): Read / Write, Write data may be changed by internal operation.

R/W: Read/Write, Write data is hold unless re-writing or operation mode changing. All adjustment would be done by R/W registers.

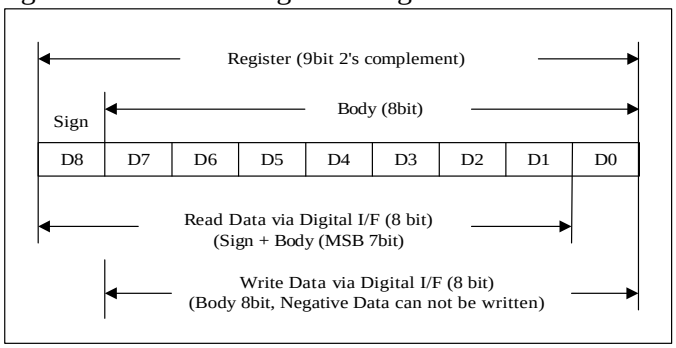
(2) Data Type

U: Unsigned, S: Signed (2's Complement)

Table 8-7 Register Map

Address	D7	D6	D5	D4	D3	D2	D1	D0
00h	VREFTRIM				TEMP_OFFSET			
01h	APC_FF_SET		APC_FB_SET		APC_ INIT_SET	SFP	DAC1_ GAIN	DAC2_ GAIN
02h			TEMP_ DET	TIMER_ OPTALM	ALM_ POL		OPTALM	
03h		TEMP_WIN						
04h								
05h		DAC1_FBRT						
06h								DATAALM_ MASK
07h		DAC2_FBRT						
08h			PDGAIN					
09h		TEMPALM						
0Ah		TEMP						
0Bh		TEMP_STDW						
0Ch	DAC1_FF							
0Dh	DAC2_FF							
0Eh	APC_FB (see Fig 8-1)							
0Fh								
10h								
11h	DAC1_FB							
12h	DAC2_FB							
13h	DAC1							
14h	DAC2							
15h				APC_TRGT				
16h	CURRALM_DAC1				CURRALM_DAC2			
17h				DUTY				
18h - 1Dh	Reserved (for AKM test)							

Fig 8-1 The data format of signed 9 bit register



9. Operation Mode

The AK2573A has 3 operating modes: Self-running, Adjustment and EEPROM mode.

9.1 Self-running Mode

Self-running mode is ready for normal operation after all adjustments are completed. In this mode, temperature detection, EEPROM access and feeding current are automatically performed using the on-chip oscillator. The AK2573A works in this mode after power-on.

9.2 Adjustment Mode

Adjustment mode is designed for training the LD characteristics. The AK2573A operates according to the register settings set through the I²C™ I/F. During adjustment mode, R_SFP should be 0.

9.3 EEPROM Mode

EEPROM mode is used for storing LD characteristics into EEPROM.

9.4 MODE Control

The AK2573A operation modes are changed through the I²C™ interface. Table 9-1 shows the access limitation of each operation mode and Table 9-2 shows the command to change operation mode.

Note: The I²C™ interface access is prohibited for 1ms after power-on or mode transfer to self-running mode.

Table 9-1 Access limitation of each operation mode

	EEPROM Access		Register Access	
Operation mode	Read	Write	Read	Write
Self-running mode (WP='L')	○	×	○	× (except mode-change command)
Adjustment mode (WP='L')	○	×	○	○
EEPROM mode (WP='L')	○	○	○	× (except mode-change command)
WP = 'H' Self-running mode only	○ (User Area Only)	×	×	×

Table 9-2 Operation mode change

Device Address	R/W	Address	Data	Operation mode
1010100	W	11111111	10100000	Self-running mode
1010100	W	11111111	10100111	Adjustment mode
1010100	W	11111111	10101110	EEPROM mode

9.5 Operation Mode Protection

When set WP = 'H', only self-running mode is selected.

10. Module Adjustment Example

Table 10-1 shows the module adjustment example.

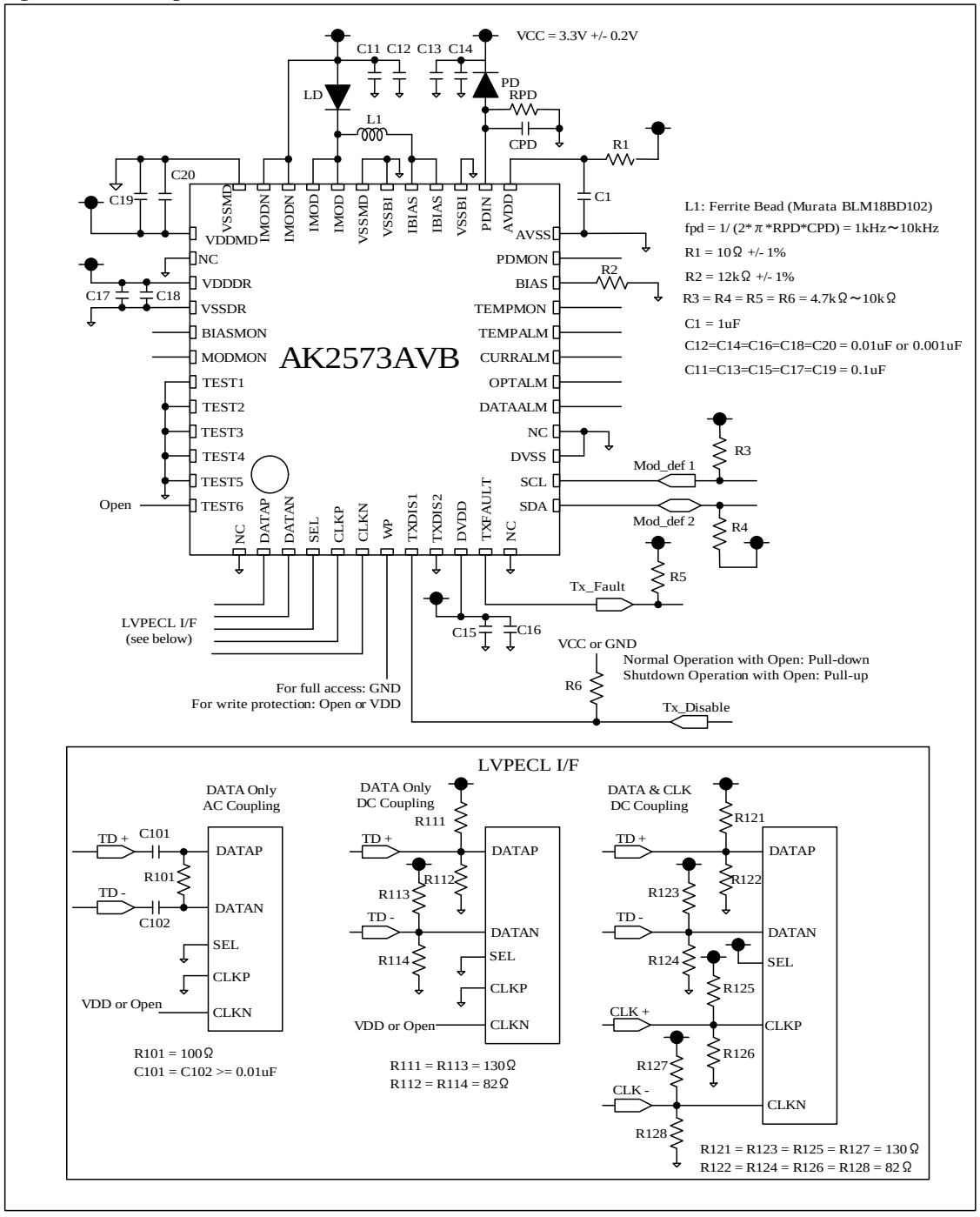
Table 10-1 Module Adjustment Example

No.	Item	Contents
1	Go to Adjustment mode	Issues "Changing to Adjustment mode command" (see Table 9-2) via I²C™ I/F.
2	SFP setting	Set R_SFP = 0 to avoid TXFAULT detection at adjustment mode.
3	APC setting	Set R_APC_FB_SET = "00" and R_APC_FF=11. BIAS and MOD current is set as "Open Loop".
4	LD current adjustment	Set R_DAC1_GAIN and R_DAC2_GAIN, then adjust R_APC_FF_DAC1 for modulation current and R_APC_FF_DAC2 for BIAS current of LD.
5	Duty adjustment	Adjust R_DUTY for 50% duty of LD power, if necessary. After duty adjustment, tune MOD and BIAS current by R_APC_FF_DAC1 and 2, if necessary.
6-A	PDGAIN adjustment	Adjust R_PDGAIN for PDMON = 1V. Go to step-7. If you cannot measure PDMON voltage, see step 6-B.
6-B	PDGAIN adjustment	Set R_APC_TRGT=100000 and R_PDGAIN=000000 (Gain=23.5dB). Then set R_APC_FF_SET and R_APC_FB_SET as your configulation. APC FB adjusts LD output automatically. Adjust R_PDGAIN for normal LD output. R_APC_TRGT adjustment is for fine tunning of optical power. Go to step-8.
7	APC FB setting	Set R_APC_TRGT = "10000". Set R_APC_FB_SET according to your configuration.
8	APC FB target adjustment	Adjust R_APC_TRGT to tunning LD output. LD output is adjusted automaticaaly according to the R_APC_TRGT.
9	Read temperature data	Read R_TEMP (on-chip temperature sensor detection temperature).
10	Estimate LD temperature characteristics	(1) 2 or more temperature adjustment Do step 2 to 8 with different temperature and estimate LD current data of look-up table. (2) Single point adjustment Calculate LD current data of look-up table with on-chip temperature sensor gain (-1.49°C/LSB), R_TEMP and LD characteristics.
11	Write adjustment data to EEPROM	(1) Make the data for EEPROM. (2) Issue mode change command to EEPROM. (3) Write adjustment data to EEPROM. (4) Read EEPROM data and verify it.
12	Self running mode	Issue mode change command to self-running. AK2573A operates temperature detection, feed current in response to temperature, and a feedback operation automatically according to the data in EEPROM.

Ⅶ. Circuit Example

Fig-A illustrates circuit example of AK2573A.

Fig-A Circuit Example



IMPORTANT NOTICE

- These products and their specifications are subject to change without notice.
  Before considering any use or application, consult the Asahi Kasei Microsystems Co., Ltd. (AKM) sales office or authorized distributor concerning their current status.
- AKM assumes no liability for infringement of any patent, intellectual property, or other right in the application or use of any information contained herein.
- Any export of these products, or devices or systems containing them, may require an export license or other official approval under the law and regulations of the country of export pertaining to customs and tariffs, currency exchange, or strategic materials.
- AKM products are neither intended nor authorized for use as critical components in any safety, life support, or other hazard related device or system, and AKM assumes no responsibility relating to any such use, except with the express written consent of the Representative Director of AKM. As used here:
  (a) A hazard related device or system is one designed or intended for life support or maintenance of safety or for applications in medicine, aerospace, nuclear energy, or other fields, in which its failure to function or perform may reasonably be expected to result in loss of life or in significant injury or damage to person or property.
  (b) A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
- It is the responsibility of the buyer or distributor of an AKM product who distributes, disposes of, or otherwise places the product with a third party to notify that party in advance of the above content and conditions, and the buyer or distributor agrees to assume any and all responsibility and liability for and hold AKM harmless from any and all claims arising from the use of said product in the absence of such notification.