PRECISION CLOCK GENERATOR OC-192 APPLICATIONS

IDT5T940

FEATURES:

- **Input frequency:**
  - *For SONET non-FEC: 19.44MHz, 38.88MHz, 77.76MHz, 155.52MHz, 311.04MHz, or 622.08MHz*
  - *For SONET FEC: 20.83MHz, 41.66MHz, 83.31MHz, 166.63MHz, 333.26MHz, or 666.52MHz*
  - *For 10GE copper: 19.53MHz, 39.06MHz, 78.125MHz, 156.25MHz, 312.5MHz, or 625MHz*
  - *For 10GE optical: 20.14MHz, 40.28MHz, 80.56MHz, 161.13MHz, 322.26MHz, or 644.53MHz*
- **3-level inputs for feedback divide ratio and output frequency range selection**
- **1x, 2x, 4x, 8x, 16x, and 32x outputs on Q_{OUT}**
- **Regenerated input clock or Q_{OUT}/4 on Q_{REG}**
- **Lock indicator**
- **Power-down mode**
- **LVPECL or LVDS outputs**
- **Three modes of output frequency range**
  - *Mode 0: Q_{OUT} range 155.5 - 166.6MHz. Q_{REG} is a regenerated version of the input clock.*
  - *Mode 1: Q_{OUT} range 622 - 666.5MHz. Q_{REG} output 155.5-166.6MHz.*
  - *Mode 2: Q_{OUT} range 622 - 666.5MHz. Q_{REG} is a regenerated version of the input clock frequency.*
- **Selectable loop bandwidths**
- **Hitless switchover**
- **Differential LVPECL, LVDS, or single-ended LVTTL input interface**
- **2.375 - 3.465V core and I/O**
- **Available in VFQFPN package**

DESCRIPTION:

The IDT5T940 generates a high precision FEC (Forward Error Correction) or non-FEC source clock for SONET/SDH systems as well as a source clock for Gigabit Ethernet systems. This device also has clock regeneration capability: it creates a "clean" version of the clock input by using the internal oscillator to square the input clock's rising and falling edges and remove jitter. In the event that the main clock input fails, the device automatically locks to a backup reference clock using a hitless switchover mechanism.

This device detects loss of valid CLKIN and leaves the VCO of the PLL at the last valid frequency while an alternate input REFIN is selected. If CLKIN and REFIN are different frequencies, the multiplication factor will be adjusted to retain the same output frequency.

The IDT5T940 can act as a translator from a differential LVPECL, LVDS, or single-ended LVTTL input to LVPECL or LVDS outputs. The IDT5T940-10 has LVDS outputs and the IDT5T940-30 has LVPECL outputs.

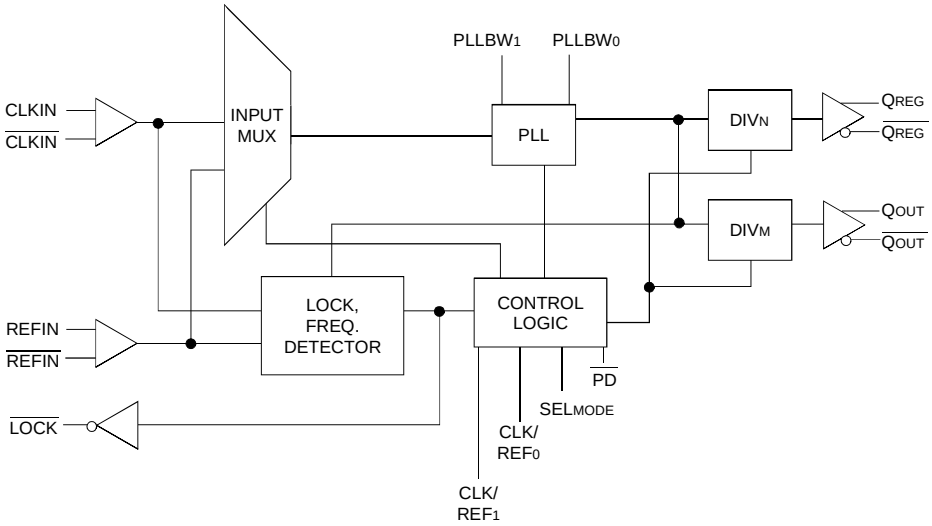
The three modes of output frequency range are controlled by the SELmode, which is a 3-level pin. When SELmode is high or low, the Q_{OUT} is a multiplied version of the input clock while Q_{REG} is a regenerated version of the input clock. When SELmode is mid, the Q_{OUT} is a multiplied version of the input clock while Q_{REG} is Q_{OUT}/4.

The IDT5T940 features a selectable loop bandwidth.

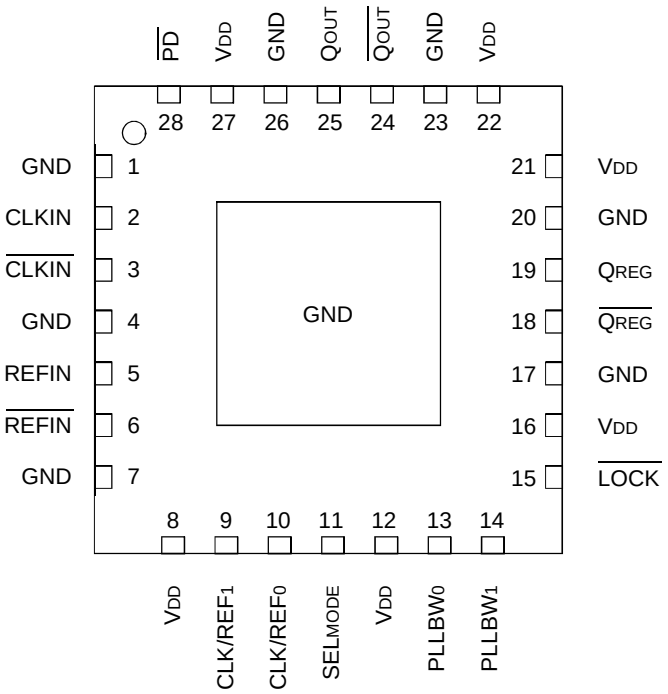
APPLICATIONS:

- **Terabit routers**
- **Gigabit ethernet systems**
- **SONET / SDH systems**
- **Digital cross connects**
- **Optical transceiver modules**

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



VFQFPN
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{DD}	Power Supply Voltage	–0.5 to +4.1	V
V_I	Input Voltage	–0.5 to +4.1	V
V_O	Output Voltage	–0.5 to V_{DD}+0.5	V
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	–65 to +165	°C

NOTE:
1. Stresses beyond those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

CAPACITANCE (T_A = +25°C, f = 1MHz, V_{IN} = 0V)

Parameter	Description	Typ.	Max.	Unit
C_{IN}	Input Capacitance	2.5	3	pF
C_{OUT}	Output Capacitance	—	—	pF

NOTE:
1. Capacitance applies to all inputs except $CLK/REF_{[1:0]}$ and SELmode.

RECOMMENDED OPERATING RANGE

Symbol	Description	Min.	Typ.	Max.	Unit
T_A	Ambient Operating Temperature	–40	+25	+85	°C
V_{DD}	Power Supply Voltage	2.375	—	3.465	V
V_T	Termination Voltage (LVPECL)	—	V_{DD} – 2	—	V
	Termination Voltage (LVDS)	—	1.2	—	

PLL BANDWIDTH SELECTION

PLLBW[1:0]	Min.	Max.	Min. CLKIN/REFIN
LL	65KHz	120KHz	19.44MHz
LH	250KHz	500KHz	19.44MHz
HL	1MHz	2MHz	38.88MHz
HH	4MHz	8MHz	155.52MHz

OUTPUT FREQUENCY RANGE

SELmode	$Q_{OUT}/\overline{Q_{OUT}}$	$Q_{REG}/\overline{Q_{REG}}$	Unit
L	155.5 - 166.6	regenerated CLKIN/$\overline{CLKIN}$	MHz
M	622 - 666.5	155.5 - 166.6	MHz
H	622 - 666.5	regenerated CLKIN/$\overline{CLKIN}$	MHz

INPUT FREQUENCY RANGE

CLK/REF[1:0]	Input Frequency Range
HH	19.4MHz - 20.9MHz
HM	reserved
HL	38.8MHz - 41.7MHz
MH	77.7MHz - 83.4MHz
MM	Automatic Detection
ML	155.5MHz - 167MHz
LH	311MHz - 334MHz
LM	reserved
LL	622MHz - 667MHz

$\overline{LOCK}$ FREQUENCY DETECTOR

The 5T940 will lock to, and track, a valid CLKIN signal; $\overline{LOCK}$ will be low when this has occurred. If CLKIN fails, the 5T940 PLL will smoothly switch to lock to REFIN without generating any glitches on the output. The fact that the PLL is locked to REFIN rather than CLKIN is indicated by a high state on $\overline{LOCK}$. When a valid input is then applied to CLKIN, the 5T940 will smoothly switch back to locking on CLKIN, and $\overline{LOCK}$ will go low. $\overline{LOCK}$ will also switch to high should the frequency of CLKIN drift close to the limits of the VCO tuning range.

PIN DESCRIPTION

Pin Name	I/O	Type	Description
CLKIN, $\overline{CLKIN}$	I	Adjustable(1)	Differential or single-ended clock input signal. For differential, LVPECL or LVDS supported. If left open-circuited, inputs will float to LVTTL threshold voltage so that either input may be used as a single-ended input. A capacitor to ground should be connected on the floating input.
REFIN, $\overline{REFIN}$	I	Adjustable(1)	Differential reference clock input. The reference clock input is used as an input to the PLL when CLKIN/$\overline{CLKIN}$ fails. Differential or single-ended clock input signal. For differential, LVPECL or LVDS supported. If left open-circuited, inputs will float to LVTTL threshold voltage so that either input may be used as a single-ended input. A capacitor to ground should be connected on the floating input.
CLK/REF[1:0]	I	3-level(2)	3 level inputs controlling PLL feedback divider ratio. Automatic detection is used if both inputs are MID.
SELmode	I	3-level(2)	3 level input to select output frequency range for $Q_{OUT}/\overline{Q_{OUT}}$ and $Q_{REG}/\overline{Q_{REG}}$ (see Output Frequency Range table)
PLLBW[1:0]	I	LVTTL	PLL Bandwidth Select Inputs (see PLL Bandwidth Selection table)
$\overline{PD}$	I	LVTTL	Power Down Control. Shuts off entire chip when LOW.
Q_{OUT}, $\overline{Q_{OUT}}$	0	Adjustable(3)	Differential clock output. LVPECL or LVDS outputs.
Q_{REG}, $\overline{Q_{REG}}$	0	Adjustable(3)	Regenerated clock output from CLKIN/$\overline{CLKIN}$, LVPECL, or LVDS outputs.
$\overline{LOCK}$	0	LVTTL	LOW when PLL is locked to CLKIN, HIGH in all other conditions
V_{DD}		PWR	Power Supply
GND		PWR	Ground

NOTES:

1. Inputs are capable of translating the following interface standards:
   Single-ended 3.3V LVTTL levels
   Single-ended 2.5V LVTTL levels
   Differential LVPECL levels
   Differential LVDS levels
2. 3-level inputs are static inputs and must be tied to V_{DD} or GND or left floating.
3. Outputs can be LVPECL or LVDS.

CLOCK INPUT/OUTPUT CONFIGURATION DESCRIPTION

Application	REFIN (MHz)	CKIN (MHz)	SELmode	Q_{REG} (MHz)	Q_{OUT} (MHz)
Non-FEC	19.44, 38.88, 77.76, 155.52, 311.04, 622.08	19.44	LOW	19.44	155.52
			MID	155.52	622.08
			HIGH	19.44	622.08
		38.88	LOW	38.88	155.52
			MID	155.52	622.08
			HIGH	38.88	622.08
		77.76	LOW	77.76	155.52
			MID	155.52	622.08
			HIGH	77.76	622.08
		155.52	LOW	155.52	155.52
			MID	155.52	622.08
			HIGH	155.52	622.08
		311.04	LOW	311.04	155.52
			MID	155.52	622.08
			HIGH	311.04	622.08
		622.08	LOW	622.08	155.52
			MID	155.52	622.08
			HIGH	622.08	622.08
FEC	20.83, 41.66, 83.31, 166.63, 333.26, 666.52	20.83	LOW	20.83	166.63
			MID	166.63	666.52
			HIGH	20.83	666.52
		41.66	LOW	41.66	166.63
			MID	166.63	666.52
			HIGH	41.66	666.52
		83.31	LOW	83.31	166.63
			MID	166.63	666.52
			HIGH	83.31	666.52
		166.63	LOW	166.63	166.63
			MID	166.63	666.52
			HIGH	166.63	666.52
		333.26	LOW	333.26	166.63
			MID	166.63	666.52
			HIGH	333.26	666.52
		666.52	LOW	666.52	166.63
			MID	166.63	666.52
			HIGH	666.52	666.52

CLOCK INPUT/OUTPUT CONFIGURATION DESCRIPTION (CONTINUED)

Application	REFIN (MHz)	CKIN (MHz)	SEL mode	Q_{REG} (MHz)	Q_{OUT} (MHz)
10GE copper	19.53, 39.06, 78.12, 156.25, 312.5, 625	19.53	LOW	19.53	156.25
			MID	156.25	625
			HIGH	19.53	625
		39.06	LOW	39.06	156.25
			MID	156.25	625
			HIGH	39.06	625
		78.12	LOW	78.12	156.25
			MID	156.25	625
			HIGH	78.12	625
		156.25	LOW	156.25	156.25
			MID	156.25	625
			HIGH	156.25	625
		312.5	LOW	312.50	156.25
			MID	156.25	625
			HIGH	312.5	625
		625	LOW	625	156.25
			MID	156.25	625
			HIGH	625	625
10GE optical	20.14, 40.28, 80.56, 161.13, 322.26, 644.53	20.14	LOW	20.14	161.13
			MID	161.13	644.53
			HIGH	20.14	644.53
		40.28	LOW	40.28	161.13
			MID	161.13	644.53
			HIGH	40.28	644.53
		80.56	LOW	80.56	161.13
			MID	161.13	644.53
			HIGH	80.56	644.53
		161.13	LOW	161.13	161.13
			MID	161.13	644.53
			HIGH	161.13	644.53
		322.26	LOW	322.26	161.13
			MID	161.13	644.53
			HIGH	322.26	644.53
		644.53	LOW	644.53	161.13
			MID	161.13	644.53
			HIGH	644.53	644.53

POWER SUPPLY CHARACTERISTICS(1,2)

Symbol	Parameter	Test Conditions	Typ.	Max	Unit
I_{DD_PD}	Power Supply Current	V_{DD} = Max., $\overline{PD}$ = GND, All outputs unloaded	—	50	µA
ΔI_{DD}	Power Supply Current per Input HIGH (LVTTL inputs only)	V_{DD} = Max., V_{IN} = 2.375V	—	100	µA
I_{TOT}	Total Power Supply Current	V_{DD} = Max., Q_{OUT} = 622MHz, All outputs unloaded	—	200	mA

NOTES:

1. These power consumption characteristics are for all the valid input interfaces and cover the worst case input and output interface combinations.
2. As a general requirement, these parts must be capable of operating at the maximum frequency under a nominal load at a reasonable operating temperature. That means that these parts must not burn up under extended use in a typical application.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Test Conditions		Min.	Max	Unit
V_{IHH}	Input HIGH Voltage Level(1)	3-Level Inputs Only		V_{DD} – 0.4	—	V
V_{IMM}	Input MID Voltage Level(1)	3-Level Inputs Only		V_{DD}/2 – 0.2	V_{DD}/2 + 0.2	V
V_{ILL}	Input LOW Voltage Level(1)	3-Level Inputs Only		—	0.4	V
I_3	3-Level Input DC Current	V_{IN} = V_{DD}	HIGH Level	—	200	µA
		V_{IN} = V_{DD}/2	MID Level	–50	+50	
		V_{IN} = GND	LOW Level	–200	—	

NOTE:

1. These inputs are normally wired to V_{DD}, GND, or left floating. Internal termination resistors bias unconnected inputs to V_{DD}/2. If these inputs are switched dynamically after powerup, the function and timing of the outputs may be glitched, and the PLL may require additional t_{AQ} time before all datasheet limits are achieved.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR LVTTL

Symbol	Parameter	Test Conditions	Min.	Typ.	Max	Unit
I_{IH}	Input HIGH Current	V_{DD} = 3.465V	—	—	±1	µA
I_{IL}	Input LOW Current	V_{DD} = 3.465V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{DD} = 2.375V, I_{IN} = -18mA	—	- 0.7	- 1.2	V
V_{IN}	DC Input Voltage		- 0.3	—	+3.465	V
V_{IH}	DC Input HIGH		1.7	—	—	V
V_{IL}	DC Input LOW		—	—	0.7	V

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR LVPECL(1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Input Characteristics						
I_{IN}	Input Current (CLKIN, REFIN)	V_{DD} = 3.465V	-20	—	+20	µA
V_{CMR}	Common Mode Input Voltage		1	—	V_{DD} - 0.3	V
V_{DIF}	Differential Voltage Required to Toggle Input		100	—	—	mV
Output Characteristics						
V_{OH}	Output Voltage HIGH (terminated through 50Ω tied to V_{DD} - 2V)(2)		V_{DD} - 1.15	—	V_{DD} - 0.9	V
V_{OL}	Output Voltage LOW (terminated through 50Ω tied to V_{DD} - 2V)(2)		V_{DD} - 1.95	—	V_{DD} - 1.61	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.55	—	0.93	V

NOTES:

1. V_{DD} = 2.375 - 3.645V.
2. Not to exceed V_{DD} - 0.05V.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR LVDS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Input Characteristics						
I_{IN}	Input Current (CLKIN, REFIN)	V_{DD} = 3.465V	-20	—	+20	µA
V_{CM}	Common Mode Input Voltage Range(1)		0.9	—	V_{DD} - 0.05	V
V_{DIF}	Differential Voltage Required to Toggle Input		100	—	—	mV
Output Characteristics						
$V_{OT(+)}$	Differential Output Voltage for the TRUE Binary State		247	—	454	mV
$V_{OT(-)}$	Differential Output Voltage for the FALSE Binary State		-247	—	-454	mV
ΔV_{OT}	Change in V_{OT} Between Complementary Output States		—	—	50	mV
V_{OS}	Output Common Mode Voltage (Offset Voltage)		1.125	1.2	1.375	V
ΔV_{OS}	Change in V_{OS} Between Complementary Output States		—	—	50	mV
I_{OS}	Outputs Short Circuit Current	$V_{OUT(+)}$ and $V_{OUT(-)}$ = 0V	—	9	24	mA
I_{OSD}	Differential Outputs Short Circuit Current	$V_{OUT(+)} = V_{OUT(-)}$	—	6	12	mA

NOTE:
1. Not to exceed V_{DD} - 0.05V.

INPUT TIMING REQUIREMENTS

Symbol	Parameter	Min.	Typ.	Max.	Unit
REF_H	Input Reference Clock Duty Cycle	40	50	60	%
F_{REF}	Input Reference Clock Range	19.44	—	666.52	MHz
REF_{TOL}	Input Reference Clock Frequency Tolerance	-100	—	100	ppm
F_{CLKIN}	Clock in Frequency Range	19.44	—	666.52	MHz
$CLKIN_H$	Clock in Duty Cycle	40	50	60	%
t_{AQ}	Acquisition Time from Return of Valid CLKIN	—	60	150	us
$LOCK_{TOL}$	Frequency Tolerance for LOCK	-600	±450	600	ppm
$t_{JIT(TOL)}$	Tolerance to Input Jitter	GR-253 Sect. 5.6.2.2			

AC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (OC-192)

Symbol	Parameter		Min.	Typ.	Max.	Unit
Q_{OUT}	Multiplied Clock Output Frequency	SELmode = LOW	155.52	—	166.63	MHz
		SELmode = MID	155.52	—	666.52	
		SELmode = HIGH	622.08	—	666.52	
Q_{REG}	Regenerated Clock Output Frequency		19.44	—	666.52	MHz
CLKIN	Input Clock Frequency		19.44	—	667	MHz
t_R	Output Rise Time	LVPECL	—	150	—	ps
		LVDS	—	100	—	
t_F	Output Fall Time	LVPECL	—	150	—	ps
		LVDS	—	100	—	
t_{SK}	Skew between Q_{OUT} and Q_{REG}		—	10	20	ps
PLLBW	PLL Bandwidth Setting		65	80	120	KHz
t_P	Jitter Transfer Peaking		—	—	0.1	dB
t_J	Jitter Generation(1)	Output Frequency = 622MHz - 666.5MHz	—	0.3	0.65	ps (RMS)
	(with 50KHz to 80MHz band pass filter)	Output Frequency = 155.5MHz - 166.6MHz	—	1	2	
t_{DUTY}	Output Duty Cycle		45	—	55	%

NOTE:
1. All input frequencies and $PLLBW_{[1:0]}$ permitted by PLL Bandwidth Selection table.

AC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (OC-48)

Symbol	Parameter		Min.	Typ.	Max.	Unit
Q_{OUT}	Multiplied Clock Output Frequency	SELmode = LOW	155.52	—	166.63	MHz
		SELmode = MID	155.52	—	666.52	
		SELmode = HIGH	622.08	—	666.52	
Q_{REG}	Regenerated Clock Output Frequency		19.44	—	666.52	MHz
CLKIN	Input Clock Frequency		19.44	—	667	MHz
t_R	Output Rise Time	LVPECL	—	150	—	ps
		LVDS	—	100	—	
t_F	Output Fall Time	LVPECL	—	150	—	ps
		LVDS	—	100	—	
t_{SK}	Skew between Q_{OUT} and Q_{REG}		—	10	20	ps
PLLBW	PLL Bandwidth Setting		65	80	120	KHz
			250	305	500	
t_P	Jitter Transfer Peaking		—	0.05	0.1	dB
t_J	Jitter Generation (with 12KHz to 20MHz filter)(1)	Output frequency = 622MHz - 666.5MHz	—	0.1	0.3	ps (RMS)
		Output frequency = 155.5MHz - 166.6MHz	—	0.4	1.5	
		Output frequency = 77.7MHz - 83.4MHz	—	0.5	1.7	
t_{DUTY}	Output Duty Cycle		45	—	55	%

NOTE:

1. All input frequencies and PLLBW[1:0] permitted by PLL Bandwidth Selection table.

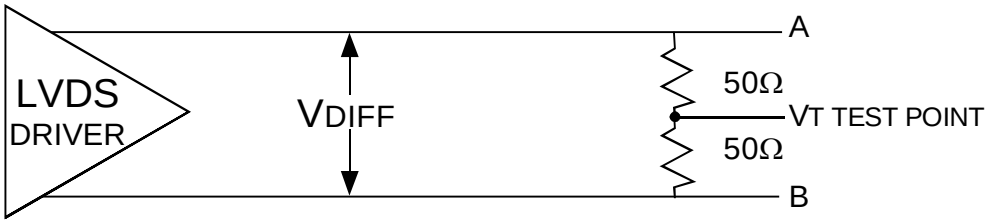
AC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (OC-12)

Symbol	Parameter		Min.	Typ.	Max.	Unit
Q_{OUT}	Multiplied Clock Output Frequency	SELmode = LOW	155.52	—	166.63	MHz
		SELmode = MID	155.52	—	666.52	
		SELmode = HIGH	622.08	—	666.52	
Q_{REG}	Regenerated Clock Output Frequency		19.44	—	666.52	MHz
CLKIN	Input Clock Frequency		19.44	—	667	MHz
t_R	Output Rise Time	LVPECL	—	150	—	ps
		LVDS	—	100	—	
t_F	Output Fall Time	LVPECL	—	150	—	ps
		LVDS	—	100	—	
t_{SK}	Skew between Q_{OUT} and Q_{REG}		—	10	20	ps
PLLBW	PLL Bandwidth Setting		65	80	120	KHz
			250	305	500	
			1000	1250	2000	
t_P	Jitter Transfer Peaking		—	0.05	0.1	dB
t_J	Jitter Generation (with 3KHz to 5MHz filter)(1)	Output frequency = 155.5MHz - 166.6MHz	—	0.3	1.1	ps (RMS)
		Output frequency = 77.7MHz - 83.4MHz	—	0.4	1.3	
		Output frequency = 19.4MHz - 20.9MHz	—	0.5	1.6	
t_{DUTY}	Output Duty Cycle		45	—	55	%

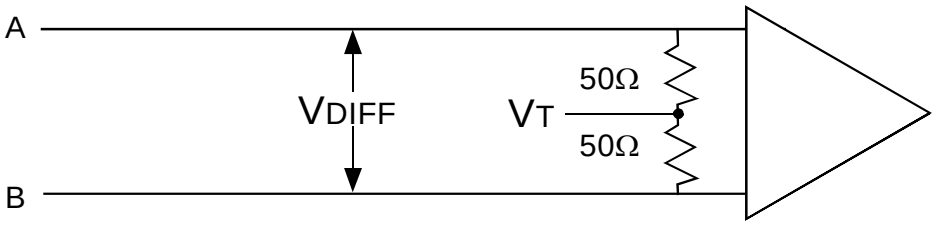
NOTE:

1. All input frequencies and PLLBW[1:0] permitted by PLL Bandwidth Selection table.

TEST CONDITIONS

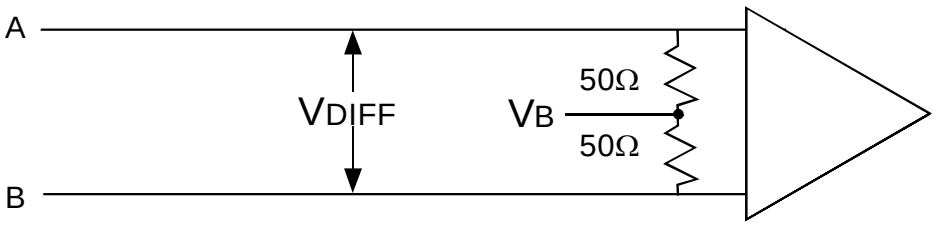


Test Circuit for LVDS Output Characteristics



Test Circuit for LVDS Input Characteristics

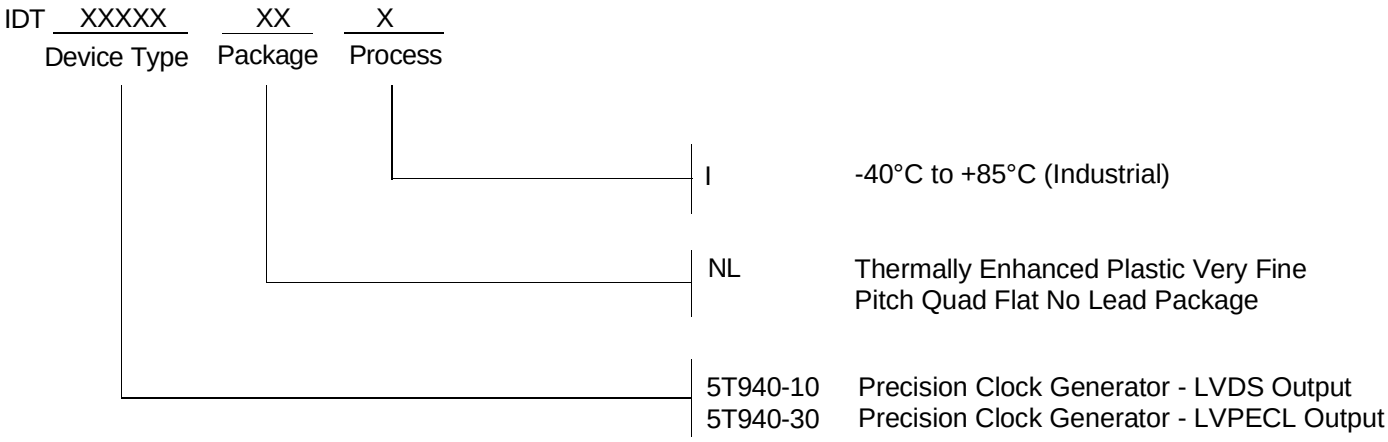
Test Circuit for LVPECL Output Characteristics



$V_B = V_{DD} - 2V$

Test Circuit for LVPECL Input Characteristics

ORDERING INFORMATION



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