DATASHEET

AX50424

Version 1.3

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Table of Contents

1. Overview

1.1. Features

- **Advanced multi-channel single chip UHF receiver**
- **Configurable for usage in 400-470 MHz and 800-930 MHz SRD bands**
- **Wide variety of modulations supported (ASK, PSK, MSK, FSK, 4-FSK, OQPSK)**
- **Data rates from 0.1 to 400 kbps (FSK, MSK, 4-FSK) and to 600 kbps (ASK, PSK)**
- **Ultra fast settling RF frequency synthesizer for low-power consumption**
- **Variable channel filtering from 2.4 kHz to 600 kHz**
- **32-bit preamble match unit**
- **RF carrier frequency programmable in 256 Hz steps**
- **Fully integrated RF frequency synthesizer with VCO auto-ranging and band-width boost modes for fast locking**
- **Few external components**
- **On-chip communication controller and flexible digital modem**
- **Channel hopping up to 2000 hops/s**
- **Sensitivity down to –122 dBm**
- **Crystal oscillator with programmable transconductance and programmable internal tuning capacitors for low cost crystals**
- **Automatic frequency control (AFC)**
- **SPI micro-controller interface**
- **Fully integrated current/voltage references**
- **QFN28 package**
- **Low power receiver: 20 - 21 mA in high sensitivity mode and 17-18 mA in low power mode**
- **Extended supply voltage range 2.3V - 3.6V**
- **Internal power-on-reset**
- **128 bit RX data FIFO**
- **Optional spectral shaping using a self synchronizing shift register**
- **Brown-out detection**
- **Differential antenna pins**

1.2. Applications

400-470 MHz and 800-930 MHz data reception in the Short Range Devices (SRD) band.

- 433/868/915 MHz SRD band systems
- Paging receivers
- Multi-channel home automation standards
- Konnex applications
- Wireless networks
- Telemetric applications, sensor readout
- Toys
- Access control
- Remote keyless entry
- ARIB compatible
- Active RFID
- 433/868/915 MHz SRD band systems

2. Block Diagram

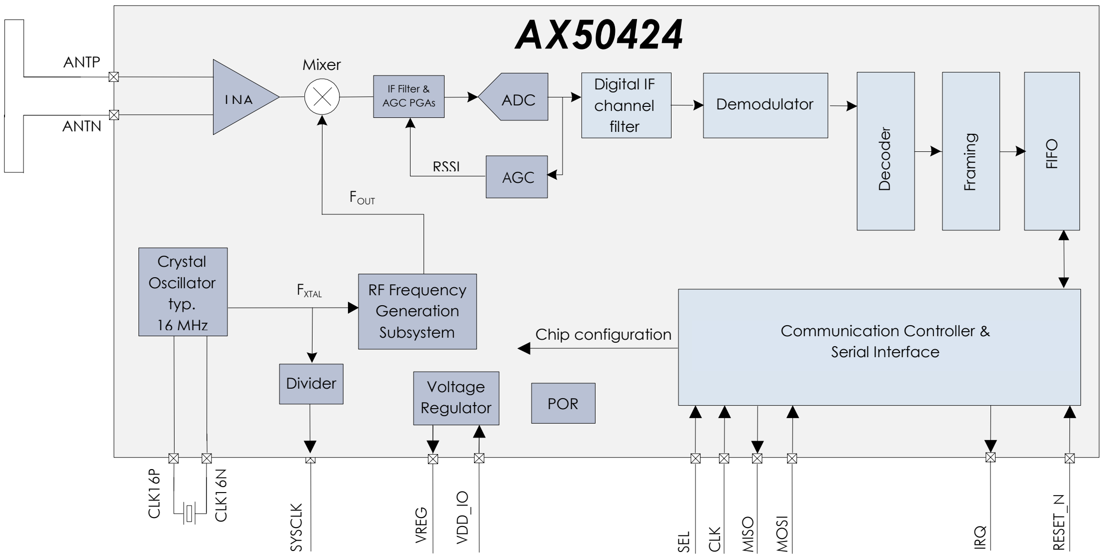


Figure 1 Functional block diagram of the AX50424

3. Pin Function Descriptions

Symbol	Pin(s)	Type	Description
NC	1	N	Not to be connected
VDD	2	P	Power supply, must be supplied with regulated voltage VREG
GND	3	G	Ground
ANTP	4	A	Antenna input
ANTN	5	A	Antenna input
GND	6	P	Ground
VDD	7	P	Power supply, must be supplied with regulated voltage VREG
NC	8	N	Not to be connected
TST1	9	O	Not to be connected
TST2	10	O	Not to be connected
GND	11	P	Ground
RESET_N	12	I	Optional reset pin. If this pin is not used it must be connected to VDD_IO.
SYSCLK	13	I/O	Default functionality: Crystal oscillator (or divided) clock output Can be programmed to be used as a general purpose I/O pin
SEL	14	I	Serial peripheral interface select
CLK	15	I	Serial peripheral interface clock
MISO	16	O	Serial peripheral interface data output
MOSI	17	I	Serial peripheral interface data input
TST3	18	O	Not to be connected
IRQ	19	I/O	Default functionality: Receive interrupt Can be programmed to be used as a general purpose I/O pin
VDD_IO	20	P	Unregulated power supply
NC	21	I/O	Not connected
GND	22	P	Ground
NC	23	N	Not connected
VREG	24	P	Regulated output voltage VDD pins must be connected to this supply voltage A 1µF low ESR capacitor to GND must be connected to this pin
NC	25	N	Not to be connected
VDD	26	P	Power supply, must be supplied with regulated voltage VREG
CLK16P	27	A	Crystal oscillator input/output
CLK16N	28	A	Crystal oscillator input/output

A = analog signal
I = digital input signal
O = digital output signal
I/O = digital input/output signal
N = not to be connected
P = power or ground

All digital inputs are Schmitt trigger inputs, digital input and output levels are LVCMOS/LVTTL compatible and 3.3V/5V tolerant.

The centre pad of the QFN28 package should be connected to GND.

3.1. Pinout Drawing

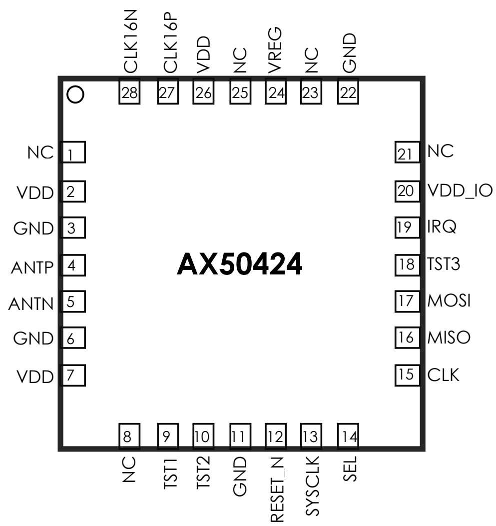


Figure 2: Pinout drawing (Top view)

4. Specifications

4.1. Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SYMBOL	DESCRIPTION	CONDITION	MIN	MAX	UNIT
VDD_IO	Supply voltage		-0.5	5.5	V
IDD	Supply current			50	mA
P_{tot}	Total power consumption			800	mW
P_i	Absolute maximum input power at receiver input			15	dBm
I_{I1}	DC current into any pin except ANTP, ANTN		-10	10	mA
I_{I2}	DC current into pins ANTP, ANTN		-100	100	mA
I_O	Output Current			40	mA
V_{ia}	Input voltage ANTP, ANTN pins		-0.5	5.5	V
	Input voltage digital pins		-0.5	5.5	V
V_{es}	Electrostatic handling	HBM	-2000	2000	V
T_{amb}	Operating temperature		-40	85	°C
T_{stg}	Storage temperature		-65	150	°C
T_j	Junction Temperature			150	°C

4.2. DC Characteristics

Supplies

SYMBOL	DESCRIPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
T_{AMB}	Operational ambient temperature		-40	27	85	°C
VDD_IO	I/O and voltage regulator supply voltage	RX operation	2.3	3.0	3.6	V
VREG	Internally regulated supply voltage	Stand-by mode PWRMODE=0x04	2.1	2.5	2.8	V
		Power-down mode PWRMODE=0x00		1.7		V
$VREG_{droptyp}$	Regulator voltage drop	RX operation			50	mV
I_{PDOWN}	Power-down current	PWRMODE=0x00		0.5		µA
I_{RX-HS}	Current consumption RX High sensitivity mode: VCO_I=001; REF_I=011	868 MHz, bit rate 10 kbit/s		20		mA
		868 MHz, bit rate 600 kbit/s		21		
		433 MHz, bit rate 10 kbit/s		20		
		433 MHz, bit rate 600 kbit/s		21		
I_{RX-LP}	Current consumption RX Low power mode: VCO_I=001; REF_I=101	868 MHz, bit rate 10 kbit/s		17		mA
		868 MHz, bit rate 600 kbit/s		18		
		433 MHz, bit rate 10 kbit/s		17		
		433 MHz, bit rate 600 kbit/s		18		

Logic

SYMBOL	DESCRIPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
DIGITAL INPUTS						
V_{T+}	Schmitt trigger low to high threshold point			1.9		V
V_{T-}	Schmitt trigger high to low threshold point			1.2		V
V_{IL}	Input voltage, low				0.8	V
V_{IH}	Input voltage, high		2.0			V
I_L	Input leakage current		-10		10	µA
DIGITAL OUTPUTS						
I_{OH}	Output Current, high	V_{OH}= 2.4V	4			mA
I_{OL}	Output Current, low	V_{OL}= 0.4V	4			mA
I_{OZ}	Tri-state output leakage current		-10		10	µA

4.3. AC Characteristics

Crystal Oscillator

SYMBOL	DESCRIPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
f_{XTAL}	Crystal frequency	Note 1		16		MHz
gm_{osc}	Transconductance oscillator	XTALOSCGM=0000		1		mS
		XTALOSCGM=0001		2		
		XTALOSCGM =0010 default		3		
		XTALOSCGM =0011		4		
		XTALOSCGM =0100		5		
		XTALOSCGM =0101		6		
		XTALOSCGM =0110		6.5		
		XTALOSCGM =0111		7		
		XTALOSCGM =1000		7.5		
		XTALOSCGM =1001		8		
		XTALOSCGM =1010		8.5		
		XTALOSCGM =1011		9		
		XTALOSCGM =1100		9.5		
		XTALOSCGM =1101		10		
		XTALOSCGM =1110		10.5		
		XTALOSCGM =1111		11		
C_{osc}	Programmable tuning capacitors at pins CLK16N and CLK16P	XTALCAP = 000000		2		pF
		XTALCAP = 111111		33		pF
$C_{osc\text{-}lsb}$	Programmable tuning capacitors, increment per LSB of XTALCAP			0.5		pF
f_{ext}	External clock input	Note 2		16		MHz
RIN_{osc}	Input DC impedance		10			kΩ

Notes

1. Tolerances and start-up times depend on the crystal used. Depending on the RF frequency and channel spacing the IC must be calibrated to the exact crystal frequency using the readings of the register TRKFREQ
2. If an external clock is used, it should be input via an AC coupling at pin CLK16P with the oscillator powered up and XTALCAP=000000

RF Frequency Generation Subsystem (Synthesizer)

SYMBOL	DESCRIPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
f_{REF}	Reference frequency			16		MHz
f_{range_hi}	Frequency range	BANDSEL=0	800		930	MHz
f_{range_low}		BANDSEL=1	400		470	
f_{RESO}	Frequency resolution		256			Hz
BW_1	Synthesizer loop bandwidth VCO current: VCOI=001	Loop filter configuration: FLT=01 Charge pump current: PLLCPI=010		100		kHz
BW_2		Loop filter configuration: FLT=01 Charge pump current: PLLCPI=001		50		
BW_3		Loop filter configuration: FLT=11 Charge pump current: PLLCPI=010		200		
BW_4		Loop filter configuration: FLT=10 Charge pump current: PLLCPI=010		500		
T_{start1}	Synthesizer start-up time if crystal oscillator and reference are running VCO current: VCO_I=001	Loop filter configuration: FLT=01 Charge pump current: PLLCPI=010		25		µs
T_{start2}		Loop filter configuration: FLT=01 Charge pump current: PLLCPI=001		50		
T_{start3}		Loop filter configuration: FLT=11 Charge pump current: PLLCPI=010		12		
T_{start4}		Loop filter configuration: FLT=10 Charge pump current: PLLCPI=010		5		
$PN868_1$	Synthesizer phase noise Loop filter configuration: FLT=01 Charge pump current: PLLCPI=010 VCO current: VCO_I=001	868 MHz, 50 kHz from carrier		-85		dBc/Hz
		868 MHz, 100 kHz from carrier		-90		
		868 MHz, 300 kHz from carrier		-100		
		868 MHz, 2 MHz from carrier		-110		
$PN433_1$		433 MHz, 50 kHz from carrier		-90		
		433 MHz, 100 kHz from carrier		-95		
		433 MHz, 300 kHz from carrier		-105		
		433 MHz, 2 MHz from carrier		-115		
$PN868_2$	Synthesizer phase noise Loop filter configuration: FLT=01 Charge pump current: PLLCPI=001 VCO current: VCO_I=001	868 MHz, 50 kHz from carrier		-80		dBc/Hz
		868 MHz, 100 kHz from carrier		-90		
		868 MHz, 300 kHz from carrier		-105		
		868 MHz, 2 MHz from carrier		-115		
$PN433_2$		433 MHz, 50 kHz from carrier		-90		
		433 MHz, 100 kHz from carrier		-95		
		433 MHz, 300 kHz from carrier		-110		
		433 MHz, 2 MHz from carrier		-122		

Receiver

SYMBOL	DESCRIPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
SBR	Signal bit rate	ASK, PSK	0.1		600	kbps
		FSK, MSK, OQPSK	0.1		400	kbps
IS_{868}	Input sensitivity at BER = 10^{-3} for 868 MHz operation	ASK 1.2 kbps		-116		dBm
		ASK 9.6 kbps		-112		
		ASK 50 kbps		-105		
		ASK 100kbps		-102		
		ASK 200 kbps		-99		
		FSK 1.2 kbps		-117		
		FSK 3.2 kbps		-115		
		4-FSK 3.2kSym/s (=6.4kBit/s)		-112		
		FSK 9.6 kbps		-111		
		FSK 50 kbps		-105		
		FSK 100kbps		-102		
		FSK 200kbps		-99		
		PSK 200 kbps		-106		
		PSK 400 kbps		-98		
		PSK 600 kbps		-96		
IS_{433}	Input sensitivity at BER = 10^{-3} for 433 MHz operation	ASK 1.2 kbps		-118		dBm
		ASK 9.6 kbps		-111		
		ASK 50 kbps		-104		
		ASK 100kbps		-101		
		ASK 200 kbps		-99		
		FSK 1.2 kbps		-122		
		FSK 9.6 kbps		-115		
		FSK 50 kbps		-107		
		FSK 100kbps		-104		
		FSK 200kbps		-100		
		PSK 200 kbps		-102		
		PSK 400 kbps		-99		
		PSK 600 kbps		-97		
IL	Maximum input level				-20	dBm
CP_{1dB}	Input referred compression point	2 tones separated by 100 kHz		-35		dBm
IIP3	Input referred IP3			-25		
RSSIR	RSSI control range			85		dB
$RSSIS_1$	RSSI step size	Before digital channel filter; calculated from register AGCCOUNTER		0.625		dB
$RSSIS_2$	RSSI step size	Behind digital channel filter; calculated from registers AGCCOUNTER, TRKAMPL		0.1		dB

SYMBOL	DESCRIPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
SEL_{868}	Adjacent channel suppression	FSK 4.8 kbps; notes 1 & 2		22		dB
	Alternate channel suppression			22		
	Adjacent channel suppression	FSK 12.5 kbps ; notes 1 & 3		20		dB
	Alternate channel suppression			22		
	Adjacent channel suppression	FSK 50 kbps; notes 1 & 4		18		dB
	Alternate channel suppression			19		
	Adjacent channel suppression	FSK 100 kbps ; notes 1 & 5		16		dB
	Alternate channel suppression			30		
	Adjacent channel suppression	PSK 200 kbps; notes 1 & 6		17		dB
	Alternate channel suppression			28		
BLK_{868}	Blocking at +/- 1MHz offset	FSK 4.8 kbps, notes 2 & 7		43		dB
	Blocking at - 2MHz offset			51		
	Blocking at +/- 10MHz offset			74		
	Blocking at +/- 100MHz offset			82		
$IMRR_{868}$	Image rejection			25		dB

Notes

1. Interferer/Channel @ BER = 10^{-3}, channel level is +10 dB above the typical sensitivity, the interfering signal is a random data signal (except PSK200); both channel and interferer are modulated without shaping
2. FSK 4.8 kbps: 868 MHz, 20kHz channel spacing, 2.4 kHz deviation, programming as recommended in the Programming Manual
3. FSK 12.5 kbps: 868 MHz, 50kHz channel spacing, 6.25 kHz deviation, programming as recommended in the Programming Manual
4. FSK 50 kbps: 868 MHz, 200 kHz channel spacing, 25 kHz deviation, programming as recommended in the Programming Manual
5. FSK 100 kbps: 868 MHz, 400kHz channel spacing, 50 kHz deviation , programming as recommended in the Programming Manual
6. PSK 200 kbps: 868 MHz, 400kHz channel spacing, programming as recommended in the Programming Manual, interfering signal is a constant wave
7. Channel/Blocker @ BER = 10^{-3}, channel level is +10dB above the typical sensitivity, the blocker signal is a constant wave; channel signal is modulated without shaping, the image frequency lies 2 MHz above the wanted signal

SPI Timing

SYMBOL	DESCRIPTION	CONDITION	MIN.	TYP.	MAX.	UNIT
Tss	SEL falling edge to CLK rising edge		10			ns
Tsh	CLK falling edge to SEL rising edge		10			ns
Tssd	SEL falling edge to MISO driving		0		10	ns
Tssz	SEL rising edge to MISO high-Z		0		10	ns
Ts	MOSI setup time		10			ns
Th	MOSI hold time		10			ns
Tco	CLK falling edge to MISO output				10	ns
Tck	CLK period	Note 1	50			ns
Tcl	CLK low duration		40			ns
Tch	CLK high duration		40			ns

Notes

1. For SPI access during power-down mode the period should be relaxed to 100ns.

For a figure showing the SPI timing parameters see section 5.14: Serial Peripheral Interface (SPI).

5. Circuit Description

The **AX50424** is a true single chip low-power CMOS receiver primarily for use in SRD bands. The on-chip receiver consists of a fully integrated RF front-end with demodulator. Base band data processing is implemented in an advanced and flexible communication controller that enables user friendly communication via the SPI interface.

AX50424 can be operated from a 2.3 V to 3.6 V power supply over a temperature range of -40 °C to 85°C, it consumes 20 - 21 mA for receiving in high sensitivity mode and 17 – 18 mA for receiving in low power mode.

The **AX50424** features make it an ideal interface for integration into various battery powered SRD solutions such as sensor readout, telemetric applications and paging receivers. As primary application, the receiver is intended for UHF radio equipment in accordance with the European Telecommunication Standard Institute (ETSI) specification EN 300 220-1 and the US Federal Communications Commission (FCC) standard CFR47, part 15. The use of **AX50424** in accordance to FCC Par 15.247, allows for improved range in the 915 MHz band.

The **AX50424** receives data via the SPI port. Interrupts control the data flow between a controller and the **AX50424**.

The **AX50424** behaves as a SPI slave interface. Configuration of the **AX50424** is also done via the SPI interface.

AX50424 supports any data rate from 0.1 kbps to 400 kbps for FSK and MSK and from 0.1 kbps for 600 kbps for ASK and PSK. To achieve optimum performance for specific data rates and modulation schemes several register settings to configure the **AX50424** are necessary, they are outlined in the following, for details see the **AX50424** Programming Manual.

The receiver supports multi-channel operation for all data rates and modulation schemes.

5.1. Voltage Regulator

The **AX50424** uses an on-chip voltage regulator to create a stable supply voltage for the internal circuitry at pin VREG from the primary supply VDD_IO. All VDD pins of the device must be connected to VREG. The antenna pins ANTP and ANTN must be DC biased to VREG. The I/O level of the digital pins is VDD_IO.

The voltage regulator requires a 1µF low ESR capacitor at pin VREG.

In power-down mode the voltage regulator typically outputs 1.7 V at VREG, if it is powered-up its output rises to typically 2.5 V. At device power-up the regulator is in power-down mode.

The voltage regulator must be powered-up before receive operations can be initiated. This is handled automatically when programming the device modes via the ***PWRMODE*** register.

Register ***VREG*** contains status bits that can be read to check if the regulated voltage is above 1.3 V or 2.3 V, sticky versions of the bits are provided that can be used to detect low supply voltage events (brown-out detection).

5.2. Crystal Oscillator

The on-chip crystal oscillator allows the use of an inexpensive quartz crystal as the RF generation subsystem's timing reference. Although a wider range of crystal frequencies can be handled by the crystal oscillator circuit, it is recommended to use 16 MHz as reference frequency since this choice allows the typical SRD band RF frequencies to be generated.

The oscillator circuit is enabled by programming the ***PWRMODE*** register. At power-up it is not enabled.

To adjust the circuit's characteristics to the quartz crystal being used without using additional external components, both the transconductance and the tuning capacitance of the crystal oscillator can be programmed.

The transconductance is programmed via register bits XTALOSCGM[3:0] in register ***XTALOSC***.

The integrated programmable tuning capacitor bank makes it possible to connect the crystal directly to pins CLK16N and CLK16P without the need for external capacitors. It is programmed using bits XTALCAP[5:0] in register ***XTALCAP***.

To synchronize the receiver frequency to a carrier signal, the oscillator frequency could be tuned using the capacitor bank however, the recommended method to implement frequency synchronization is to make use of the high resolution RF frequency generation sub-system together with the Automatic Frequency Control, both are described further down.

Alternatively a single ended reference (TXCO, CXO) may be used. The CMOS levels should be applied to CLK16P via an AC coupling with the crystal oscillator enabled.

5.3. SYSCLK Output

The SYSCLK pin outputs the reference clock signal divided by a programmable integer. Divisions from 1 to 2048 are possible. For divider ratios > 1 the duty cycle is 50%. Bits SYSCLK[3:0] in the ***PINCFG1*** register set the divider ratio. The SYSCLK output can be disabled.

Outputting a frequency that is identical to the IF frequency (default 1 MHz) on the SYSCLK pin is not recommended during receive operation, since it requires extensive decoupling on the PCB to avoid interference.

5.4. Power-on-reset (POR) and RESET_N Input

AX50424 has an integrated power-on-reset block. No external POR circuit or signal at the RESET_N pin is required, prior to POR the RESET_N pin is disabled.

After POR the **AX50424** can be reset in two ways:

1. By SPI accesses: the bit RST in the ***PWRMODE*** register is toggled.
2. Via the RESET_N pin: A low pulse is applied at the RESET_N pin. With the rising edge of RESET_N the device goes into its operational state.

After POR or reset all registers are set to their default values.

If the RESET_N pin is not used it must be tied to VDD_IO.

5.5. RF Frequency Generation Subsystem

The RF frequency generation subsystem consists of a fully integrated synthesizer, which multiplies the reference frequency from the crystal oscillator to get the desired RF frequency. The advanced architecture of the synthesizer enables frequency resolutions of 256 Hz, as well as fast settling times of 5 – 50 µs depending on the settings (see section 4.3: AC Characteristics). Fast settling times mean fast start-up, which enables low-power system design.

The frequency must be programmed to the desired carrier frequency. The RF frequency shift by the IF frequency that is required for RX operation, is automatically set when the receiver is activated and does not need to be programmed by the user. The default IF frequency is 1 MHz. It can be programmed to other values. Changing the IF frequency and thus the centre frequency of the digital channel filter can be used to adapt the blocking performance of the device to specific system requirements.

The synthesizer loop bandwidth can be programmed, this serves two purposes:

1. Start-up time optimization. Start-up is faster for higher synthesizer loop bandwidths
2. RX spurious reception optimisation, phase-noise at 300kHz to 1MHz distance from the LO and thus spurious reception improves with lower synthesizer loop bandwidths

VCO

An on-chip VCO converts the control voltage generated by the charge pump and loop filter into an output frequency. The frequency can be programmed in 256 Hz steps in the ***FREQ*** registers. For operation in the 433 MHz band, the BANDSEL bit in the ***PLLLOOP*** register must be programmed.

VCO Auto-Ranging

The **AX50424** has an integrated auto-ranging function, which allows to set the correct VCO range for specific frequency generation subsystem settings automatically. Typically it has to be executed after power-up. The function is initiated by setting the RNG_START bit in the ***PLLRANGING*** register. The bit is readable and a 0 indicates the end of the ranging process. If the bit RNGERR is 0, then the auto-ranging has been executed successfully.

Loop Filter and Charge Pump

The **AX50424** internal loop filter configuration together with the charge pump current sets the synthesizer loop band width. The loop-filter has three configurations that can be programmed via the register bits FLT[1:0] in register ***PLLLOOP***, the charge pump current can be programmed using register bits PLLCPI[2:0] also in register ***PLLLOOP***. Synthesizer bandwidths are typically 50 - 500 kHz depending on the ***PLLLOOP*** settings, for details see the section 4.3: AC Characteristics.

Registers

Register	Bits	Purpose
PLLLOOP	FLT[1:0]	Synthesizer loop filter bandwidth, recommended usage is to increase the bandwidth for faster settling time, bandwidth increases of factor 2 and 5 are possible.
	PLLCPI[2:0]	Synthesizer charge pump current, recommended usage is to decrease the bandwidth (and improve the phase-noise) for low data-rate transmissions.
	BANDSEL	Switches between 868 MHz/915 MHz and 433 MHz bands
FREQ		Programming of the carrier frequency
IFFREQHI, IFFREQLO		Programming of the IF frequency
PLLRANGING		Initiate VCO auto-ranging and check results

5.6. RF Input Stage (ANTP/ANTN)

The **AX50424** uses fully differential antenna pins.

LNA

The LNA amplifies the differential RF signal from the antenna and buffers it to drive the I/Q mixer. An external matching network is used to adapt the antenna impedance to the IC impedance. A DC feed to the regulated supply voltage VREG must be provided at the antenna pins. For recommendations, see section 7: Application Information.

I/Q Mixer

The RF signal from the LNA is mixed down to an IF of typically 1 MHz. I- and Q-IF signals are buffered for the analog IF filter.

5.7. Analog IF Filter

The mixer is followed by a complex band-pass IF filter, which suppresses the down-mixed image while the wanted signal is amplified. The centre frequency of the filter is 1 MHz, with a passband width of 1 MHz. The RF frequency generation subsystem must be programmed in such a way that for all possible modulation schemes the IF frequency spectrum fits into the passband of the analog filter.

5.8. Digital IF Channel Filter and Demodulator

The digital IF channel filter and the demodulator extract the data bit-stream from the incoming IF signal. They must be programmed to match the modulation scheme as well as the data-rate. Inaccurate programming will lead to loss of sensitivity.

The channel filter offers bandwidths of 2.4 kHz up to 600 kHz. Data-rates down to 0.1 kbit/s can be demodulated, but sensitivities will not increase significantly vs. 2.4 kbit/s.

The demodulator features a 4-FSK mode. 4-FSK is used in certain paging systems.

For detailed instructions how to program the digital channel filter and the demodulator see the **AX50424** Programming Manual, an overview of the registers involved is given in the following table. The register setups typically must be done once at power-up of the device.

Registers

Register	Remarks
CICDECHI, CICDECLO	These registers program the bandwidth of the digital channel filter.
DATARATEHI, DATARATELO	These registers specify the receiver bit rate, relative to the channel filter bandwidth.
TMGGAINHI, TMGGAINLO	These registers specify the aggressiveness of the receiver bit timing recovery. More aggressive settings allow the receiver to synchronize with shorter preambles, at the expense of more timing jitter and thus a higher bit error rate at a given signal-to-noise ratio.
MODULATION	This register selects the modulation to be used by the receiver, i.e. whether ASK, PSK, FSK, MSK or OQPSK should be used.
FOURFSK, FSKDMAXHI, FSKDMAXLO, FSKDMINHI, FSKDMINLO	These registers control the 4-FSK mode. Recommended settings and procedures are provided in the Programming Manual.
PHASEGAIN, FREQGAIN, FREQGAIN2, AMPLGAIN	These registers control the bandwidth of the phase, frequency offset and amplitude tracking loops. Recommended settings are provided in the Programming Manual.
AGCATTACK, AGCDECAY	These registers control the AGC (automatic gain control) loop slopes, and thus the speed of gain adjustments. The faster the bit-rate, the faster the AGC loop should be. Recommended settings are provided in the Programming Manual.

5.9. Decoder

The decoder is located between the Framing Unit and the Demodulator. It can optionally transform the bit-stream in the following ways:

- It can invert the bit stream.
- It can perform differential decoding. This means that a zero is transmitted as no change in the level, and a one is transmitted as a change in the level. Differential encoding is useful for PSK, because PSK transmissions can be received either as transmitted or inverted, due to the uncertainty of the initial phase. Differential encoding / decoding removes this uncertainty.
- It can perform Manchester decoding. Manchester encoding ensures that the modulation has no DC content and enough transitions (changes from 0 to 1 and from 1 to 0) for the demodulator bit timing recovery to function correctly, but does so at a doubling of the data rate.
- It can perform decoding of Spectral Shaping. Spectral Shaping removes DC content of the bit stream, ensures transitions for the demodulator bit timing recovery, and makes sure that the transmitted spectrum does not have discrete lines even if the transmitted data is cyclic. It does so without adding additional bits, i.e. without changing the data rate. Spectral Shaping uses a self synchronizing feedback shift register.

The decoder is programmed using the register ***ENCODING***, details and recommendations on usage are given in the **AX50424** Programming Manual.

5.10. Framing and FIFO

The framing unit is responsible for grouping the bit-stream arriving from the demodulator into bytes and then storing the bytes in the FIFO.

The framing unit supports two different modes:

- Raw
- Raw with Preamble Match

The micro-controller communicates with the framing unit through a 16 level × 8 bit FIFO. The FIFO decouples micro-controller timing from the radio (demodulator) timing.

The FIFO can be operated in polled or interrupt driven modes. In polled mode, the micro-controller must periodically read the FIFO status register or the FIFO count register to determine whether the FIFO needs servicing.

In interrupt mode EMPTY, NOT EMPTY, FULL, NOT FULL and programmable level interrupts are provided. By default **AX50424** signals interrupts by asserting (driving high) its IRQ line. The interrupt line is level triggered, active high. The IRQ line polarity can be inverted by programming register ***PINCFG2***. Interrupts are acknowledged by removing the cause for the interrupt, i.e. by emptying or filling the FIFO.

Basic FIFO status (EMPTY, FULL, Overrun, Underrun) are also provided during each SPI access on MISO while the micro-controller shifts out the register address on MOSI. See the SPI interface section for details. This feature significantly reduces the number of SPI accesses necessary during receive.

RAW Mode

In Raw mode, the **AX50424** de-serializes the received bit-stream and groups it into bytes.

This mode is ideal for implementing legacy protocols in software.

RAW Mode with Preamble Match

Raw mode with preamble match is similar to raw mode. In this mode, however, the receiver does not receive anything until it detects a user programmable bit pattern (called the preamble) in the receive bit-stream. When it detects the preamble, it aligns the de-serialization to it.

The preamble can be between 4 and 32 bits long. The data to be matched must be written to the ***PATTERN*** registers.

5.11. RX AGC and RSSI

AX50424 features two receiver signal strength indicators (RSSI):

1. RSSI before the digital IF channel filter.
   The gain of the receiver is adjusted in order to keep the analog IF filter output level inside the working range of the ADC and demodulator. The register ***AGCCOUNTER*** contains the current value of the AGC and can be used as an RSSI. The step size of this RSSI is 0.625 dB. The value can be used as soon as the RF frequency generation sub-system has been programmed.

2. RSSI behind the digital IF channel filter.
   The demodulator also provides amplitude information in the ***TRK_AMPLITUDE*** register. By combining both the ***AGCCOUNTER*** and the ***TRK_AMPLITUDE*** registers, a high resolution (better than 0.1dB) RSSI value can be computed at the expense of a few arithmetic operations on the micro-controller. Formulas for this computation can be found in the **AX50424** Programming Manual.

5.12. Automatic Frequency Control (AFC)

The **AX50424** has a frequency tracking register ***TRKFREQ*** to synchronize the receiver frequency to a carrier signal. For AFC adjustment, the frequency offset can be computed with the following formula:

$$\Delta f = \frac{TRKFREQ}{2^{16}} BITRATE \times FSKMUL .$$

FSKMUL is the FSK oversampling factor, it depends on the FSK bit rate and deviation used. To determine it for a specific case, see the **AX50424** Programming Manual. For modulations other than FSK, FSKMUL=1.

5.13. PWRMODE Register

The ***PWRMODE*** register controls, which parts of the chip are operating.

PWRMODE register	Name	Description	Typical Idd
0000	POWERDOWN	All digital and analog functions, except the register file, are disabled. The core supply voltage is reduced to conserve leakage power. SPI registers are still accessible, but at a slower speed.	0.5 µA
0100	VREGON	All digital and analog functions, except the register file, are disabled. The core voltage, however is at its nominal value for operation, and all SPI registers are accessible at the maximum speed.	200 µA
0101	STANDBY	The crystal oscillator is powered on; the receiver is off.	650 µA
1000	SYNTHRX	The synthesizer is running on the receive frequency. The receiver is still off. This mode is used to let the synthesizer settle on the correct frequency for receive.	11 mA
1001	FULLRX	Synthesizer and Receiver are running.	17 - 20 mA

A typical ***PWRMODE*** sequence for a receive session :

Step	PWRMODE[3:0]	Remarks
1	POWERDOWN	
2	STANDBY	The settling time is dominated by the crystal used, typical value 3 ms
3	SYNTHRX	The synthesizer settling time is 5 – 50 µs depending on settings, see section AC Characteristics
4	FULLRX	Data reception
5	POWERDOWN	

5.14. Serial Peripheral Interface (SPI)

The **AX50424** can be programmed via a four wire serial interface according SPI using the pins CLK, MOSI, MISO and SEL. Registers for setting up the **AX50424** are programmed via the serial peripheral interface in all device modes.

When the interface signal SEL is pulled low, a 16 bit configuration data stream is expected on the input signal pin MOSI, which is interpreted as D0...D7, A0...A6, R_N/W.

Data read from the interface appears on MISO.

Figure 3 shows a write/read access to the interface. The data stream is built of an address byte including read/write information and a data byte. Depending on the R_N/W bit and address bits A[6..0], data D[7..0] can be written via MOSI or read at the pin MISO.

R_N/W = 0 means read mode, R_N/W = 1 means write mode.

The read sequence starts with 7 bits of status information S[6..0] followed by 8 data bits.

The status bits contain the following information:

S6	**S5**	**S4**	**S3**	**S2**	**S1**	**S0**
PLL LOCK	FIFO OVER	FIFO UNDER	FIFO FULL	FIFO EMPTY	0	0

SPI Timing

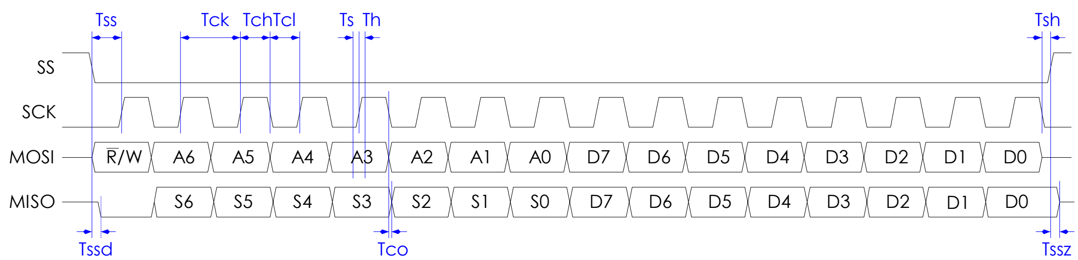


Figure 3 Serial peripheral interface timing

6. Register Bank Description

This section describes the bits of the register bank in detail. The registers are grouped by functional block to facilitate programming.

No checks are made whether the programmed combination of bits makes sense! Bit 0 is always the LSB.

Note Whole registers or register bits marked as reserved should be kept at their default values.

Note All addresses not documented here must not be accessed, neither in reading nor in writing.

6.1. Control Register Map

Addr	Name	Dir	Reset	Bit								Description
				7	6	5	4	3	2	1	0	
Revision & Interface Probing												
0	***REVISION***	R	10000111	SILICONREV(7:0)								Silicon Revision
1	***SCRATCH***	RW	11000101	SCRATCH(7:0)								Scratch Register
Operating Mode												
2	***PWRMODE***	RW	011-0101	RST	REFEN	XOEN	-	PWRMODE(3:0)				Power Mode
Crystal Oscillator, Part 1												
3	***XTALOSC***	RW	----0010	-	-	-	-	XTALOSCGM(3:0)				GM of Crystal Oscillator
FIFO, Part 1												
4	***FIFOCTRL***	R	--------	-	-	FIFO OVER	FIFO UNDER	FIFO FULL	FIFO EMPTY	-	-	FIFO Control
5	***FIFODATA***	R	--------	FIFODATA(7:0)								FIFO Data
Interrupt Control												
6	***IRQMASK***	RW	--000000	-	-	IRQMASK(5:0)						IRQ Mask
7	***IRQREQUEST***	R	--------	-	-	IRQREQUEST(5:0)						IRQ Request
Interface & Pin Control												
0C	***PINCFG1***	RW	00100111	reserved		IRQZ	reserved	SYSCLK(3:0)				Pin Configuration 1
0D	***PINCFG2***	RW	11010000	reserved		IRQE	reserved	reserved		IRQI	reserved	Pin Configuration 2
0E	***PINCFG3***	R	--------	-	-	-	SYSCLKR	reserved		IRQR	reserved	Pin Configuration 3
0F	***IRQINVERSION***	RW	--000000	-	-	IRQINVERSION(5:0)						IRQ Inversion
Modulation & Framing												
10	***MODULATION***	RW	-0000010	-	MODULATION(6:0)							Modulation
11	***ENCODING***	RW	----0010	-	-	-	-	ENC MANCH	ENC SCRAM	ENC DIFF	ENC INV	Encoder/Decoder Settings

12	***FRAMING***	RW	-0000000	FRMRX	MATCHLEN(2:0)			FRMMODE(2:0)			FABORT	Framing settings
14	***PATTERN3***	RW	11111111	PATTERN(31:24)								Preamble Match Data
15	***PATTERN2***	RW	11111111	PATTERN(23:16)								Preamble Match Data
16	***PATTERN1***	RW	11111111	PATTERN(15:8)								Preamble Match Data
17	***PATTERN0***	RW	11111111	PATTERN(7:0)								Preamble Match Data
Voltage Regulator												
1B	***VREG***	R	--------	-	-	-	-	SSDS	SSREG	SDS	SREG	Voltage Regulator Status
Synthesizer												
20	***FREQ3***	RW	00111001	FREQ(31:24)								Synthesizer Frequency
21	***FREQ2***	RW	00110100	FREQ(23:16)								Synthesizer Frequency
22	***FREQ1***	RW	11001100	FREQ(15:8)								Synthesizer Frequency
23	***FREQ0***	R	10000000	FREQ(7:0)								Synthesizer Frequency
28	***IFFREQHI***	RW	00100000	IFFREQ(15:8)								2nd LO / IF Frequency
29	***IFFREQLO***	RW	00000000	IFFREQ(7:0)								2nd LO / IF Frequency
2C	***PLLLOOP***	RW	-0011101	-	reserved	BANDSEL	PLLCPI(2:0)			FLT(1:0)		Synthesizer Loop Filter Settings
2D	***PLLRANGING***	RW	00001000	STICKY LOCK	PLL LOCK	RNGERR	RNG START	VCOR(3:0)				Synthesizer VCO Auto-Ranging
FIFO, Part 2												
35	***FIFOCOUNT***	R	--------	-	-	-	FIFOCOUNT(4:0)					FIFO Fill state
36	***FIFOTHRESH***	RW	---00000	-	-	-	FIFOTHRESH(4:0)					FIFO Threshold
37	***FIFOCONTROL2***	RW	0-----00	CLEAR	-	-	-	-	-	STOPONERR(1:0)		Additional FIFO control
Receiver												
3A	***AGCATTACK***	RW	00010110	-	-	-	AGCATTACK(4:0)					AGC Attack
3B	***AGCDECAY***	RW	0-010011	reserved	–	reserved	AGCDECAY(4:0)					AGC Decay
3C	***AGCCOUNTER***	R	--------	AGCCOUNTER(7:0)								AGC Current Value
3D	***CICSHIFT***	R	-0000100	-	reserved	CICSHIFT(5:0)						CIC Shift Factor
3E	***CICDECHI***	RW	------00	-	-	-	-	-	-	CICDEC(9:8)		CIC Decimation Factor
3F	***CICDECLO***	RW	00000100	CICDEC(7:0)								CIC Decimation Factor

40	***DATARATEHI***	RW	00011010	DATARATE(15:8)								Datarate
41	***DATARATELO***	RW	10101011	DATARATE(7:0)								Datarate
42	***TMGGAINHI***	RW	00000000	TIMINGGAIN(15:8)								Timing Gain
43	***TMGGAINLO***	RW	11010101	TIMINGGAIN(7:0)								Timing Gain
44	***PHASEGAIN***	RW	00--0011	reserved		–	–	PHASEGAIN(3:0)				Phase Gain
45	***FREQGAIN***	RW	----1010	–	–	–	–	FREQGAIN(3:0)				Frequency Gain
46	***FREQGAIN2***	RW	----1010	–	–	–	–	FREQGAIN2(3:0)				Frequency Gain 2
47	***AMPLGAIN***	RW	---00110	–	–	–	reserved	AMPLGAIN(3:0)				Amplitude Gain
48	***TRKAMPLHI***	R	--------	TRKAMPL(15:8)								Amplitude Tracking
49	***TRKAMPLLO***	R	--------	TRKAMPL(7:0)								Amplitude Tracking
4A	***TRKPHASEHI***	R	--------	–	–	–	–	TRKPHASE(11:8)				Phase Tracking
4B	***TRKPHASELO***	R	--------	TRKPHASE(7:0)								Phase Tracking
4C	***TRKFREQHI***	R	--------	TRKFREQ(15:8)								Frequency Tracking
4D	***TRKFREQLO***	R	--------	TRKFREQ(7:0)								Frequency Tracking
Crystal Oscillator, Part 2												
4F	***XTALCAP***	RW	--011100	-	-	XTALCAP(5:0)						Crystal oscillator tuning capacitance
4-FSK Control												
50	***FOURFSK***	RW	-1000010	-	DEVDECAY(3:0)				FSKHALF SPEED	DEVUPDATE	FOURFSKENA	4-FSK Control
52	***FSKDMAXHI***	RW	00000000	FSKDMAX(15:8)								4-FSK Frequency Deviation
53	***FSKDMAXLO***	RW	00000000	FSKDMAX(7:0)								4-FSK Frequency Deviation
54	***FSKDMINHI***	RW	00000000	FSKDMIN(15:8)								4-FSK Frequency Deviation
55	***FSKDMINLO***	RW	00000000	FSKDMIN(7:0)								4-FSK Frequency Deviation
Misc												
72	***PLLVCOI***	RW	--000100	-	-	reserved			VCO_I[2:0]			Synthesizer VCO current **Must be set to 001**

7A	***LOCURST***	RW	00110000	LOCURST	reserved			LOCURST **Must be set to 1**
7C	***REF***	RW	--100011	-	-	reserved	REF_I[2:0]	Reference adjust
7D	***RXMISC***	RW	--110110	-	-	reserved	RXIMIX(1:0)	Misc RF settings **RXIMIX(1:0) must be set to 01**

7. Application Information

7.1. Typical Application Diagram

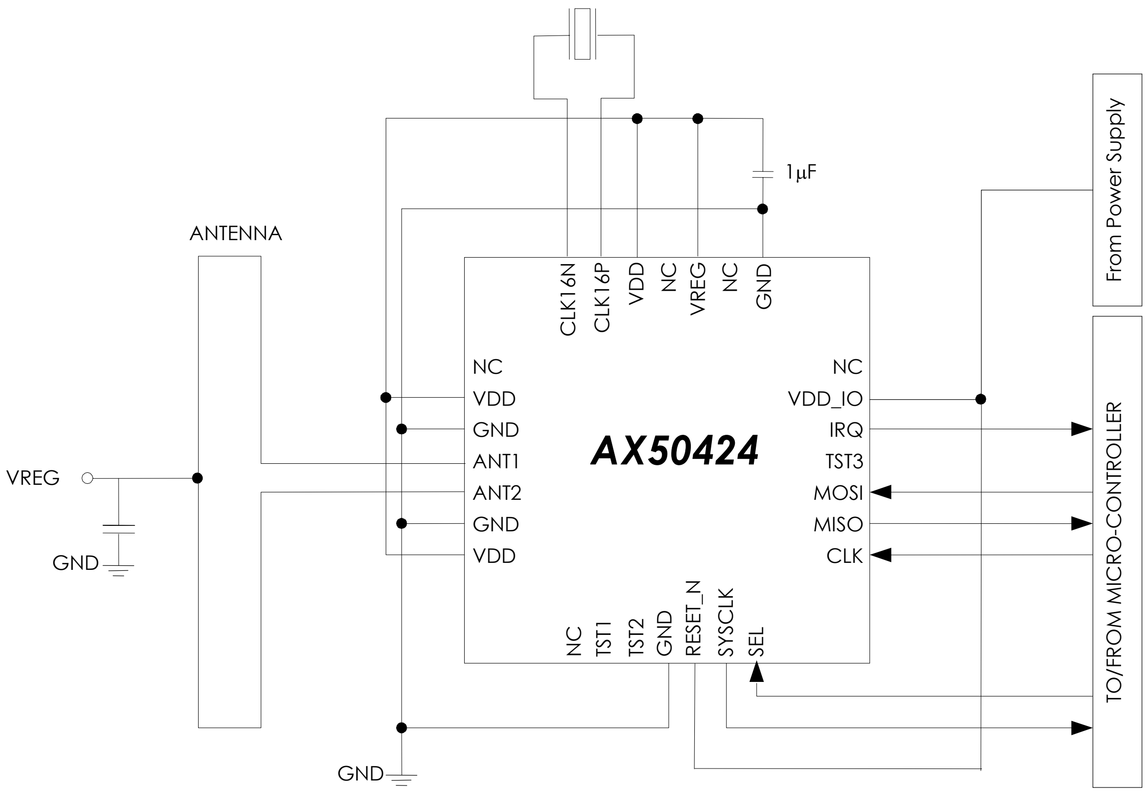


Figure 4 Typical application diagram

It is mandatory to add 1 µF (low ESR) between VREG and GND.
Decoupling capacitors are not all drawn. It is recommended to add 100 nF decoupling capacitor for every VDD and VDD_IO pin. In order to reduce noise on the antenna inputs it is recommended to add 27 pF on the VDD pins close to the antenna interface.

7.2. Antenna Interface Circuitry

The ANTP and ANTN pins provide RF input to the LNA when **AX50424** is in receive mode. A small antenna can be connected with an optional translation network. The network must provide DC power to the LNA. A biasing to VREG is necessary.

Single-Ended Antenna Interface

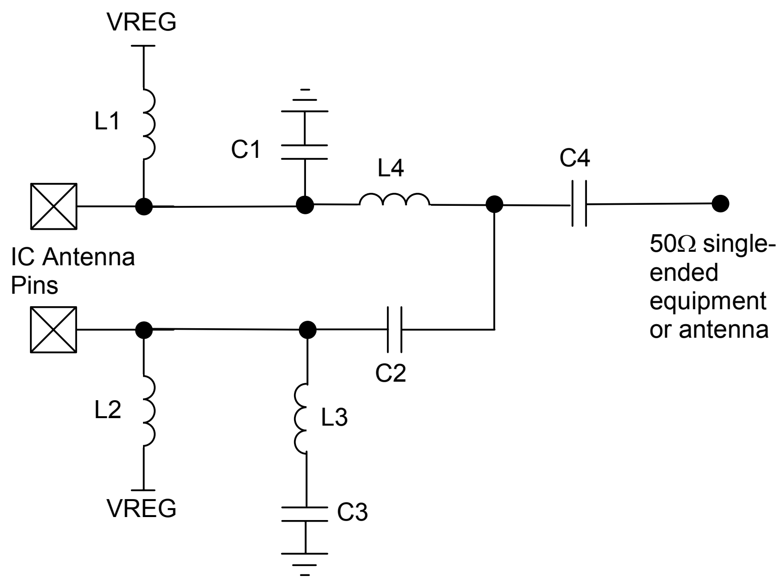


Figure 5 Structure of the antenna interface to 50Ω single-ended equipment or antenna

Frequency Band	L1=L2 [nH]	C1=C2 [pF]	L3=L4 [nH]	C3=C4 [pF]
868 / 915 MHz	18	1.8	18	220
433 MHz	33	3.3	39	220

Folded Dipole Antenna Interface

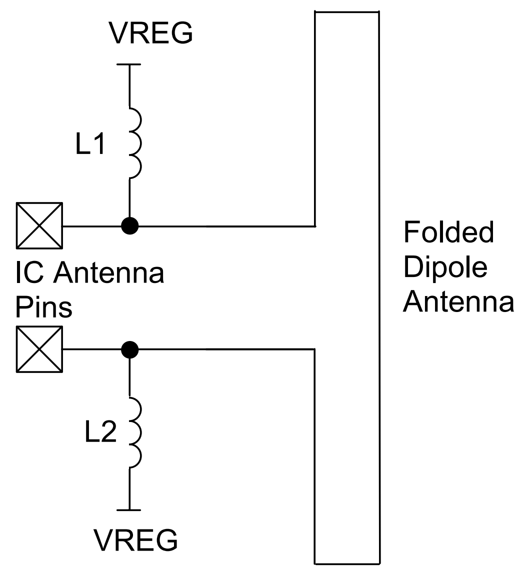


Figure 6 Structure of the antenna interface to a folded dipole antenna

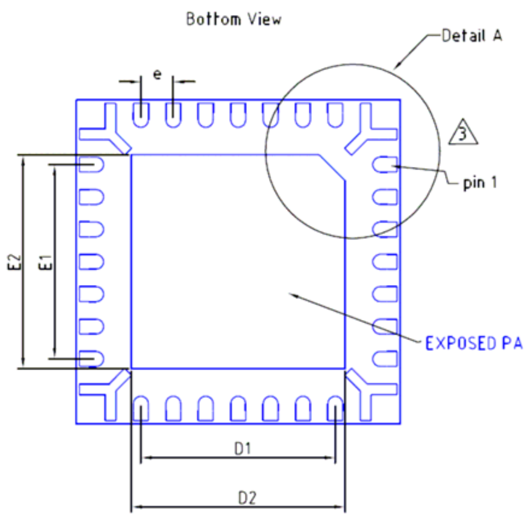
Frequency Band	L1=L2 [nH]
868 / 915 MHz	18
433 MHz	33

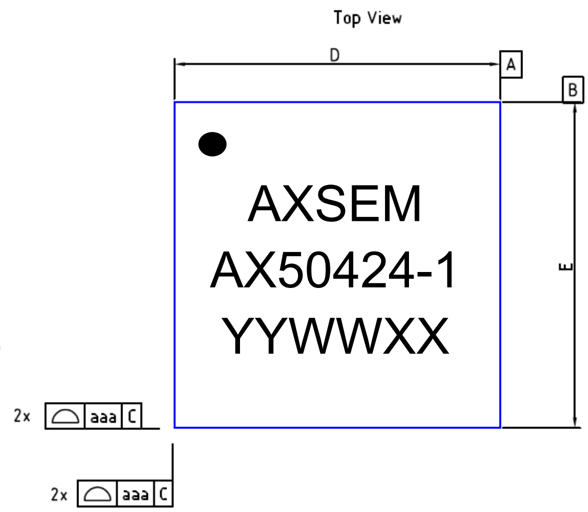
7.3. Voltage Regulator

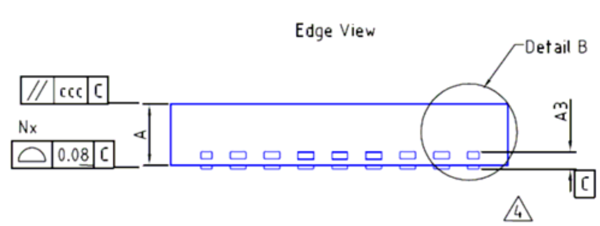
The **AX50424** has an integrated voltage regulator which generates a stable supply voltage VREG from the voltage applied at VDD_IO. Use VREG to supply all the VDD supply pins.

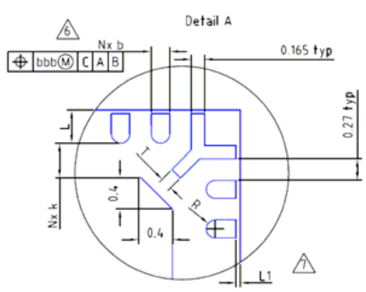
8. QFN28 Package Information

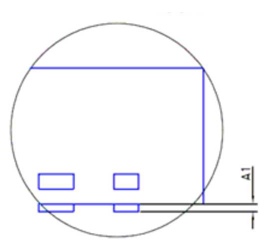
8.1. Package Outline QFN28











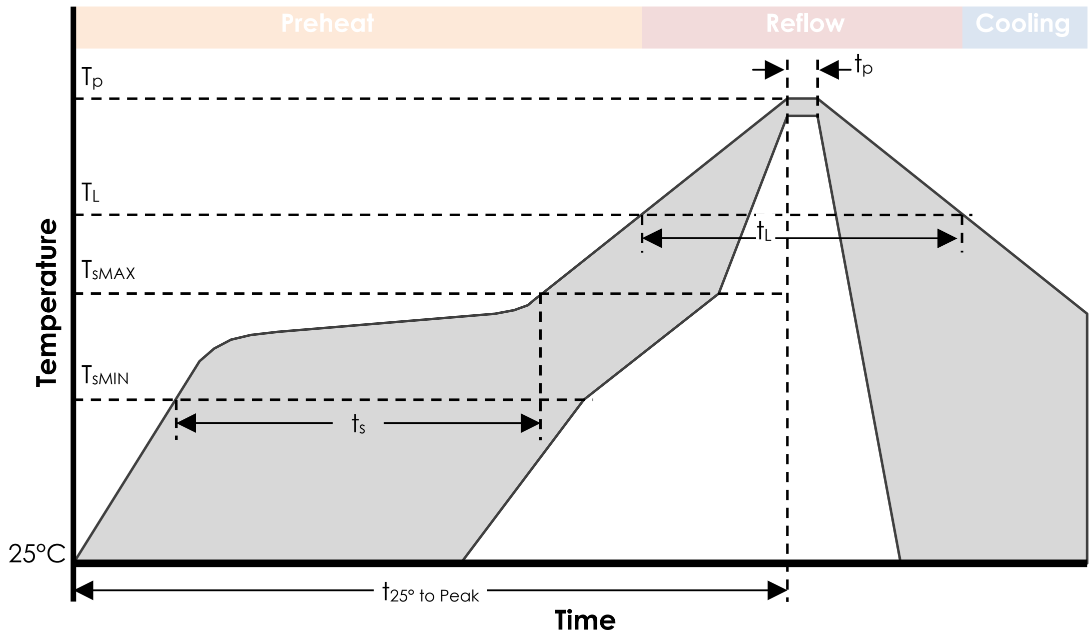
Sym.	Tolerances for Form & Position	Notes
aaa	0.15	
bbb	0.10	
ccc	0.10	

Notes

1. JEDEC ref MO-220
2. All dimensions are in millimeters
3. Pin 1 is identified by chamfer on corner of exposed die pad.
4. Datum C and the seating plane are defined by the flat surface of the metallised terminal
5. Dimension 'e' represents the terminal pitch
6. Dimension b applies to metallised terminal and is measured 0.25 to 0.30mm from terminal tip.
7. Dimension L1 represents terminal pull back from package edge. Where terminal pull back exists, only upper half of lead is visible on package edge due to half etching of leadframe.
8. Package surface shall be matte finish, Ra 1.6-2.2
9. Package warp shall be 0.050 maximum
10. Leadframe material is copper A194
11. Coplanarity applies to the exposed pad as well as the terminal
12. YYWWXX is the packaging lot code

Common Dimensions			
Sym.	Minimum	Nominal	Maximum
A	0.85	0.90	1.0
A1	0	0.02	0.05
A3		0.20 ref	
D	4.90	5.0	5.10
D1		3.00	
D2	3.20	3.30	3.40
E	4.90	5.0	5.10
E1		3.0	
E2	3.20	3.30	3.40
L	0.35	0.40	0.45
L1			0.1
b	0.18	0.23	0.30
N		28	
e		0.50	
k	0.20		
R	b min / 2		
T		0.15	

8.2. QFN28 Soldering Profile



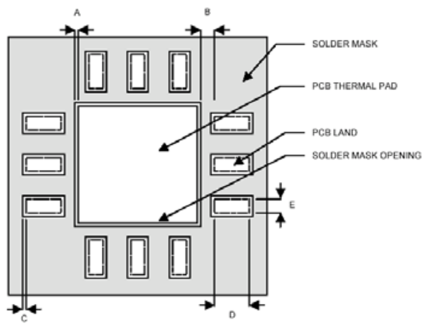
Profile Feature		Pb-Free Process
Average Ramp-Up Rate		3 °C/sec max.
Preheat Preheat		
Temperature Min	T_{sMIN}	150°C
Temperature Max	T_{sMAX}	200°C
Time (T_{sMIN} to T_{sMAX})	t_s	60 – 180 sec
Time 25°C to Peak Temperature	$T_{25\,°\,to\,Peak}$	8 min max.
Reflow Phase		
Liquidus Temperature	T_L	217°C
Time over Liquidus Temperature	t_L	60 – 150 sec
Peak Temperature	t_p	260°C
Time within 5°C of actual Peak Temperature	T_p	20 – 40 sec
Cooling Phase		
Ramp-down rate		6°C/sec max.

Notes:

All temperatures refer to the top side of the package, measured on the package body surface.

8.3. QFN28 Recommended Pad Layout

1. PCB land and solder masking recommendations are shown in Figure 7.



A = Clearance from PCB thermal pad to solder mask opening, 0.0635 mm minimum
B = Clearance from edge of PCB thermal pad to PCB land, 0.2 mm minimum
C = Clearance from PCB land edge to solder mask opening to be as tight as possible to ensure that some solder mask remains between PCB pads
D = PCB land length = QFN solder pad length + 0.1mm
E = PCB land width = QFN solder pad width + 0.1 mm

Figure 7: PCB land and solder mask recommendations

2. Thermal vias should be used on the PCB thermal pad (middle ground pad) to improve thermal conductivity from the device to a copper ground plane area on the reverse side of the printed circuit board. The number of vias depends on the package thermal requirements, as determined by thermal simulation or actual testing.

3. Increasing the number of vias through the printed circuit board will improve the thermal conductivity to the reverse side ground plane and external heat sink. In general, adding more metal through the PC board under the IC will improve operational heat transfer, but will require careful attention to uniform heating of the board during assembly.

8.4. Assembly Process

Stencil Design & Solder Paste Application

1. Stainless steel stencils are recommended for solder paste application.

2. A stencil thickness of 0.125 – 0.150 mm (5 – 6 mils) is recommended for screening.

3. For the PCB thermal pad, solder paste should be printed on the PCB by designing a stencil with an array of smaller openings that sum to 50% of the QFN exposed pad area. Solder paste should be applied through an array of squares (or circles) as shown in Figure 8.

4. The aperture opening for the signal pads should be between 50-80% of the QFN pad area as shown in Figure 9.

5. Optionally, for better solder paste release, the aperture walls should be trapezoidal and the corners rounded.

6. The fine pitch of the IC leads requires accurate alignment of the stencil and the printed circuit board. The stencil and printed circuit assembly should be aligned to within + 1 mil prior to application of the solder paste.

7. No-clean flux is recommended since flux from underneath the thermal pad will be difficult to clean if water-soluble flux is used.

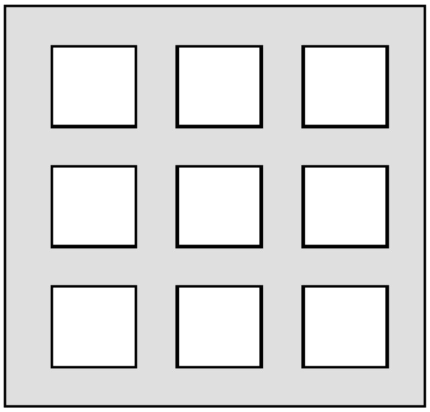


Figure 8: Solder paste application on exposed pad

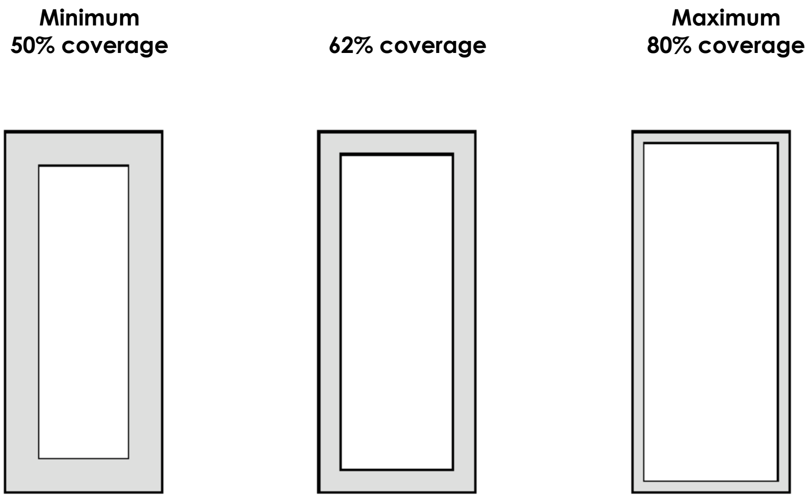


Figure 9: Solder paste application on pins

9. Life Support Applications

This product is not designed for use in life support appliances, devices, or in systems where malfunction of this product can reasonably be expected to result in personal injury. AXSEM customers using or selling this product for use in such applications do so at their own risk and agree to fully indemnify AXSEM for any damages resulting from such improper use or sale.

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