TENTATIVE

TOSHIBA RISC PROCESSOR

TMPR3927F

(32-bit RISC MICROPROCESSOR)

1. GENERAL DESCRIPTION

The TMPR3927F (to be called "TX3927" hereinafter) is a standard micro controller of the 32-bit RISC Microprocessor TX39 family. The TX3927 uses the TX39/H2 processor core as the CPU. The TX39/H2 processor core is a RISC CPU core Toshiba developed based on the R3000A architecture of MIPS Technologies, Inc. The TX3927 has built-in peripheral circuits which include memory controllers, a PCI controller, DMA controller, serial and parallel ports, and timer/counters.

2. FEATURES

❑ TX39/H2 Processor Core

- The TX39/H2 is a high-performance 32-bit microprocessor core developed by Toshiba based on the R3000A™ architecture.
- 8kbytes of Instruction cache (2-way set associative)
- 4kbytes of Data cache (2-way set associative)
- Cache support of burst refill and cache locking functions.
- Supports Critical Word First Mode
- Incorporates MMU with translation lookaside buffer (TLB)
- Single cycle, 32 x 32 bit MAC unit for DSP functions
- Built-in Debug Support Unit (DSU)

❑ SDRAM Controller

- Supports 8 channels of SDRAM, Flash (DIMM), SGRAM, or SMROM memory
- Supports 16M/64M/128M/256M bit SDRAM with 2/4 bank size availability
- Support of 16/32-bit static bus sizing on a per channel basis
- Supports Single Data Rate (SDR) SDRAM
- Supports JEDEC standard 100-pin or 168-pin DIMM sockets for SDRAM
- Supports JEDEC standard 100-pin DIMM sockets for Flash

❑ ROM Controller

- Supports 8 channels of ROM, Page Mode ROM, Mask ROM, EPROM, E^2PROM, SRAM, and Flash Memory and I/O devices.
- Supports memory sizes of 1M Byte to 1GByte per channel in 32-bit mode, and sizes of 1M Byte to 512M Byte per channel in 16-bit mode

- Supports independent per channel 32/16-bit static bus sizing

❑ **Timer/Counter**

- 3-channel 24-bit up-counter
- Interval and Watchdog timer modes
- Support of up to 3 external (multiplexed) timer output pins
- Support of external input clock

❑ **Interrupt Controller**

- Priority process of 8 internal and up to 6 external interrupt sources
- Support of Non Maskable interrupt (NMI)

❑ **PCI Controller**

- Full compliance with PCI Local Bus Specification Revision 2.1
- 32-bit PCI interface at 33MHz
- Supports both target and initiator mode
- Supports zero-wait-state read and write burst transfer for target mode
- FIFO to minimize initial latency requirements to and from memory controller
- Supports auto PCI bus to local bus address space mapping
- Arbiter function can be enabled/disabled
- External interrupt function capability

❑ **Direct Memory Access Controller (DMAC)**

- Independent 4-channel DMA
- Supports 8/16/32-bit wide I/O devices
- Supports Internal/External transfer requests
- Supports both Dual Address and Single Address transfer modes
- Support of word aligned memory to memory transfers using 4-word/8-word burst reads and writes

- **Serial I/O Ports**
  - Two-channel UART
  - Baud rate generator and modem flow control support
  - Supports 8-bit x 8 Transmitter FIFO
  - Supports 13-bit x 16 (data 8-bits and status 5 –bits) Receiver FIFO

- **Parallel I/O Ports**
  - Supports up to 16 bi-directional I/O pins that can be read regardless of direction or mode
  - Independent selection of direction of pins and choice of totem-pole or open-drain outputs
  - Support of 16-bit Flag register available as read/write register or Flag register

- Power Supply: **2.5V (internal) / 3.3V (I/O)**
- Operating Frequency: **133MHz**
- Package Type: **240-pin Plastic QFP**

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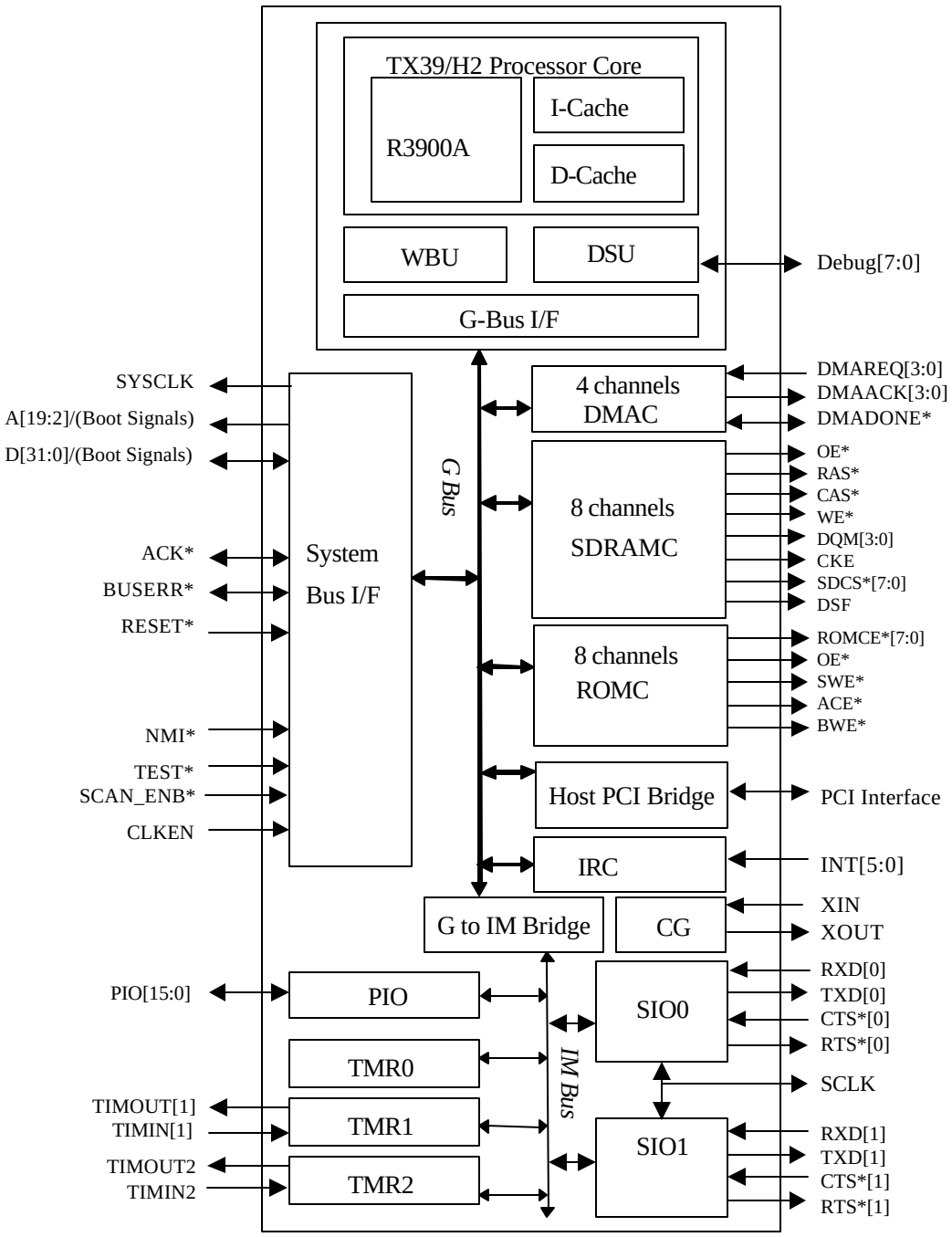
3. SYSTEM CONFIGURATION

3.1 TMPR3927F Block Diagram



*Note: This diagram shows the full set of functional signal connections. Due to pin multiplexing, not all of these signals will be available.

4. PIN DESCRIPTION

4.1 PIN OUT (240-pin PQFP)

Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
1	VSS2	31	VSS2	61	VSS	91	VSS2
2	DATA[30]	32	VSS	62	PCIAD[29]	92	DEVSEL*
3	DATA[23]	33	VDDS	63	PCIAD[28]	93	STOP*
4	DATA[31]	34	RTS*[1]	64	PCIAD[27]	94	PERR*
5	CE*[1]	35	GPCST[2]	65	VSS	95	SERR*
6	VSS	36	GPCST[1]	66	PCIAD[26]	96	PAR
7	CE*[0]	37	GPCST[0]	67	PCIAD[25]	97	C_BE[1]
8	ACE*	38	GDCLK	68	PCIAD[24]	98	VSS
9	ADDR[4]	39	GSDI	69	VSS	99	PCIAD[15]
10	ADDR[3]	40	GDRESET*	70	C_BE[3]	100	VDDS
11	ADDR[2]	41	GDBGE*	71	VDDS	101	PCIAD[14]
12	SYSCLK	42	PCICLK[3]	72	IDSEL	102	PCIAD[13]
13	VDD2	43	VDDS	73	PCIAD[23]	103	VSS
14	BWE*[3]	44	VSS	74	PCIAD[22]	104	PCIAD[12]
15	BWE*[2]	45	PCICLK[2]	75	VSS	105	PCIAD[11]
16	VSS	46	PCICLK[1]	76	PCIAD[21]	106	PCIAD[10]
17	BWE*[1]	47	PCICLK[0]	77	PCIAD[20]	107	VSS
18	BWE*[0]	48	VSS	78	PCIAD[19]	108	PCIAD[9]
19	OE*	49	GNT[3]	79	VSS	109	PCIAD[8]
20	SWE*	50	GNT[2]	80	PCIAD[18]	110	VDDS
21	SCLK	51	GNT[1]	81	PCIAD[17]	111	C_BE[0]
22	RXD[0]	52	GNT[0]	82	VDDS	112	VSS
23	TXD[0]	53	REQ[3]	83	PCIAD[16]	113	PCIAD[7]
24	RTS*[0]	54	REQ[2]	84	VSS	114	PCIAD[6]
25	CTS*[0]	55	REQ[1]	85	C_BE[2]	115	PCIAD[5]
26	RXD[1]	56	REQ[0]	86	FRAME*	116	VSS
27	TXD[1]	57	PCIAD[31]	87	IRDY*	117	PCIAD[4]
28	CTS*[1]	58	PCIAD[30]	88	VSS	118	PCIAD[3]
29	GSDAO[0]	59	VSS2	89	TRDY*	119	PCIAD[2]
30	VDD2	60	VDDS	90	VDD2	120	VDDS

Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
121	VSS	151	VSS2	181	VSS2	211	VSS2
122	PCIAD[1]	152	DATA[12]	182	XIN	212	SDCS*[0]
123	PCIAD[0]	153	VSS	183	XOUT	213	SDCS*[1]
124	ACK*	154	DATA[5]	184	VDD2	214	SDCS_CE*[2]
125	DMAREQ[3]	155	DATA[13]	185	VDD2	215	SDCS_CE*[3]
126	DMAACK[3]	156	DATA[6]	186	PLLVDD	216	SDCS_CE*[4]
127	DMAREQ[2]	157	DATA[14]	187	FILTER[0]	217	SDCS_CE*[5]
128	DMAACK[2]	158	DATA[7]	188	FILTER[1]	218	VDDS
129	DMAREQ[0]	159	VDDS	189	PLLVSS	219	DMAACK[1]
130	VSS	160	DATA[15]	190	VSS2	220	DMAREQ[1]
131	VDDS	161	VSS	191	NMI*	221	DQM[2]
132	DMAACK[0]	162	DQM[0]	192	SCANENB*	222	VSS
133	DMADONE*	163	DQM[1]	193	CLKEN	223	DQM[3]
134	INT[3]	164	ADDR[5]	194	RESET*	224	DATA[16]
135	INT[2]	165	ADDR[6]	195	TEST*	225	DATA[24]
136	INT[1]	166	ADDR[7]	196	ADDR[18]	226	DATA[17]
137	INT[0]	167	ADDR[8]	197	ADDR[19]	227	DATA[25]
138	PIO[0]	168	VSS	198	RAS*	228	DATA[18]
139	DATA[0]	169	ADDR[9]	199	VSS	229	VSS
140	DATA[8]	170	VDDS	200	CAS*	230	VDDS
141	DATA[1]	171	ADDR[10]	201	SDCLK[0]	231	DATA[26]
142	DATA[9]	172	ADDR[11]	202	SDCLK[1]	232	DATA[19]
143	VSS	173	ADDR[12]	203	SDCLK[2]	233	DATA[27]
144	DATA[2]	174	ADDR[13]	204	VDDS	234	DATA[20]
145	DATA[10]	175	ADDR[14]	205	SDCLK[3]	235	DATA[28]
146	DATA[3]	176	VSS	206	SDCLK[4]	236	DATA[21]
147	VDDS	177	ADDR[15]	207	VSS	237	VSS
148	DATA[11]	178	ADDR[16]	208	CKE	238	DATA[29]
149	DATA[4]	179	ADDR[17]	209	WE*	239	DATA[22]
150	VDD2	180	VDDS	210	VDD2	240	VDDS

* Active-low signal

5. PIN FUNCTION

Name of Signal	I/O	Function
System Interface		
SYSCLK	O	System Clock Outputs a system clock with frequencies for full or half-speed bus mode depending upon programmed configuration captured at RESET*.
DATA[31:0]	I/O	32-bit external data bus During RESET*, the state of DATA[6:0] are used to set the configuration of the TX3927. DATA[6:0] are propagated through a transparent latch and are captured on the rising edge of RESET*. Signal is connected to internal pull-up resistor.
ACK*	I/O	Acknowledge Signifies that there is valid data on the data bus or that a data transfer has been made. Can be driven by the TX3927 or external devices. Signal is connected to internal pull-up resistor.
RESET*	I	Reset Initializes the TX3927. RESET* signal must remain low for a minimum of 256 SDCLK cycles to effect a valid reset. Signal is connected to internal pull-up resistor.

Clock Signals		
XIN	I	Crystal Input Input from a crystal oscillator at 1/1, 1/2, or 1/4 of the core frequency; or input from an external crystal at 1/16 of the core frequency.
XOUT	O	Crystal Output Asserted high if an external clock source is selected, or attached to an external crystal with a frequency of 1/16 of the core frequency.
CLKEN	I	Clock Enable Enables internal clock generator. Should be asserted via external logic when V_{dd} reaches minimum specification and XIN has started and is stable. Signal is connected to internal pull-up resistor.

Interrupt Signals		
NMI*	I	Non Maskable Interrupt Non-Maskable interrupt input. Signal is connected to internal pull-up resistor.
INT[5:4]	I	INT [5:4] multiplexed with CTS0/RTS0
INT[3:0]	I	Interrupt Requests Signal is connected to internal pull-up resistor.

Timer Interface		
TIMER[1:0]	O	Timer Pulse Width Output Multiplexed with other functions. DMAREQ[3]/PIO15/TIMER[1] DMAACK[3]/PIO14/TIMER[0] DMADONE/PIO7/TIMER[0]

Memory Interface		
SDCLK[4:0]	O	SDRAM Controller Clock Signal is connected to internal pull-up resistor.
RAS*	O	Row Address Strobe RAS* signal for the access of all synchronous memory devices.
CAS*	O	Column Address Strobe CAS* signal for the access of all synchronous memory devices.
SDCS*[7:0]	O	Synchronous Memory Device Chip Select Chip select for synchronous memory devices and 100-pin DIMM Flash. SDCS[7:2] are shared with ROMCE[7:2] and are assigned by software. SDCS[7:6] are also shared with DMA REQ/ACK[1] and PIO[11:10] via software assignment.
DQM[3:0]	O	Data Mask During a write cycle, the DQM signal functions as a Data Mask and can control every byte of the input data for SDRAMs. During a read cycle, the DQM functions as the control of the SDRAM output buffers. The DQMs also function as byte write enables to DIMM Flash during a write cycle.
WE*	O	Write Enable Write enable signal for access of synchronous memory devices.
CKE	O	Clock Enable Used for synchronous memory devices.

ACE*	O	ROM Address Clock Enable Enables capture of upper ten bits (multiplexed address) in an external latch. Used with ROM, SRAM, and peripheral I/O. (Only active if next upper address differs from the prior value.)
SWE*	O	Static RAM Write Enable (Used in conjunction with ROM Controller)
ADDR[19:2]	O	Addresses for all memory devices (During RESET*, the state of these pins are used to set the configuration of the TX3927. Pin states are propagated through a transparent latch and are captured on the rising edge of RESET*.) Signal is connected to internal pull-up resistor.
OE*	O	Output Enable Output enable for all devices controlled by the ROM Controller and for SMROM and DIMM Flash.
CE*[7:0]	O	ROM Chip Enable Chip selects to ROM, SRAM, FLASH and peripheral devices. Shared with SDRAM SDCS*[7:2] via software assignment. Signals connected to internal pull-up resistors.
BWE*[3:0]	O	Data Byte Write Enable Can be Byte write enables or Byte enables during a ROMC cycle.
DSF	O	Define Special Function Multiplexed with PIO[1] and used for SGRAM special register functions.

PCI Interface		
PCIAD[31..0]	I/O	The 32 Bit Address and Data Buses are multiplexed on the same PCI pins.
C_BE[3..0]	I/O	Command and Byte Enable
PAR	I/O	Parity for PCIAD[31..0] and C_BE[3..0]. Even Parity
FRAME*	I/O	Indicates beginning and duration of an transaction.
TRDY*	I/O	Target ready
IRDY*	I/O	Initiator ready
STOP*	I/O	STOP* indicates that the current Target is requesting Initiator to stop the current transaction.
DEVSEL*	I/O	Device select Indicates that an active device has decoded its address as the target of the current access.

REQ*[3:0]	I/O	Request PCI bus In internal arbiter mode, REQ*[3:0] are inputs. In external arbiter mode, REQ*[0] is an output, REQ*[1] is an interrupt output, and REQ*[3:2] are unused.
GNT*[3:0]	I/O	Grant PCI bus In internal arbiter mode, GNT*[3:0] are outputs. In external arbiter mode, GNT*[0] is an input and GNT*[3:1] are unused.
PCICLK[3:0]	I/O	PCICLK[0] becomes input when PCICLKEN is disabled. PCICLK[3:1] are tri-state outputs.
PERR*	I/O	Data Parity Error Reports parity error on all transactions except Special Cycle command.
ID_SEL	I	Initialization Device select Used as chip select during configuration read/write transaction on PCI bus.
SERR*	I/O	System Error Reports errors for all address parity errors and data parity error on Special Cycle commands, and may optionally be used to report any other non-parity or system errors.

DMA Interface		
DMAREQ[3:0]	I	DMA Request DMA request from an external device. Signals are software assigned and shared with PIO/TIMER and SDCS_CE[7] functions. Signal is connected to internal pull-up resistor.
DMAACK[3:0]	O	DMA Acknowledge DMA acknowledge to external devices. Signals are software assigned and shared with PIO/TIMER and SDCS_CE[6] functions. Signal is connected to internal pull-up resistor.
DMADONE*	I/O	DMA Transfer/Chain Finished Signal is connected to internal pull-up resistor.

SIO Interface		
CTS*[1:0]	I	SIO Clear to Send Signals are software assigned and shared with PIO/INT and serial debug GSDAO[1] functions. Signal is connected to internal pull-up resistor.
RTS*[1:0]	O	SIO Request to Send Signals are software assigned and shared with PIO/INT and serial debug GPCST[3] functions. Signal is connected to internal pull-up resistor.
RXD[1:0]	I	SIO Receive Data Signals are multiplexed with PIO/INT functions. Signal is connected to internal pull-up resistor.
TXD[1:0]	O	SIO Transmit Data Signals are multiplexed with PIO/INT functions. Signal is connected to internal pull-up resistor.
SCLK	I	External Serial Clock Signal is connected to internal pull-up resistor.

PIO Interface		
PIO[15:0]	I/O	PIO Ports All PIO signals, except 0, are shared with either DMA, INT, TIMER, Debug, or SIO functions. PIO[1] is shared with DSF, an SGRAM memory function. PIO[0] is connected to internal pull-up resistor.

Debug Interface		
GDCLK	O	Debug Clock Signal This is the clock output for the real-time debugging system. The serial monitor bus and PC trace interface signals all have their timings regulated by this debug clock. During serial monitor bus operation, this clock is half the frequency of the TX39/H2 core operating clock.
GSDAO[1:0]	O	Serial Data and Address Output/Target PC These signals function as serial data/address outputs when operating with the serial monitor bus interface or as debug interrupt input when operating with the PC trace interface.

GPCST[3:0]	O	PC Trace Status Outputs PC trace status information and serial monitor bus mode.
GDRESET*	I	Debug Reset A reset input for the real-time debugging system. When this signal is asserted, the debug support unit (DSU) is initialized. Signal is connected to internal pull-up resistor.
GDBGE*	I	Debugger Enable Indicates whether a real-time debugging system is connected external to the TX39/H2 core. This signal must be low when a real-time debugging system is connected or high when not connected. When DBGE* = high, the clock supplied to the DSU block is stopped. Signal is connected to internal pull-up resistor.
GSDI*	I	Serial Data Input/ Debug Interrupt This signal functions as serial data/address input when operating with the serial monitor bus interface or as target PC input when operating with the PC trace interface. Signal is connected to internal pull-up resistor.

Others		
TEST*	I	Test Pin This signal is used as internal functional test. It should be set to high. Signal is connected to internal pull-up resistor.
SCAN_ENB*	I	Scan Mode Test Control This signal is used as internal functional test. It should be set to high. Signal is connected to internal pull-up resistor.

Power pins and Total pin count		
PLL_VSS, PLL_VDD	I	Power and Ground pins to internal PLL circuit.
VDD2	I	Power pins at 2.5V
VDDS	I	Power pins at 3.3V
VSS2,VSS	I	Ground pins
Total Pin Count		**Pins: 240 pins**

6. ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DDS}	-0.3 ~ 4.5	V
	V_{DD2}	-0.3 ~ 3.6	
Input voltage RXD[1:0], CTS[1:0], PCIAD[31:0], PCICLK[3:0], GNT[3:0], REQ[3:0], C_BE[3:0], IDSEL, FRAME*, IRDY*, TRDY*, DEVSEL*, STOP*, PERR*, SERR*, PAR	V_{IN1}	-0.3 ~ 6.7V	V
Other inputs	V_{IN2}	-0.3 ~ V_{DDS} + 0.3V	V
Storage temperature	T_{STG}	-40 ~ 125	°C
Maximum power dissipation	P_D	2.0	W

Note: The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any absolute maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in possible injury to the user. Thus, when designing products which include this device, ensure that no absolute maximum rating will ever be exceeded.

6.2 Recommended Operating Conditions

Parameter		Symbol	Condition	Min.	Max.	Unit
Supply voltage	I/O	V_{DDS}		3.0	3.6	V
	Internal	V_{DD2}		2.3	2.7	V
Operating case temperature		T_C		0	70	°C

Note: The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device, is used under conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC and DC values, etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

6.3 DC Characteristics

6.3.1 DC characteristics of pins other than PCI interface pins

(T_c = 0 ~ 70°C, V_{DDS} = 3.3V±0.3V, V_{DD2} = 2.5V±0.2V, V_{SS} = 0V)

Parameter	Symbol	Condition	Min.	Max.	Unit
Low-level input voltage	V_{IL1} V_{IL2}	RXD[1:0], CTS[1:0] RXD[1:0], CTS[1:0]		V_{DD} × 0.2 0.8	V
High-level input voltage	V_{IH1} V_{IH2}	RXD[1:0], CTS[1:0] RXD[1:0], CTS[1:0]	V_{DDS} × 0.8 2.0	V_{DDS} × 0.3 5.5	V
Low-level output current	I_{OL1} I_{OL2}	(1) V_{OL} = 0.4V (2) V_{OL} = 0.4V		8 16	mA mA
High-level output current	I_{OH1} I_{OH2}	(1) V_{OH} = 2.4V (2) V_{OH} = 2.4V	-8 -16		mA mA
Operating current I/O Internal	 I_{DDS} I_{DD2}	 (3) f=133MHz, V_{DDS} = 3.6V (3) f=133MHz, V_{DDS} = 2.7V		 120 420	 mA mA
Input leakage current	I_{IH} I_{IL}		-10 -10	10 10	µA µA
Pullup Resistor	RST		50	300	kΩ

(1) : Other signals, Excluding (2)

(2) : ADDR[19:5], SDCLK[4:0], DQM[3:0], DATA[31:0], CAS*, RAS*, CKE, WE*, OE*, SYSCLK, GDCLK, ACK*

(3) f: CPU frequency

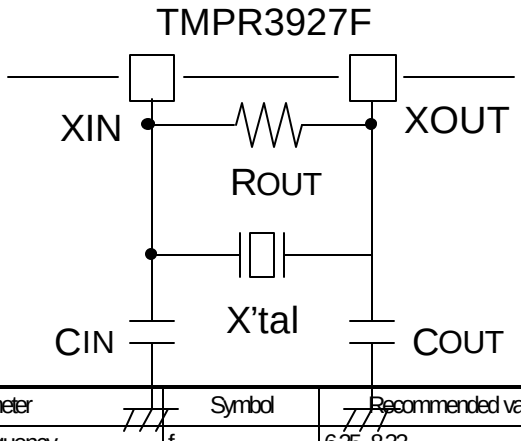
6.3.2 DC characteristics of PCI interface pins

(T_c = 0 ~ 70°C, V_{DDS} = 3.3V±0.3V, V_{DD2} = 2.5V±0.2V, V_{SS} = 0V)

Parameter	Symbol	Condition	Min.	Max.	Unit
Low-level input voltage	V_{IL3}		-0.5	V_{DDS} x 0.3	V
High-level input voltage	V_{IH3}		V_{DDS} x 0.5	5.5	V
Output High Voltage	V_{OH}	I_{OUT} = -2mA	V_{DDS} x 0.9		V
Output Low Voltage	V_{OL}	I_{OUT} = 3mA, 6mA		V_{DDS} x 0.1	V
Input leakage current	I_{IH} I_{IL}	0 < V_{IN} < 5V	-10 -10	10 10	μA μA

6.4 Crystal Oscillator Characteristics

6.4.1 Recommended oscillator conditions



Parameter	Symbol	Recommended value	Unit
Crystal Oscillator frequency	f_{IN}	6.25~8.33	MHz
Output register	R_{OUT}	10	MΩ
External condenser	C_{IN}, C_{OUT}	12	pF
Clock generator Rising time Falling time	 t_r t_f	 5(1) 5(1)	 ns ns

(1) For a reference. Ask clock generator manufacture.

6.4.2 Recommended input clock conditions (when 2-multiply)

Parameter	Symbol	Recommended Value	Unit
Input Clock Frequency	f_{IN}	50 ~ 66.67	MHz

Note: When 2-multiply, the external clock should input to the XIN pin. Then the XOUT pin must be left open.

6.4.3 Electrical characteristics

(T_c = 0 ~ 70°C, V_{DDS} = 3.3V±0.3V, V_{DD2} = 2.5V±0.2V, V_{SS} = 0V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Oscillation start time	t_{STA}	f=6.25~8.75MHz	-	1	10	ms

6.5 PLL Filter Circuit

The following filter circuit is recommended for the PLL filter using the pins LP (Filter0) and AGS (Filter1).

Filter0 Filter1

Symbol	Symbol	Recommended Value	Unit
External Capacitor	C_{Filter}	1800 (using 16x divider)	pF
		220 (using 2x divider)	pF

6.6 AC Characteristics (of pins other than PCI interface pins)

6.6.1 Table of AC characteristics

(T_c = 0 ~ 70°C, V_{DDS} = 3.3V±0.3V, V_{DD2} = 2.5V±0.2V, V_{SS} = 0V, CL = 50pF)

Symbol	Signal	Description	Min	Max	Unit
t_{sys}	SYSCLK/SDCLK[4:0]	Cycle Time	15		ns
t_{sysh}	SYSCLK	Cycle Time (Half-speed bus mode)	30		ns
t_{sysm}	SYSCLK/SDCLK[4:0]	Min High/Low Level	5		ns
t_{sysmh}	SYSCLK	Min Half-Speed High/Low Level	12		ns
t_d	(1)	Output Delay		7	ns
t_{oh}	(1)	Output Hold	1		ns
t_{su}	(2)	Input Setup	7		ns
t_{ih}	(2)	Input Hold	0		ns
t_{daz}	DATA[31:0], ACK*	Data Active to Hi-Z		7	ns
t_{dza}	DATA[31:0], ACK*	Data Hi-Z to Active	1		ns

(1) ACK*, DATA[31:0], ROMCE[7:0]*, OE*, ACE*, SWE*, BWE[3:0]*, ADDR[19:2], DMAACK[3:0], DMADONE*, PIO[15:0], TIMER[1:0]

(2) ACK*, DATA[31:0], NMI*, INT[5:0], DMAREQ[3:0], DMADONE*, PIO[15:0]

6.6.2 SDRAM Interface AC characteristics

(T_c = 0 ~ 70°C, V_{DDS} = 3.3V±0.3V, V_{DD2} = 2.5V±0.2V, V_{SS} = 0V, CL = 50pF for SDCLK[4:0

			50pF		100pF		150pF		
Symbol	Signal	Description	Min	Max	Min	Max	Min	Max	Unit
t_{sdclk}	SDCLK[4:0]/SYSCLK	Cycle Time	15		15		15		ns
t_{sdclkm}	SDCLK[4:0]/SYSCLK	Minimum High/Low Level	5		5		5		ns
t_{sd}	[3]	Output Delay		7		8		9	ns
t_{sdd}	DATA[31:0]	Output Delay		8		10		12	ns
t_{soh}	[4]	Output Hold	1		1		1		ns
t_{ssu1}	DATA[31:0]	Input Setup (Internal clock)	7		7		7		ns
t_{ssu2}	DATA[31:0]	Input Setup (Pin feed-back clock)	2		2		2		ns
t_{sih}	DATA[31:0]	Input Hold	0		0		0		ns
t_{sdaz}	DATA[31:0]	Data Active to Hi-Z		7		7		7	ns
t_{sdza}	DATA[31:0]	Data Hi-Z to Active	1		1		1		ns

(3) SDCS[7:0], RAS*, CAS*, WE*, CKE, OE*, DSF, ADDR[19:5], DQM[3:0]

(4) SDCS[7:0], RAS*, CAS*, WE*, CKE, OE*, DSF, ADDR[19:5], DQM[3:0], DATA[31:0]

6.7 AC Characteristics (of PCI interface pins)

6.7.1 AC characteristics table

(PCI_CLK speed = 33MHz, Tc = 0 ~ 70°C, V_{DD} = 5.0V ± 0.25V, V_{SS} = 0V, C_L = 50pF)

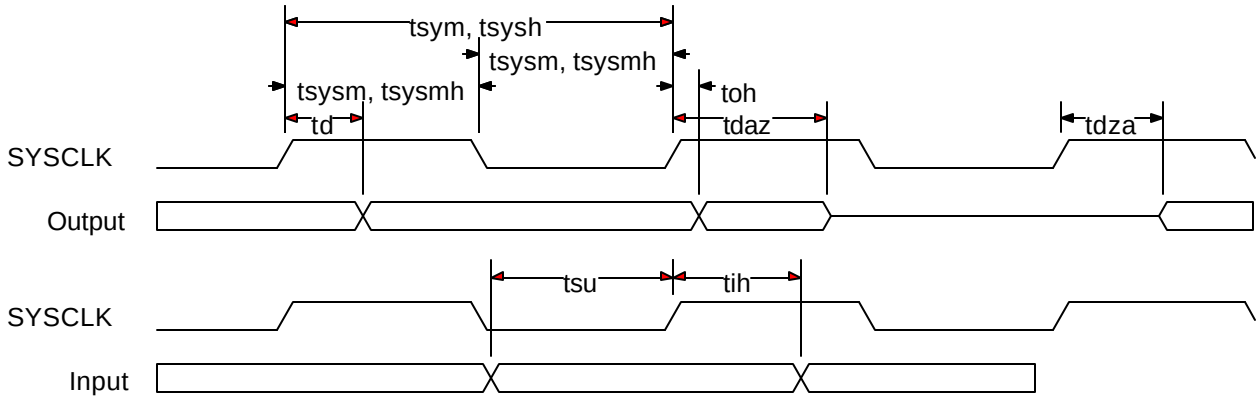
Symbol	Signal	Description	Min.	Max.	Unit
t_{cyc}		PCI_CLK cycle time	30		ns
t_{high}		PCI_CLK high time	11		ns
t_{low}		PCI_CLK low time	11		ns
-		PCI_CLK slew rate	1	4	V/ns
t_{val}		PCI_CLK to signal valid delay - bused signals	2	11	ns
$t_{val(ptp)}$		PCI_CLK to signal valid delay - point to point signals	2	12	ns
t_{on}		Float to active delay	2		ns
t_{off}		Active to float delay		28	ns
t_{su}		Input set up time to PCI_CLK - bused signals	7		ns
$t_{su(ptp)}$		Input set up time to PCI_CLK - point to point signals	12		ns
t_h		Input hold time from PCI_CLK	0		ns
t_{rst}		Reset active time after power stable	1		ms
$t_{rst-clk}$		Reset active time after PCI_CLK stable	100		us
$t_{rst-off}$		Reset active to output float delay		40	ns

Symbol	Parameter	Condition	Min.	Max.	Unit
$I_{OH\ (AC)}$	Switching Current High	$0 < V_{out} \leq 1.4$	-44	0.8	mA
		$1.4 < V_{out} < 2.4$	$-44+(V_{out}-1.4)/0.024$		mA
		$3.1 < V_{out} < V_{cc}$		Eqt'n A	
	(Test Point)	$V_{out} = 3.1$		-142	mA
$I_{OL\ (AC)}$	Switching Current Low	$V_{out} \geq 2.2$	95		mA
		$2.2 > V_{out} > 0.55$	$V_{out} / 0.023$		mA
		$0.71 > V_{out} > V_{cc}$		Eqt'n B	
	(Test Point)	$V_{out} = 0.71$		206	mA
I_{CL}	Low Clamp Output	$-5 < V_{in} \leq -1$	$-25+(V_{in}+1)/0.015$		mA
$slew_r$	Output Rise Slew Rate	0.4V to 2.4V load	1	5	V/ns
$slew_f$	Output Fall Slew Rate	2.4V to 0.4V load	1	5	V/ns

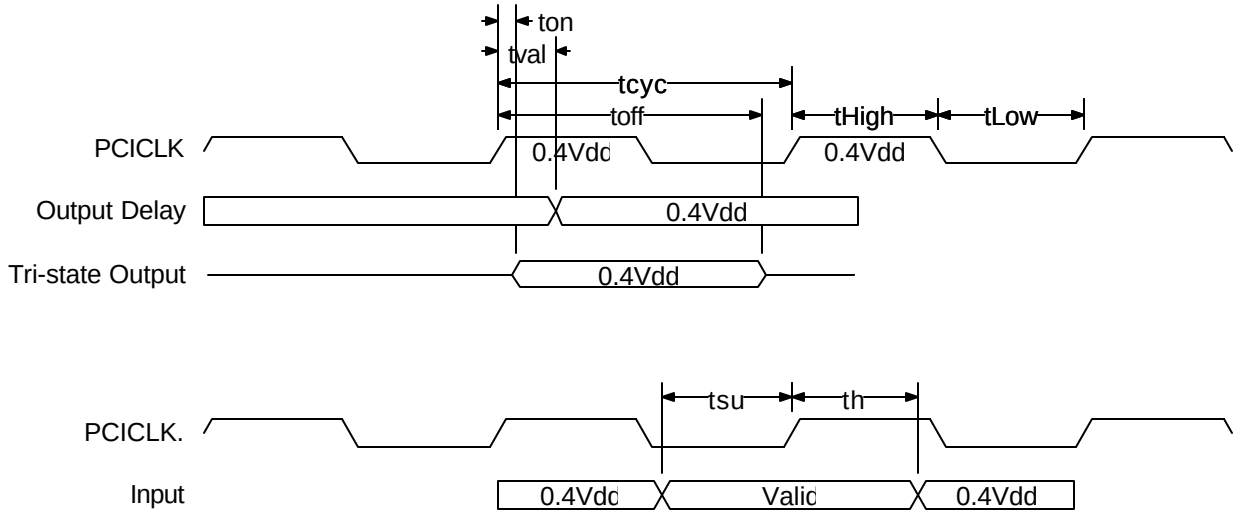
Please refer to the PCI Local Bus Specification Revision 2.2 for more information.

6.8 Timing Diagrams

6.8.1 Definition of AC characteristics

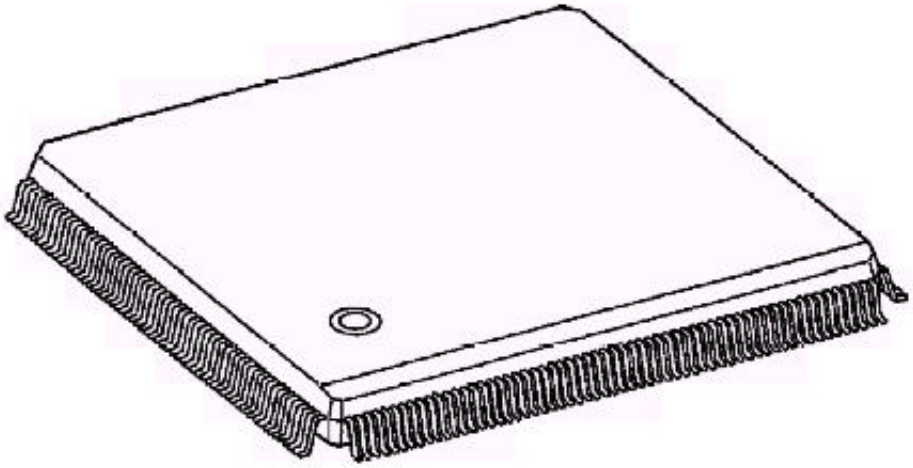


6.8.2 Definition of AC characteristics (of PCI pins)



7. PACKAGE DIMENSION

QFP240-P-3232-0.5 Unit: mm



TENTATIVE

QFP240-P-3232-0.5 Unit: mm