

## TOSHIBA RISC PROCESSOR

## TMPR4955AF-200 (TX4955A)

(64-bit RISC MICROPROCESSOR)

## 1. GENERAL DESCRIPTION

The TMPR4955AF is a 64-bit RISC (Reduced Instruction Set Computer) microprocessor that is a low-cost, low-power microprocessor developed for interactive consumer applications including set-top terminals, LBP(Laser Beam Printer), and video games.

## 2. FEATURES

- True 64-bit microprocessor, with TX49/H2 core.
- Optimized 5-stage pipeline
- 32-bit System Address/Data bus
- Single or double-precision Floating-Point Operation
- 32-bit physical address space and 64-bit virtual address space.
- 32-bit SysAD bus interface with R4000/R4400/R5000 or TX4300 compatible protocol
- On-chip 32-Kbyte Instruction Cache and 32-Kbyte Data Cache.
- Low power consumption
  - 3.3 /1.5V Dual power supply (I/O:3.3V,Internal:1.5V)
  - Reduced power mode (Halt)
- Data cache prefetching
- Memory management unit
  - contains 48-double entry JTLB, 2-entry Instruction TLB, and 4-entry Data TLB
- Software compatibility with all MIPS processors
  - MIPS I, II, and III Instruction Set Architecture (ISA)
- EJTAG (Enhanced JTAG) debug support
- Maximum operating frequency
  - Internal:200MHz External:100MHz
- Package : 160-pin QFP

●The information contained herein is subject to change without notice.

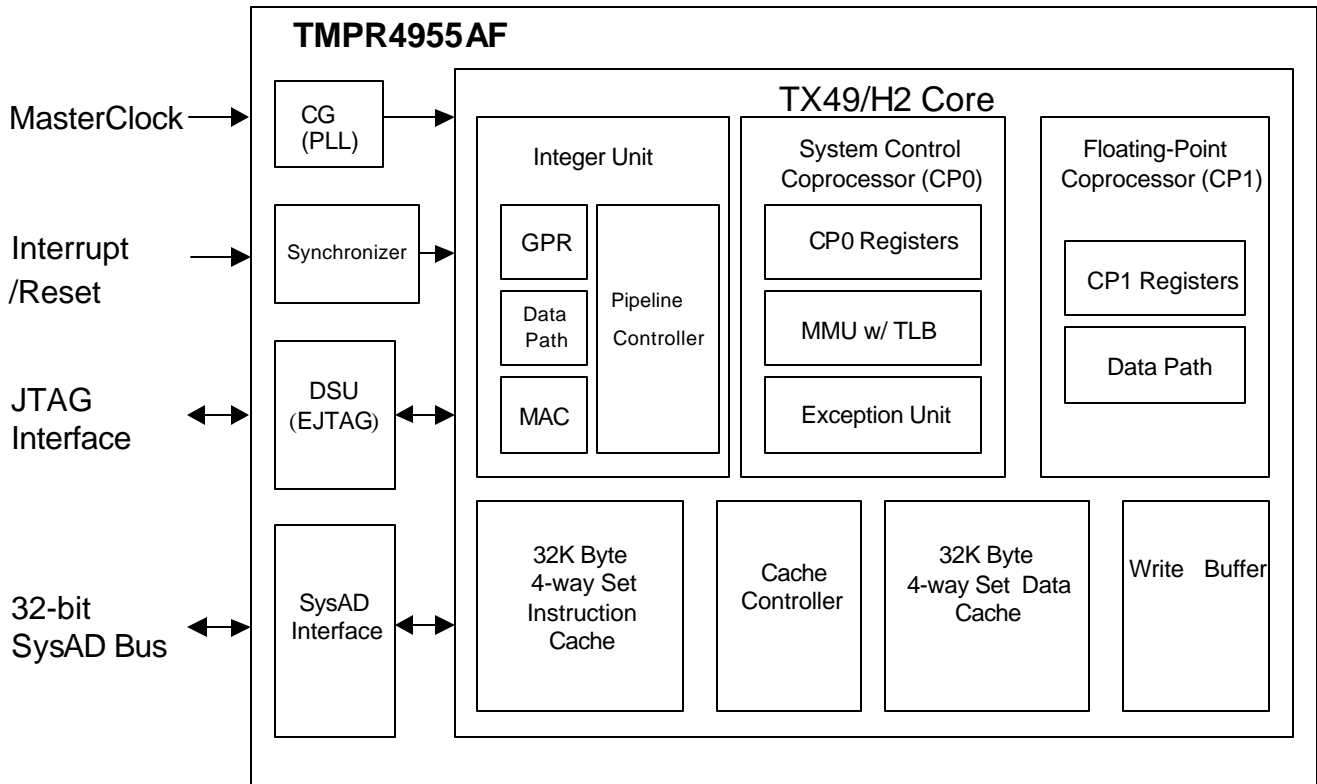
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### 3. SYSTEM CONFIGURATION

#### 3.1 TMPR4955AF BLOCK DIAGRAM



## 3.2 BLOCK FUNCTION

### □ TX49/H2 Core

- True 64-bit microprocessor
- 32, 64-bit integer general purpose registers
- 32, 64-bit floating point general purpose registers
- Optimized 5-stage pipeline
- Instruction Set

Upward compatible with MIPS I, MIPS II, MIPS III ISA

MAC (Multiply and Accumulate) instructions

PREF (Prefetch) instruction

- On-chip 32-Kbyte Instruction Cache and 32-Kbyte Data Cache  
4-way set associative and Lock function support  
Data Cache: Write-back and Write-through support
- MMU  
32-bit physical address space and 64-bit virtual address space  
48-double-entry (even/odd) Joint TLB  
2-entry Instruction TLB and 4-entry Data TLB
- IEEE754 compatible single and double precision FPU
- Debug Support Unit (DSU) with EJTAG support
- Power management modes ( HALT/DOZE )

### □ SysAD BUS I/F

- Bus protocol conversion  
It converts TMPR4955AF Internal GBus Read/Write request into outside SysAD Bus protocol.
- Output buffer level selectable

### □ Synchronizer

- The external interrupt  
It takes contents of interrupt register and bitwise OR of external interrupt signal (INT(5:0)).

### □ Clock Generator

- Generates the internal operating clock of the TMPR4955AF from external crystal oscillator.

### □ Debug Support Unit (DSU)

- EJTAG function support  
Consists of an Enhanced JTAG (EJTAG) Module and a Debug Support Unit (DSU). It can be used to provide single-step execution and hardware break-points for debugging processor systems. EJTAG utilizes JTAG interface and extends the ability to access the inside register contents, host system peripherals, and system memory.

## 4. PIN DESCRIPTION

### 4.1 PIN OUT (160-pin QFP)

1	Vss	41	Vss	81	Vcclnt	121	SysAD28
2	BufSel1	42	TRST*	82	NMI*	122	SysAD29
3	JTDO	43	RdRdy* / (GND)	83	ExtRqst* / (Ereq*)	123	Vcclnt
4	JTDI	44	WrRdy* / (EOK*)	84	Reset*	124	Vss
5	JTCK	45	ValidIn* / (Evalid*)	85	ColdReset*	125	SysAD30
6	JTMS	46	ValidOut* / (Pvalid*)	86	VcclO	126	VcclO
7	VcclO	47	Release* / (PMaster*)	87	Endian	127	Vss
8	Vss	48	VcclO	88	VcclO	128	SysAD31
9	SysAD4	49	PLLReset*	89	Vss	129	SysADC2/ (GND)
10	SysAD5	50	Vcclnt	90	SysAD16	130	Vcclnt
11	Vcclnt	51	TintDis	91	Vcclnt	131	Vss
12	Vss	52	Vss	92	Vss	132	SysADC3/ (GND)
13	SysAD6	53	SysCmd0	93	SysAD17	133	VcclO
14	VcclO	54	SysCmd1	94	SysAD18	134	Vss
15	Vss	55	SysCmd2	95	VcclO	135	SysADC0/ (GND)
16	SysAD7	56	SysCmd3	96	Vss	136	Vcclnt
17	SysAD8	57	SysCmd4	97	SysAD19	137	Vss
18	Vcclnt	58	SysCmd5 / (GND)	98	Vcclnt	138	SysADC1/ (GND)
19	Vss	59	VcclO	99	Vss	139	SysAD0
20	SysAD9	60	Vss	100	SysAD20	140	VcclO
21	VcclO	61	SysCmd6 / (GND)	101	SysAD21	141	Vss
22	Vss	62	SysCmd7 / (GND)	102	VcclO	142	SysAD1
23	SysAD10	63	SysCmd8 / (GND)	103	Vss	143	SysAD2
24	SysAD11	64	SysCmdP / (GND)	104	SysAD22	144	Vcclnt
25	Vcclnt	65	Vcclnt	105	Vcclnt	145	Vss
26	Vss	66	Vss	106	Vss	146	SysAD3
27	SysAD12	67	VcclO	107	SysAD23	147	PCST8
28	VcclO	68	HALT/DOZE	108	SysAD24	148	PCST7
29	Vss	69	Int0*	109	VcclO	149	PCST6
30	SysAD13	70	Int1*	110	Vss	150	PCST5
31	SysAD14	71	Int2*	111	SysAD25	151	PCST4
32	Vcclnt	72	Int3*	112	Vcclnt	152	VcclO
33	Vss	73	Int4*	113	Vss	153	Vss
34	SysAD15	74	Int5*	114	SysAD26	154	VcclO
35	BufSel0	75	VcclO	115	SysAD27	155	VssPLL
36	PCST3	76	Vss	116	VcclO	156	PLLAP
37	PCST2	77	TPC3	117	MODE43*	157	VccPLL
38	PCST1	78	TPC2	118	DivMode1	158	Vss
39	PCST0	79	TPC1	119	DivMode0	159	MasterClock
40	VcclO	80	DCLK	120	Vss	160	VcclO

Note1: “ \* ” means the signal is the low-active.

Note2: MODE43\* SysAD Bus protocol select.

0 : TX4300 protocol 1 : R5000 protocol

Note3: At TX4300 protocol mode PReq\* signal is not support.

## 4.2 PIN FUNCTION

The following is a list of interface, interrupt, and miscellaneous pins available on the TMPR4955AF.

### SYSTEM INTERFACE (When MODE43\* = 1)

PIN NAME	I / O	FUNCTION
SysAD(31:0)	I / O	<b>System address / data bus</b> A 32-bit address and data bus for communication between the processor and an external agent.
SysCmd(8:0)	I / O	<b>System command / data identifier bus</b> A 9-bit bus for command and data identifier transmission between the processor and an external agent.
SysADC(3:0)	I / O	<b>System command/data check bus</b> A 4-bit bus containing parity check bits for the SysAD bus during data cycles.
SysCmdP	I / O	<b>Reserved for system command/data identifier bus parity</b> For the TMPR4955AF this signal is unused on input and zero on output.
ValidIn*	I	<b>Valid input</b> The external agent asserts ValidIn* when it is driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
ValidOut*	O	<b>Valid output</b> The processor asserts ValidOut* when it is driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
ExtRqst*	I	<b>External request</b> An external agent asserts ExtRqst* to request use of the System interface.
Release*	O	<b>Release interface</b> Signals that the system interface needs to submit an external request.
WrRdy*	I	<b>Write Ready</b> Signals that an external agent can now accept a processor write request.
RdRdy*	I	<b>Read Ready</b> Signals that an external agent can now accept a processor read request.

## SYSTEM INTERFACE (When MODE43\* = 0)

PIN NAME	I / O	FUNCTION
SysAD(31:0)	I / O	<b>System address / data bus</b> A 32-bit address and data bus for communication between the processor and an external agent.
SysCmd(4:0)	I / O	<b>System command / data identifier bus</b> A 9-bit bus for command and data identifier transmission between the processor and an external agent.
SysCmd(8:5) / GND	O	<b>Reserved</b> <b>Always output Low level signal.</b>
SysADC(3:0) / GND	O	<b>Reserved</b> Always output Low level signal.
SysCmdP / GND	O	<b>Reserved</b> Always output Low level signal.
ValidIn* / EValid*	I	<b>Valid input</b> The external agent asserts EValid* when it is driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
ValidOut* / PValid*	O	<b>Valid output</b> The processor asserts PValid* when it is driving a valid address or data on the SysAD bus and a valid command or data identifier on the SysCmd bus.
ExtRqst* / EReq*	I	<b>External request</b> An external agent asserts EReq* to request use of the System interface.
Release* / PMaster*	O	<b>Processor master</b> Show that the TMPR4955AF is the System bus master.
WrRdy* / EOK*	I	<b>External OK</b> Signals that an external agent can now accept a processor write request.
RdRdy* / GND	I	<b>Reserved</b> Always input Low level signal. This signal has the internal pull-down resistor.

## CLOCK / CONTROL INTERFACE

PIN NAME	I / O	FUNCTION															
MasterClock	I	<b>Master clock</b> Master clock input that establishes the processor operating frequency.															
DivMode(1:0)	I	<b>Set the operational frequency of the System interface</b> <table border="1"> <thead> <tr> <th>DivMode(1:0)</th> <th>MasterClock</th> <th>Pclock</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>50.0MHz</td> <td>200MHz (1:4)</td> </tr> <tr> <td>01</td> <td>80.0MHz</td> <td>200MHz (1:2.5)</td> </tr> <tr> <td>10</td> <td>100.0MHz</td> <td>200MHz (1:2)</td> </tr> <tr> <td>11</td> <td>66.7MHz</td> <td>200MHz (1:3)</td> </tr> </tbody> </table>	DivMode(1:0)	MasterClock	Pclock	00	50.0MHz	200MHz (1:4)	01	80.0MHz	200MHz (1:2.5)	10	100.0MHz	200MHz (1:2)	11	66.7MHz	200MHz (1:3)
DivMode(1:0)	MasterClock	Pclock															
00	50.0MHz	200MHz (1:4)															
01	80.0MHz	200MHz (1:2.5)															
10	100.0MHz	200MHz (1:2)															
11	66.7MHz	200MHz (1:3)															
TintDis	I	<b>Timer-Interrupt disable input</b> 0 enable Timer-Interrupt (can not use int5*) 1 disable Timer-Interrupt															
HALT/DOZE	O	<b>HALT/DOZE mode output</b> This signal indicates that the TMPR4955AF is in the HALT or DOZE mode when this signal is "H".															
PLLReset*	I	<b>PLL reset input</b> A signal to halt the PLL oscillation of the TMPR4955AF built-in clock generator. 0 PLL is halt (no oscillation ) 1 PLL is enabled.															
Endian	I	<b>Endianess input</b> Indicates the initial setting of the endian during a reset. 0 Little Endian 1 Big Endian															

## INTERRUPT INTERFACE

PIN NAME	I / O	FUNCTION
Int(5:0)*	I	<b>Interrupt</b> Five general processor interrupts, bit-wise ORed with bits 5:0 of the interrupt register and visible as bits 15:10 of the Cause register.
NMI*	I	<b>Non-maskable interrupt</b> Non-maskable interrupt, ORed with bit 6 of the interrupt register.

## JTAG INTERFACE

PIN NAME	I / O	FUNCTION
JTDI	I	<b>JTAG data input / Debug interrupt input</b> Run-time mode : input serial data to data/instruction register of JTAG. Real-time mode : interrupt line to change the debug unit state from real time mode to Run-time mode.
JTCK	I	<b>JTAG clock input</b> The processor receives a serial clock on JTCK. On the rising edge of JTCK, both JTDI and JTMS are sampled.
JTDO/TPC(0)	O	<b>JTAG data output / PC Trace output</b> Run-time mode : output serial data from data/instruction register of JTAG. Real-time mode : output non-sequential program.
JTMS	I	<b>JTAG command</b> JTAG command signal, indicating the incoming serial data is command data.
DCLK	O	<b>Debug Clock</b> A clock output for a real-time debug system. The timing of a serial monitor bus and PC trace interface signal are all defined by this debug clock DCLK. The operation clock of the TMPR4955AF is divided by 3 at the time of a serial monitor bus operation.
PCST(8:0)	O	<b>PC trace status</b> Output PC trace status information and the mode of the serial monitor bus.
TPC(3:1)	O	<b>PC trace output</b> Output a non-sequential program counter at DCLK.
TRST*	I	<b>Test Reset input</b> A reset input for a real-time debug system. When TRST* is asserted, the debug support unit (DSU) is initialized.



## INITIALIZATION INTERFACE

PIN NAME	I / O	FUNCTION										
Reset*	I	<b>Soft (Warm) Reset</b> This signal must be asserted synchronously with MasterClock for a soft reset.										
ColdReset*	I	<b>Cold reset</b> This signal indicates to the processor that the +3.3V(I/O) and +1.5V(Internal) power supply is stable and the processor should initiate a cold reset sequence, resetting the PLL.										
MODE43*	I	MODE43* SysAD Bus protocol select. 0 TX4300 protocol 1 R5000 protocol										
BufSel(1:0)	I	Output buffer level Select <table border="1"> <thead> <tr> <th>BufSel(1:0)</th> <th>Level</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>50% (4mA buffer)</td> </tr> <tr> <td>01</td> <td>Reserved</td> </tr> <tr> <td>10</td> <td>150% (12mA buffer)</td> </tr> <tr> <td>11</td> <td>100% (8mA buffer)</td> </tr> </tbody> </table>	BufSel(1:0)	Level	00	50% (4mA buffer)	01	Reserved	10	150% (12mA buffer)	11	100% (8mA buffer)
BufSel(1:0)	Level											
00	50% (4mA buffer)											
01	Reserved											
10	150% (12mA buffer)											
11	100% (8mA buffer)											
PLLCAP	I	<b>PLL connect to capacitor</b> Non connection.										

## OTHERS

PIN NAME	I / O	FUNCTION
VccPLL	I	<b>Quiet V<sub>CC</sub> for PLL</b> Quiet V <sub>CC</sub> for the internal phase locked loop. (1.5v)
VssPLL	I	<b>Quiet V<sub>SS</sub> for PLL</b> Quiet V <sub>SS</sub> for the internal phase locked loop.
VccIO	I	<b>Vcc</b> Power supply pin for IO.( 3.3v )
VccInt	I	<b>Vcc</b> Power supply pin for internal.(1.5v)
VSS	I	<b>Vss</b> Ground pin

## 5. ELECTRICAL CHARACTERISTICS

**Note:** “Be careful of static” , please see “From Incoming to Shipping” of **General Safety Precautions and Usage Considerations.**

### 5.1 ABSOLUTE MAXIMUM RATINGS

TMPR4955AF-200

$V_{SS} = 0 \text{ V (GND)}$			
PARAMETER	SYMBOL	RATINGS	UNIT
Supply voltage ( for I/O)	$V_{CCIO\text{Max}}$	-0.5 to 3.9	V
Supply voltage ( for internal )	$V_{CCInt\text{Max}}$	-0.5 to 3.0	V
Input voltage <sup>(*1) (*2)</sup>	$V_{IN}$	-0.5 to $V_{CC} + 0.3$	V
Storage Temperature	$T_{STG}$	-65 to +150	°C

Note ) If LSI is used above the maximum ratings, permanent destruction of LSI can result. In addition, it is desirable to use LSI for normal operation under the recommended condition. If these conditions are exceeded, reliability of LSI may be adversely affected.

(\*1)  $V_{IN}$  Min. = -1.5V for pulse width less than 10 ns.

(\*2) keep ( $V_{CCIO} + 0.3\text{V}$ ) less than  $V_{CCIO\text{Max}}$

### 5.2 RECOMMENDED OPERATING CONDITIONS

TMPR4955AF- 200

$V_{SS} = 0 \text{ V (GND)}$					
PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	Unit
Supply Voltage ( for I/O )	$V_{CCIO}$		3.1	3.5	V
Supply Voltage ( for internal )	$V_{CCInt}$		1.4	1.6	V
Operating Case Temperature	$T_C$		0	+70	°C

Note : The recommended operating conditions for a device are operating conditions under which it can be guaranteed that the device will operate as specified. If the device is used under operating conditions other than the recommended operating conditions (supply voltage, operating temperature range, specified AC and DC values etc.), malfunction may occur. Thus, when designing products which include this device, ensure that the recommended operating conditions for the device are always adhered to.

## 5.3 DC CHARACTERISTICS

TMPR4955AF-200

 $T_C = 0^\circ\text{C to } 70^\circ\text{C}, V_{CCInt} = 1.5\text{V} \pm 0.1\text{V}, V_{CCIO} = 3.3\text{V} \pm 0.2\text{V}$ 

PARAMETER	SYM BOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output High Voltage	$V_{OH}$	$V_{CCIO} = 3.3\text{V}, V_{SS} = 0\text{V}$ $I_{OH} = -4\text{ mA}$	2.4			V
Output Low Voltage	$V_{OL}$	$V_{CCIO} = 3.3\text{V}, V_{SS} = 0\text{V}$ $I_{OL} = 4\text{ mA}$			0.4	V
Input High Voltage <sup>(*2)</sup>	$V_{IH}$		2.0		$V_{CCIO} + 0.3$	V
Input Low Voltage <sup>(*1,2)</sup>	$V_{IL}$		-0.5 <sup>(*1)</sup>		0.8	V
Operating Current 1 (Normal operation)	$I_{CCInt}$	$V_{CCIO} = 3.3\text{V},$ $V_{CCInt} = 1.5\text{V},$ MasterClock=100MHz, PClock = 200MHz		350	550	mA
Operating Current 2 (HALT mode)	$I_{CCInt}$	$V_{CCIO} = 3.3\text{V},$ $V_{CCInt} = 1.5\text{V},$ MasterClock=100MHz, PClock = 0MHz			150	mA
Operating Current 3 (MasterClock stopped)	$I_{CCInt}$	$V_{CCIO} = 3.3\text{V},$ $V_{CCInt} = 1.5\text{V},$ MasterClock=0MHz, PClock = 0MHz			50	mA
Operating Current	$I_{CCIO}$	$V_{CCIO} = 3.3\text{V},$ $V_{CCInt} = 1.5\text{V},$ MasterClock=100MHz, PClock = 200MHz Load = 25pF		50	60	mA
Input Leakage	$I_{LI}$	Except (*3)port			$\pm 10$	$\mu\text{A}$
Pull-up <sup>(*3)</sup>	R <sub>inU</sub>		30	50	100	Kohm
Pull-down <sup>(*4)</sup>	R <sub>inD</sub>		30	50	100	Kohm
Output Leakage	$I_{LO}$				$\pm 20$	$\mu\text{A}$
Input Capacitance	$C_{IN}$				10	pF
Output Capacitance	$C_{OUT}$				10	pF

(\*1)  $V_{IL}$  Min. = -1.5V for pulse width less than 10 ns.

(\*2) Except for MasterClock input

(\*3) Applies to Int(5:0)\*, NMI\*, RESET\*, JTMS, JTCK, JTDI, TPC1 inputs with pull-up resistor

(\*4) Applies to TRST\*, RdRdy\*, TPC3, TPC2 inputs with pull-down resistor

## 5.4 AC CHARACTERISTICS

### 5.4.1 CLOCK TIMING

TMPR4955AF-200

$T_c = 0^\circ\text{C to } 70^\circ\text{C}$ ,  $V_{ccInt} = 1.5\text{V} \pm 0.1\text{V}$ ,  $V_{ccIO} = 3.3\text{V} \pm 0.2\text{V}$

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNITS
MasterClock High	$t_{MCH}$	Transition 5 ns	3.0		ns
MasterClock Low	$t_{MCL}$	Transition 5 ns	3.0		ns
MasterClock Frequency <sup>(*)1</sup>	$f_{MCK}$		20	100.0	MHz
Internal Operation Frequency	$f_{PCK}$		50	200	MHz
MasterClock Period	$t_{MCP}$		10	50	ns
MasterClock Rise Time	$t_{MCR}$			2.0	ns
MasterClock Fall Time	$t_{MCF}$			2.0	ns

(\*1) Operation of TMPR495AF is only guaranteed with the Phase Lock Loop enabled.

(\*2) All output timings assume a 25 pF capacitive load. Output timings should be derated where appropriate.

### 5.4.2 SYSTEM INTERFACE

TMPR4955AF-200

$T_c = 0^\circ\text{C to } 70^\circ\text{C}$ ,  $V_{ccInt} = 1.5\text{V} \pm 0.1\text{V}$ ,  $V_{ccIO} = 3.3\text{V} \pm 0.2\text{V}$ , BufSel=100%

PARAMETER	SYMBOL	MIN.	MAX.	UNITS
Data Output <sup>(*)1,2,3</sup>	$t_{DO}$	1.0	6.5	ns
Data Setup <sup>(*)3</sup>	$t_{DS}$	3.5		ns
Data Hold <sup>(*)3</sup>	$t_{DH}$	1.0		ns

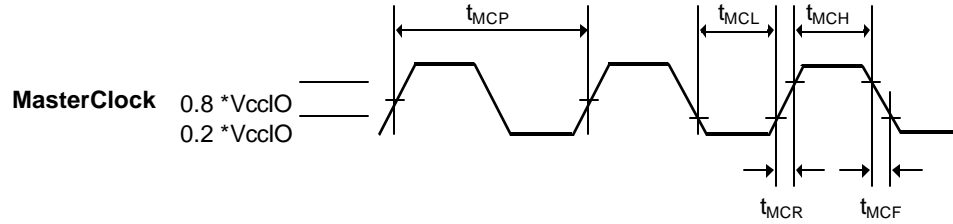
(\*1) Timings are measured from 1.5V of the SClOCK to 1.5V of signal.

(\*2) Capacitive load for all output timings is 25 pF.

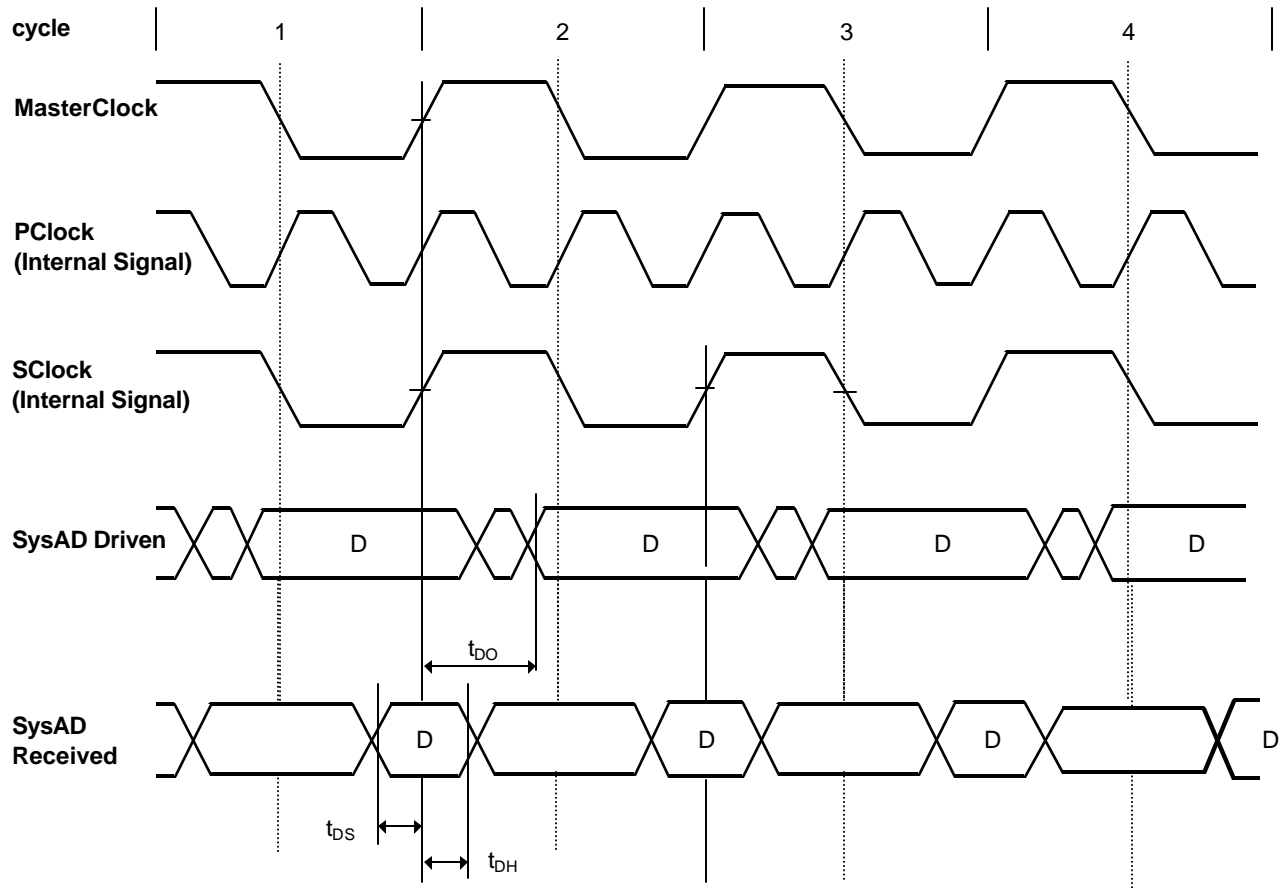
(\*3) Data Output, Data Setup and Data Hold apply to all logic signals driven out of or driven into the TMPR4955AF on the system interface. Clocks are specified separately.

**5.5 TIMING DIAGRAMS**

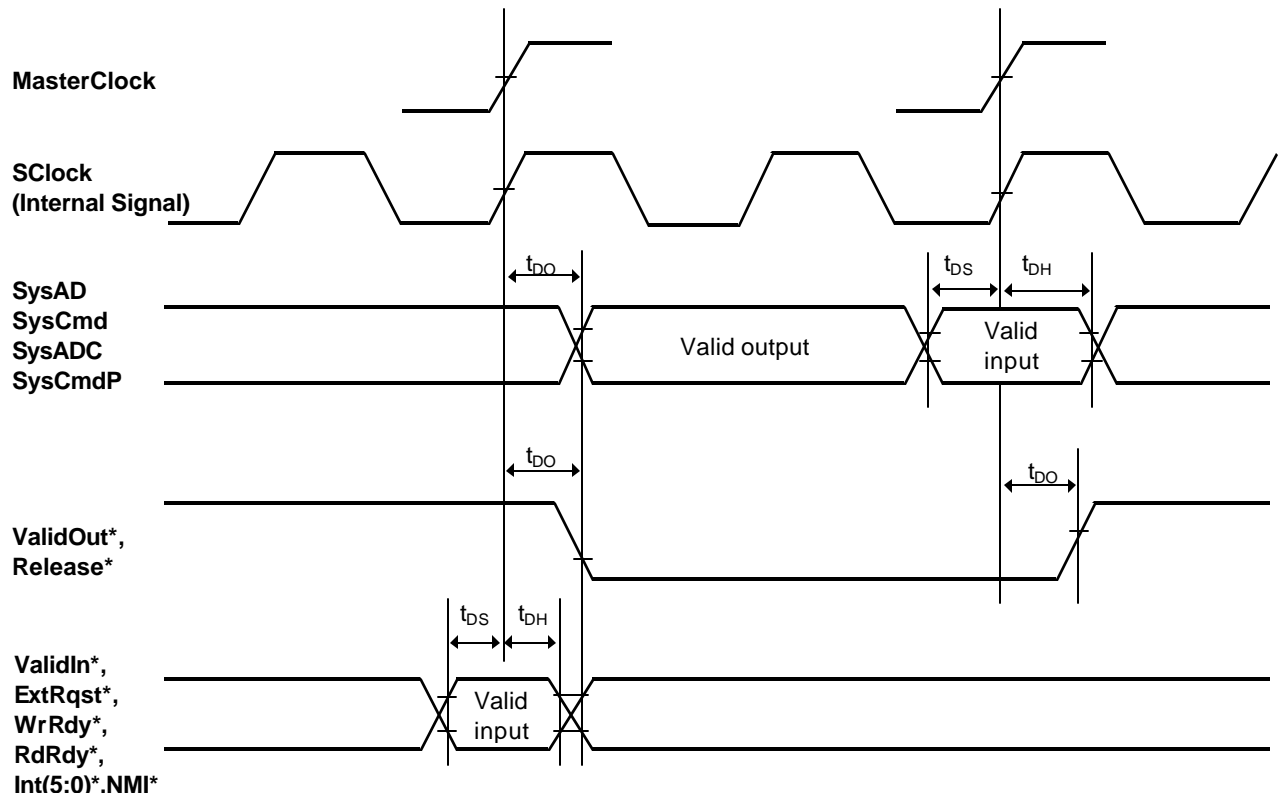
**5.5.1 CLOCK TIMING**



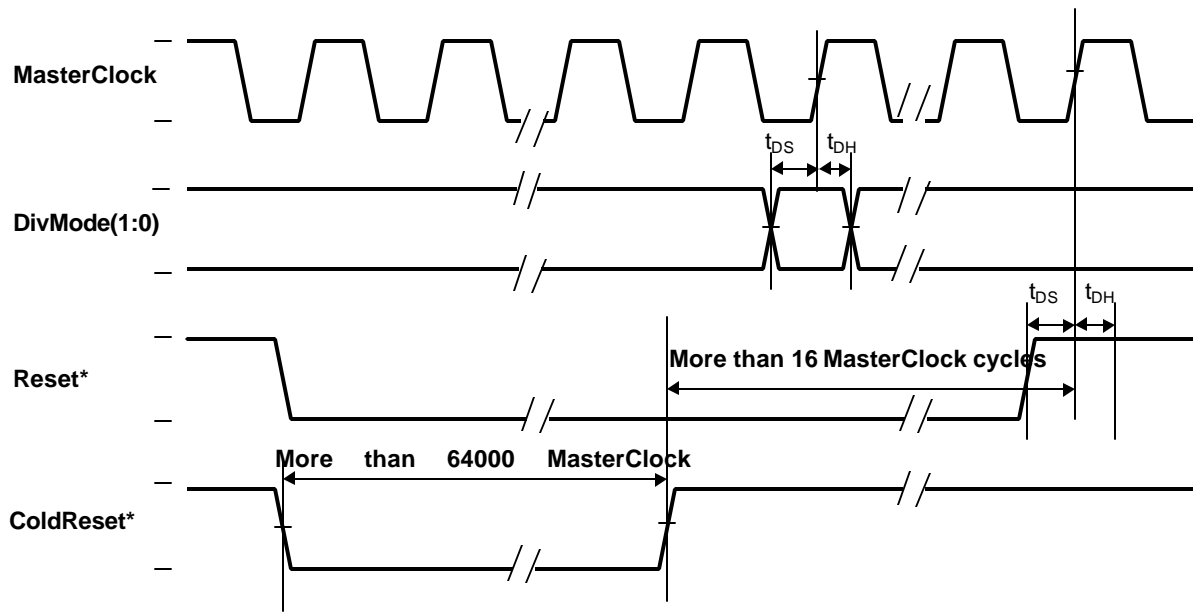
5.5.2 PClock to SClock DIVISOR of 2



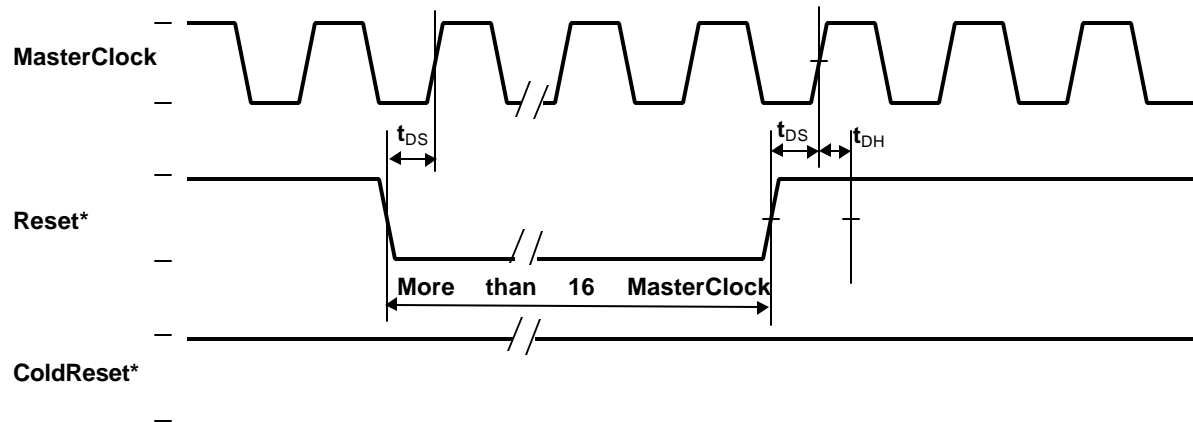
5.5.3 SYSTEM INTERFACE TIMING



5.5.4 COLD RESET TIMING



5.5.5 WARM RESET TIMING







## 7. PLL Passive Components

The Phase Locked Loop circuit requires several passive components for proper operation, which are connected to VccPLL, and VssPLL, as illustrated in Figure 1.

In addition, the capacitors for PLLCAP (CP) can be connected to either VccPLL. Note that C2 and the Cp capacitors are only incorporated into the QFP package as surface-mounted chip capacitors.

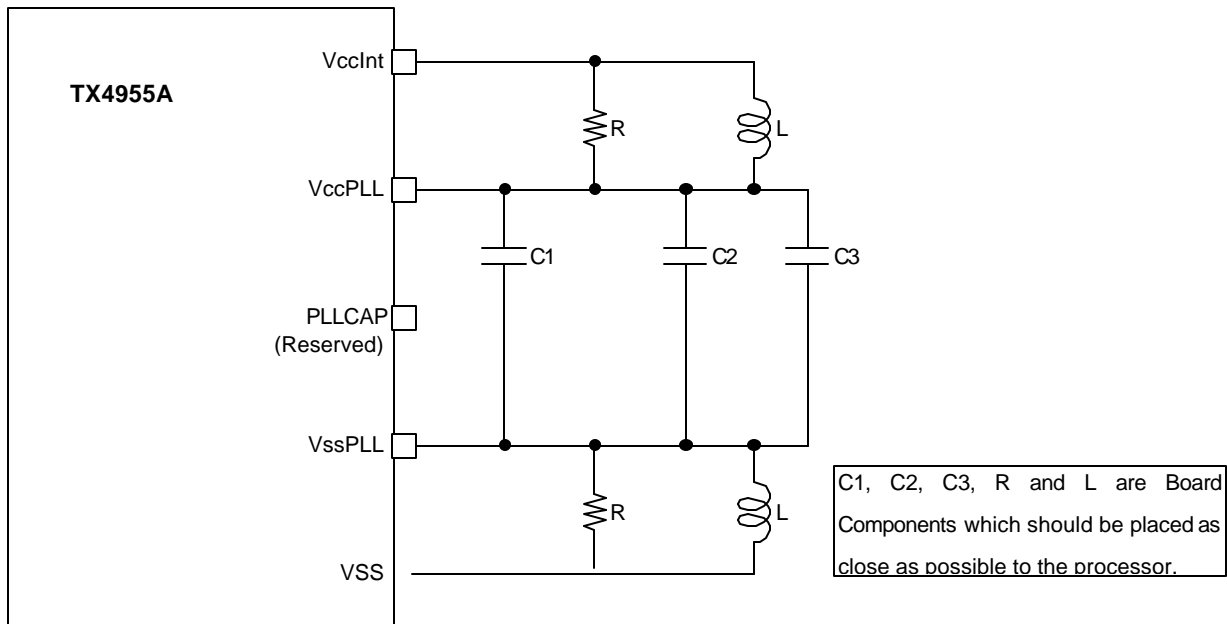


Figure 1 PLL Recommended Circuit

### Reference Values:

$$R = 5 \Omega^{(*)}$$

$$C1 = 1 \text{ nF}^{(*)}$$

$$C2 = 82 \text{ nF}^{(*)}$$

$$C3 = 10 \mu\text{F}^{(*)}$$

$$V_{ccInt} = 1.5 \text{ V} \pm 0.1 \text{ V}$$

Note \*1 : Change to the suitable value on each board

The inductors (L) can be used as alternatives to the resistors (R) to filter the power supply.

It is essential to isolate the analog power and ground for the PLL circuit (VccPLL/VssPLL) from the regular power and ground (VccInt/Vss).

## 8. Differences Between the TMPR4955F and the TMPR4955AF

Product Name	TMPR4955F	TMPR4955AF
Power Supply: Core (incl. PLL) I/O	2.5V 3.3 V	1.5V 3.3 V
Pin Assignment (No.2) and (No.35)	VccIO VccIO	BufSel1 BufSel0
I/O Buffer Drive (Ratio)	1.0	Selectable from 0.5, 1.0 and 1.5

Note:            BufSel (1:0) =    11      10      01      00  
                   Output Drive Ratio =    100%    150% Reserved    50%

<u>Influenced Signals</u>	<u>I/O</u>
SysAD(31:0)	I/O
SysCmd(8:0)	I/O
SysADC(3:0)	I/O
SysCmdP	I/O
ValidOut*	O
Release*	O
HALTDOZE	O

## 9. History

2000-9-29

2000-10-12 page-9 OTHERS of PIN FUNCTION VccPLL 2.5V -> 1.5V

2000-11-17 AC and DC specification

PLL passive components

2002-1-17 Deleted 167MHz spec.