E4/STM-1/OC-3 ATM TRANSCEIVER S3031B

FEATURES

- Complies with Bellcore and ITU-T specifications
- On-chip high-frequency PLLs for clock generation and clock recovery
- On-chip analog circuitry for transformer driver and equalization
- Supports 139.264 Mbps (E4) and 155.52 Mbps (OC-3) transmission rates
- Supports 139.264 Mbps and 155.52 Mbps Coded Mark Inversion (CMI) interfaces
- TTL Reference frequencies of 19.44 and 38.88 MHz (OC-3) or 17.408 and 34.816 MHz (E4)
- Interface to both PECL and TTL logic
- Lock detect on clock recovery function — monitors run length and frequency
- Serial and 4 bit (nibble) system interfaces
- Low jitter PECL interface
- +5V operation
- 100 PQFP/TEP package
- Supports both electrical and optical interfaces

APPLICATIONS

- ATM over SONET/SDH
- OC-3/STM-1 or E4-based transmission systems
- OC-3/STM-1 or E4 modules
- OC-3/STM-1 or E4 test equipment
- Section repeaters
- Add Drop Multiplexers (ADM)
- Broadband cross-connects
- Fiber optic terminators
- Fiber optic test equipment

GENERAL DESCRIPTION

The S3031B transceiver chip is a fully integrated CMI encoding transmitter and CMI decoding receiver. The chip derives high speed timing and data signals for SONET/SDH or PDH-based equipment. The circuit is implemented using AMCC's proven Phase Locked Loop (PLL) technology. Figures 1a and 1b show typical network applications.

The S3031B has two independent VCOs which are synchronized to the local NRZ transmitted data and the received CMI data respectively. The chip can be used with either a 19.44 MHz or a 38.88 MHz reference clock when operated in the SONET/SDH OC-3 mode. In E4 mode the chip can be operated with a 17.408 MHz or a 34.816 MHz reference in support of existing system clocking schemes. On-chip coded-mark-inversion (CMI) encoding and decoding is provided for 139.264 Mbps and 155.52 Mbps interfaces.

The low jitter PECL interface for the serial data inputs and the PECL nibble clock interface guarantee compliance with the bit-error rate requirements of the Bellcore and ITU-T standards. The S3031B is packaged in a 0.65 mm pitch 100-pin PQFP/TEP.

The S3031B provides the major active components on-chip for a coaxial cable interface, including analog transformer driver circuitry and equalization interface circuitry. Discrete controls permit separate selection of CMI or NRZ operation and analog (coaxial copper) or PECL (optical module) media interfaces. Both line loopback and diagnostic local loopback operation are supported.

Figure 1a. Electrical Interface

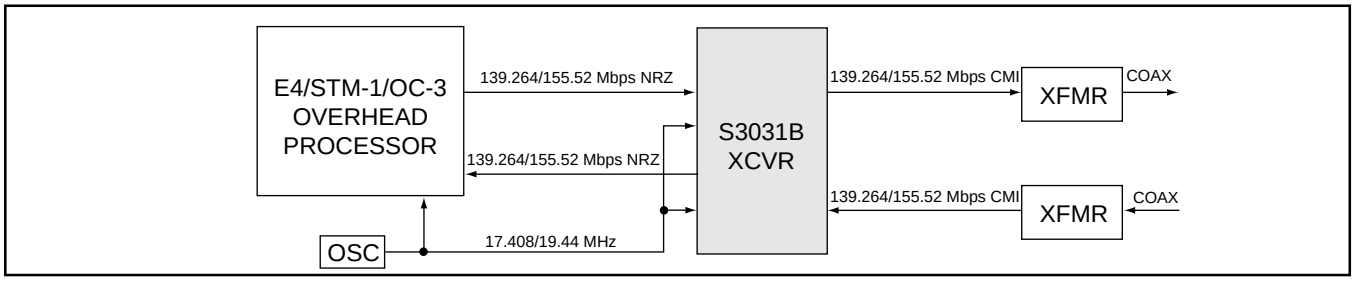
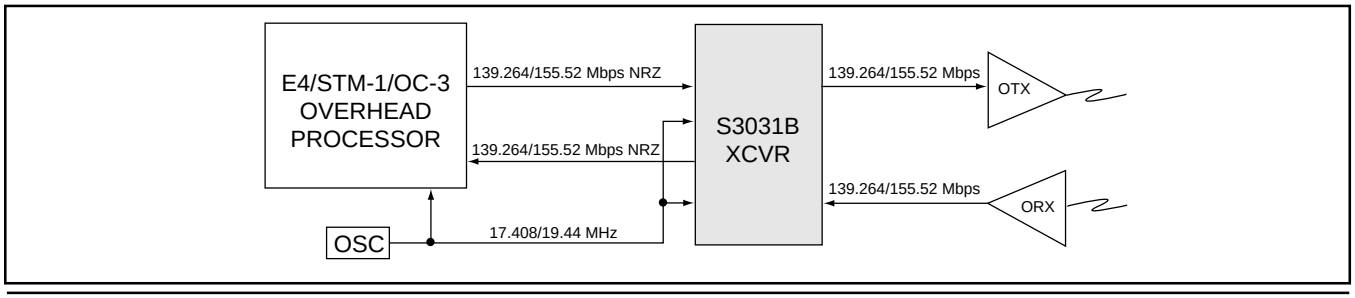


Figure 1b. Optical Interface



SONET/SDH OVERVIEW

Synchronous Optical Network (SONET) is a standard for connecting one fiber system to another at the optical level. SONET, together with the Synchronous Digital Hierarchy (SDH) administered by the ITU-T, form a single international standard for fiber interconnect between telephone networks of different countries. SONET is capable of accommodating a variety of transmission rates and applications.

The SONET standard is a layered protocol with four separate layers defined. These are:

- Photonic
- Section
- Line
- Path

Figure 2 shows the layers and their functions. Each of the layers has overhead bandwidth dedicated to administration and maintenance. The photonic layer simply handles the conversion from electrical to optical and back with no overhead. It is responsible for transmitting the electrical signals in optical form over the physical media. The section layer handles the transport of the framed electrical signals across the optical cable from one end to the next. Key functions of this layer are framing, scrambling, and error monitoring. The line layer is responsible for the reliable transmission of the path layer information stream carrying voice, data, and video signals. Its main functions are synchronization, multiplexing, and reliable transport. The path layer is responsible for the actual transport of services at the appropriate signaling rates.

Data Rates and Signal Hierarchy

Table 1 contains the data rates and signal designations of the SONET hierarchy. The lowest level is the basic SONET signal referred to as the synchronous transport signal level-1 (STS-1). An STS-*N* signal is made up of *N* byte-interleaved STS-1 signals. The optical counterpart of each STS-*N* signal is an optical carrier level-*N* signal (OC-*N*). The S3031B supports OC-3 rates (155.52 Mbps).

Frame and Byte Boundary Detection

The SONET/SDH fundamental frame format for STS-3 consists of nine transport overhead bytes followed by Synchronous Payload Envelope (SPE) bytes. This pattern of 9 overhead and 261 SPE bytes is repeated nine times in each frame. Frame and byte boundaries are detected using the A1 and A2 bytes found in the transport overhead. (See Figure 3.)

For more details on SONET operations, refer to the Bellcore SONET standard document.

Table 1. SONET Signal Hierarchy

Elec.	ITU-T	Optical	Data Rate (Mbps)
STS-1		OC-1	51.84
STS-3	STM-1	OC-3	155.52
STS-12	STM-4	OC-12	622.08
STS-24		OC-24	1244.16
STS-48	STM-16	OC-48	2488.32

Figure 2. SONET Structure

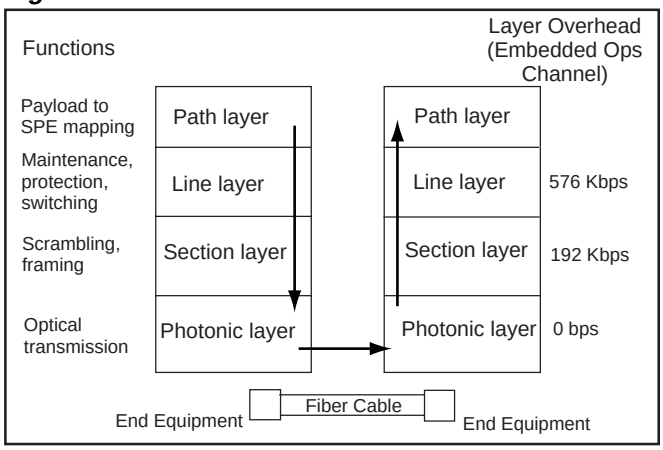
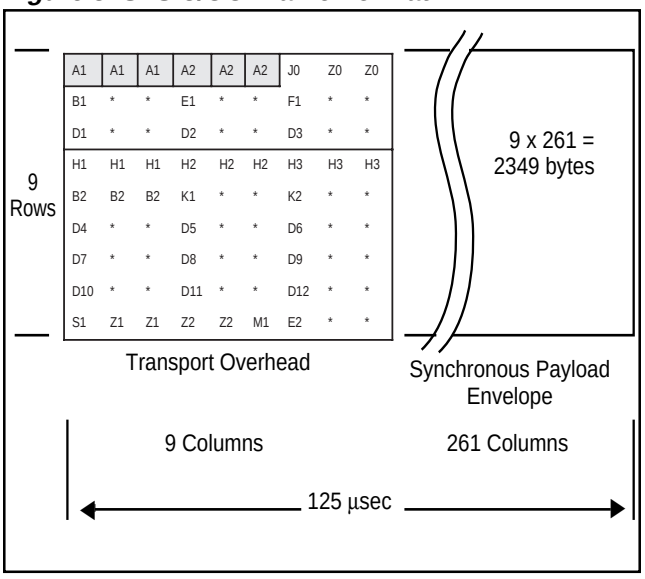


Figure 3. STS-3/OC Frame Format



S3031B OVERVIEW

The S3031B transceiver can be used to implement the front end of STS-3, OC-3 or E4 equipment. The block diagram in Figure 9 shows the basic operation of the chip.

When the S3031B is operating in the nibble parallel mode, the transmitter VCO is synchronized to the 38.88 MHz nibble clock as both the reference clock and the data transfer clock. If the serial input is selected as the transmitter data source the VCO will be synchronized directly to the incoming data. Serial operation of the S3031B transmitter section is possible with either the 38.88 MHz or 19.44 MHz reference oscillator. In the absence of incoming serial data the transmitter section will operate as a clock synthesizer. The receiver section performs clock recovery by synchronizing its on-chip VCO directly to the incoming data stream.

In E4 operation, the 34.816 MHz REFCLK is used as the nibble clock. Thus in Nibble parallel mode, the S3031B transmitter section supports unscrambled E4 operation. If serial mode is selected, the NRZ E4 data must be scrambled to allow the PLL to lock onto the data transitions.

The S3031B provides a PECL output for an optical interface and two transformer driver outputs for an electrical interface. One of these drivers is a monitor output. The S3031B provides a PECL input for an optical interface and an analog input for an electrical interface.

The transformer driver outputs are separately enabled. Status outputs detect the disabled, stuck at 1, stuck at 0, and non-CMI states to qualify the transformer driver outputs.

The CMI outputs, analog equalizer input section, and PLL sections are independently powered for isolation and for power savings when the device is used in single function applications.

S3031B TRANSMITTER ARCHITECTURE/FUNCTIONAL DESIGN

Transmitter Operation

The S3031B chip's transmitter section performs the last stages of digital processing of a transmit SONET STS-3 or ITU-T E4 serial or 4-bit nibble parallel data stream.

Clock Recovery

If the serial input data has been selected, and serial data is present at the TSDATIP/N inputs, the clock is recovered from the serial data stream at 139.264 MHz or 155.52 MHz and synthesized to 278.528 MHz or 311.04 MHz to CMI encode the incoming data.

In clock recovery mode, the transmitter PLL continues to monitor the reference clock with respect to the VCO and the activity of the serial data input. The transmitter PLL will re-lock to the reference clock under the following conditions:

1. If the serial data inputs contains insufficient transition density (run length greater than 100 to 200 bit times).
2. If the VCO drifts away from the local reference clock by more than 1000 ppm.

If either XFRMENA or XFRMENB are enabled (logic Low) the density or frequency error defined above will set the appropriate status (XFRMSTATA and/or XFRMSTATB) to the low or fault state.

The selected drive status bits will return to the High or clear state and the PLL will again lock to the data if the serial data contains sufficient transition density (less than 100 to 200 bit times between rising edges), and the serial clock is within 250 ppm of the reference clock determined frequency.

Optical and Electrical Interfaces

The digital data outputs (TSDATOP/N) are the PECL outputs for an optical interface and are to be connected to an electrical to optical converter, as shown in Figure 17. This data is also routed to two on-chip transformer drivers and sent out on XFRMDRVA and XFRMDRVB to drive the transformers of the electrical interface, as shown in Figure 19. These outputs are shut off when the reset is active, XFRMEN is active, or when the chip is in NRZ mode and the data inputs are in the logic zero state. The electrical characteristics for the transformer drivers are shown in Table 9.

Parallel-to-Serial Converter

The parallel-to-serial converter shown in Figure 9 is comprised of two 4-bit registers. The first register latches the data from the PIN[3:0] bus on the rising edge of REFCLK. The second register is a parallel loadable shift register which takes its parallel input from the first register.

The parallel data transfer between registers is accomplished on the falling edge of REFCLK. The serial data is shifted out at the serial bit rate to the CMI encoder.

CMI Encoding

Coded Mark Inversion format (CMI) ensures at least one data transition per 1.5 bit periods, thus aiding the clock recovery process. Zeros are represented by a Low state for one half a bit period, followed by a High state for the rest of that bit period. Ones are represented by a steady Low or High state for a full bit period. The state of the ones bit period alternates at each occurrence of a one. Figure 4 shows an example of CMI-encoded data. The STS-3 electrical interface and the E4 interface are specified to have CMI-encoded data.

The CMI encoder on the S3031B accepts serial data from TSDATIP/N at 139.264 or 155.52 Mb/s. The data is then encoded into CMI format, and the result is shifted out with transitions at twice the basic data rate. The CMISEL input controls whether the CMI encoder is in the data path. A CMI code violation can be inserted for diagnostic purposes by activating the DLCV input. The DLCV input is sampled on every cycle of the serial clock to allow the single or multiple line code violations to be inserted. This violation is either an inverted zero code or an inversion of the alternating ones logic level, depending on the state of the data. Subsequent one codes take into account the induced violation to avoid error multiplication.

Jitter Generation

Jitter Generation is defined as the amount of jitter at the OC-3 or E-4 output of equipment. Jitter generation for OC-3 shall not exceed 0.01 UI rms when measured using a highpass filter with a 12 kHz cutoff frequency.

For STM-1 and E4, the jitter generated shall not exceed the specifications shown in Figure 5.

In order to meet the SONET, STM-1 E4 jitter specifications as shown in Figure 5, the TSDATIP/N serial data input must meet the jitter characteristics as shown in Figure 6.

Figure 4. CMI Encoded Data

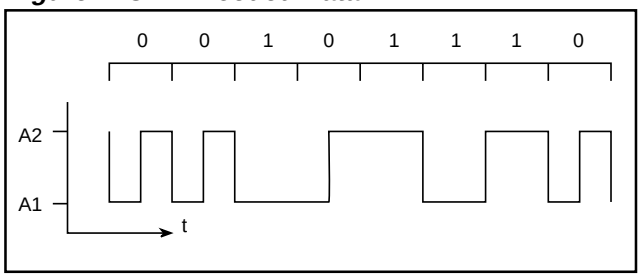
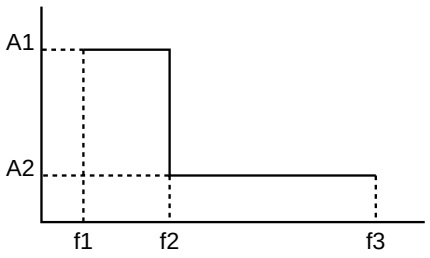


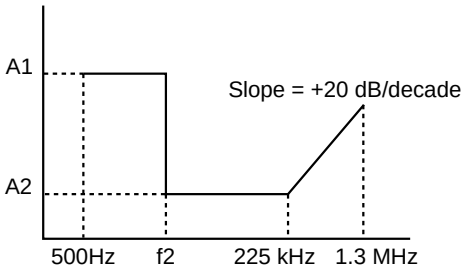
Figure 5. Jitter Generation Specifications Compliant to G.823 and G.825



	f1(Hz)	f2(kHz)	f3(MHz)	A1	A2
OC-3	—	—	—	0.01(1)	0.01(1)
STM-1	500	65	1.3	1.5(2)	0.15(2)
E4	200	10	3.5	1.5(2)	0.075(2)

1. UI rms
2. UI p–p

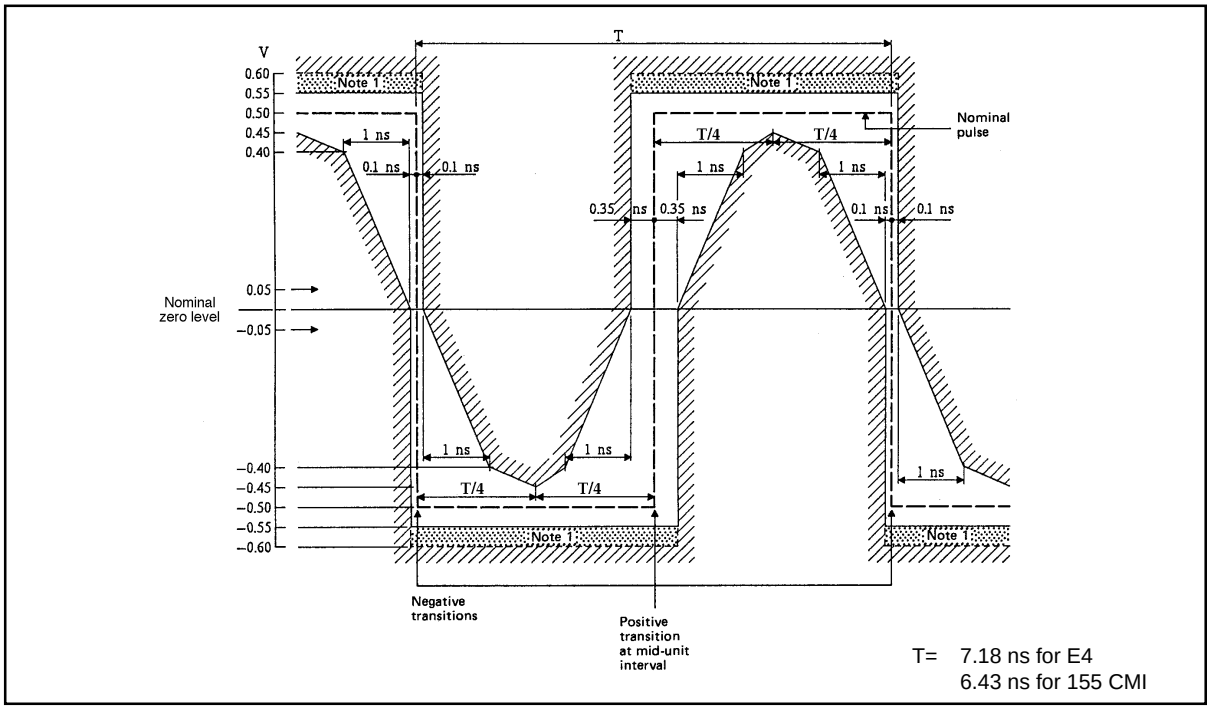
Figure 6. S3031B Maximum Allowable Input Jitter



	f2(kHz)	A1	A2
OC-3	—	0.005(1)	0.005(1)
STM-1	65	1.45(2)	0.10(2)
E4	10	1.45(2)	0.025(2)

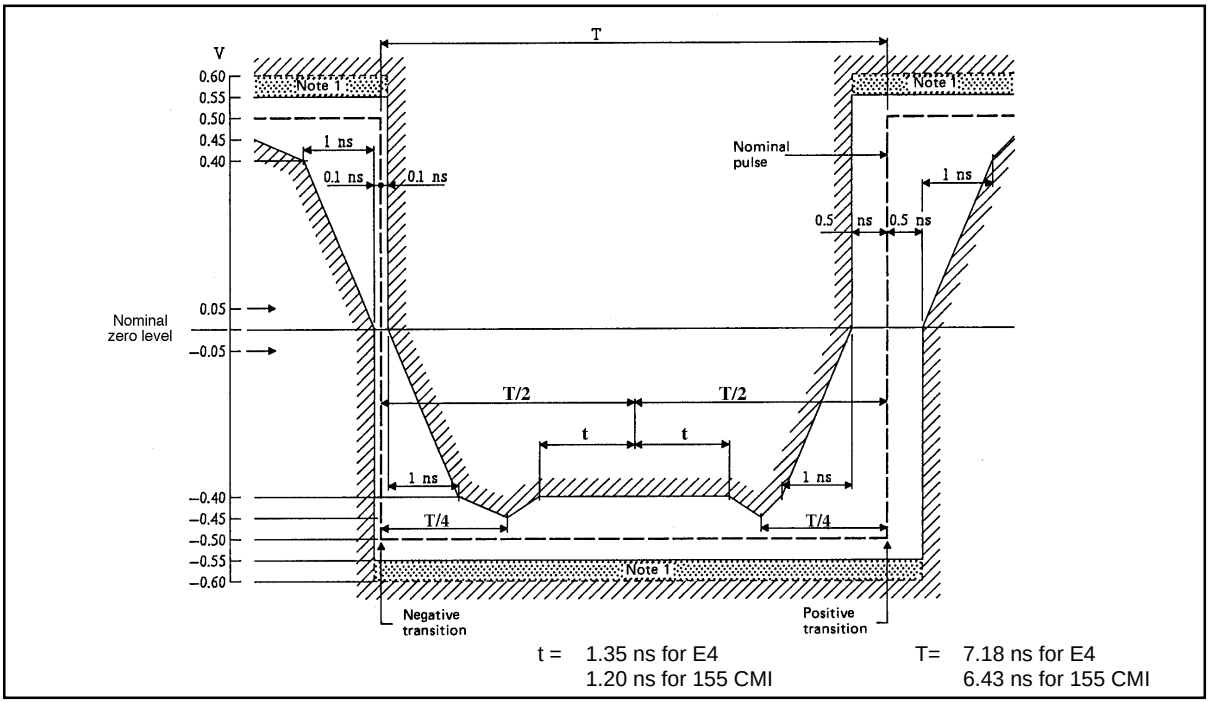
1. UI rms
2. UI p–p

Figure 7. Mask of a pulse corresponding to a binary 0 Compliant to G.703



T= 7.18 ns for E4
6.43 ns for 155 CMI

Figure 8. Mask of a pulse corresponding to a binary 1 Compliant to G.703



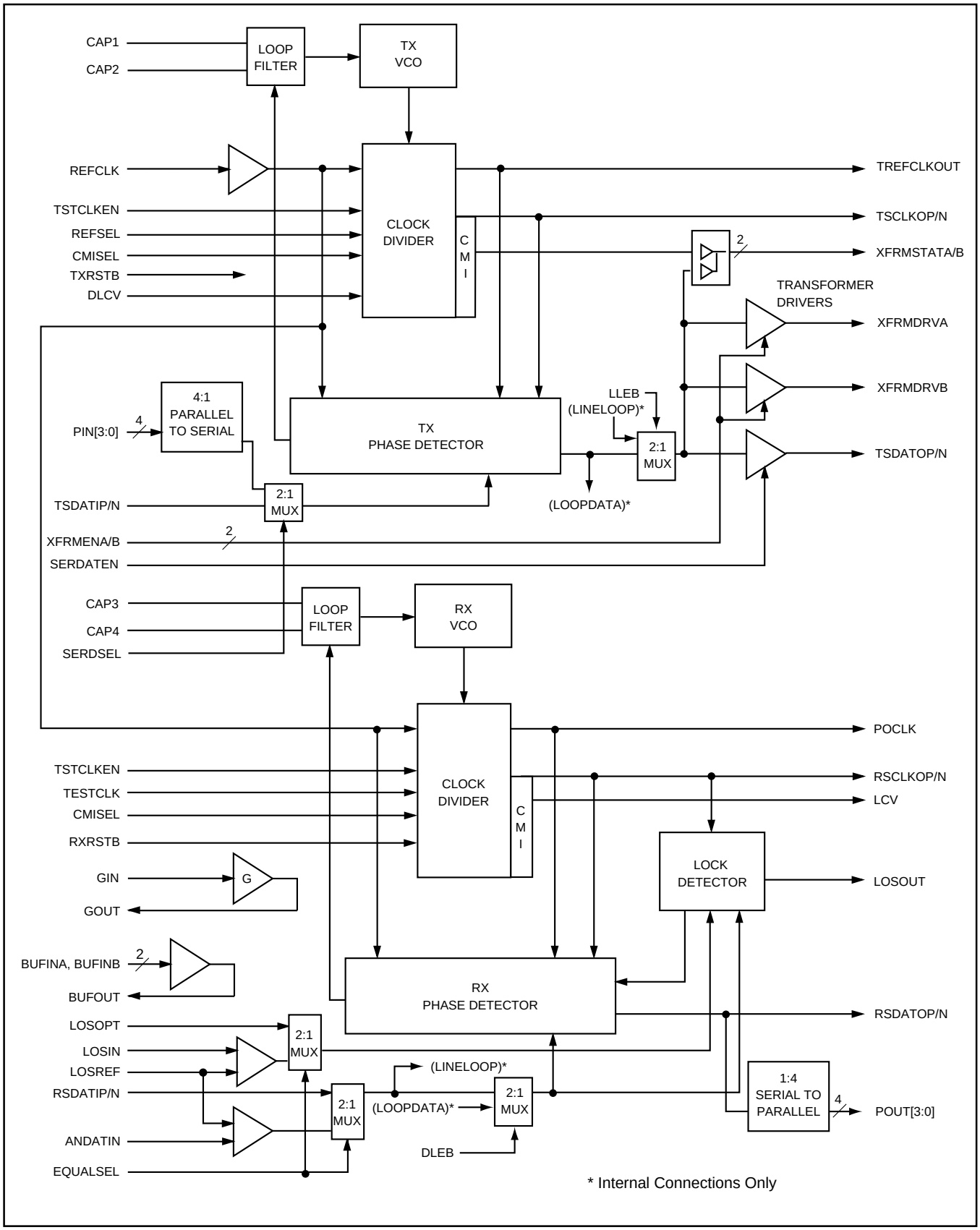
t = 1.35 ns for E4
1.20 ns for 155 CMI

T= 7.18 ns for E4
6.43 ns for 155 CMI

Notes:

1. The maximum “steady state” amplitude should not exceed the 0.55V limit. Overshoots and other transients are permitted to fall into the dotted area, bounded by the amplitude levels 0.55V and 0.6V, provided that they do not exceed the steady state level by more than 0.05V. The possibility of relaxing the amount by which the overshoot may exceed the steady state level is under study.
2. For the purpose of these masks, the rise time and decay time should be measured between -0.4V and 0.4V, and should not exceed 2 ns.
3. The inverse pulse in Figure 8 will have the same characteristics, noting that the timing tolerances at the zero level of the negative and positive transitions are ±0.1 ns and ±0.5 ns respectively.

Figure 9. S3031B OC-3/STM-1/E4 Transceiver



S3031B RECEIVER OPERATION

The S3031B transceiver chip provides the first stage of the digital process of a receive SONET STS-3 or ITU-T E4 serial bit stream. A Coded Mark Inversion (CMI) decoder can be enabled for decoding STS-3 electrical and E4 signal. The recovered and decoded signal is output as both retimed bit-serial 155.52 or 139.264 Mbps NRZ data and as a 38.88 or 34.816 Mbyte/s 4-bit nibble parallel outputs.

Clock recovery is performed on the incoming scrambled NRZ or CMI-coded data stream. A reference clock is required for phase locked loop start-up and proper operation under loss of signal conditions. An integral prescaler and phase locked loop circuit is used to multiply this reference frequency to the nominal bit rate.

Clock Recovery

The clock recovery function, as shown in the block diagram in Figure 9, generates a clock that is frequency matched to the incoming data baud rate at the RSDATIP/N differential inputs. The clock is phase aligned by a PLL so that it samples the data in the center of the data eye pattern.

The phase relationship between the edge transitions of the data and those of the generated clock are compared by a phase/frequency discriminator. Output pulses from the discriminator indicate the required direction of phase corrections. These pulses are smoothed by an integral loop filter. The output of the loop filter controls the frequency of the Voltage Controlled Oscillator (VCO), which generates the recovered clock. Frequency stability without incoming data is guaranteed by an alternate reference input (REFCLK) to which the PLL locks when data is lost.

When the Test Clock Enable (TSTCLKEN) input is set high, the clock recovery block is disabled. The Test Clock (TESTCLK) is used as the bit rate clock input in place of the recovered clock. This feature is used for functional testing of the device.

The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET or E4 data signal. This transfer function yields a typical capture time of 16 µs for random incoming NRZ data.

The total loop dynamics of the clock recovery PLL yield a jitter tolerance which exceeds the minimum tolerance proposed for OC-3/STM-1/E4 equipment by the Bellcore and ITU-T documents, shown in Figure 12.

Optical and Electrical Interfaces

The digital data inputs (RSDATIP/N) are the PECL inputs from an optical to electrical converter, as shown in Figure 16. The data input for the coaxial interface is ANDATIN, which is the serial data input from the equalizer circuit and should be connected as shown in Figure 19. The EQUALSEL input is used to select either RSDATIP/N or ANDATIN.

CMI Decoding

The CMI decoder block on the S3031B accepts serial data from the TSDATIP/N input at the rate of 139.264 or 155.52 Mbps. The incoming CMI data, which has transitions that represent this data rate (the clock associated with this data would be running at twice this rate), is then decoded from CMI to NRZ format.

Loss of Signal

The clock recovery circuit monitors the incoming data stream for loss of signal. If the incoming encoded data stream has had no transitions continuously for 100 to 200 recovered clock cycles, loss of signal is declared and the PLL will switch from locking onto the incoming data to locking onto the reference clock per the requirements of G.775. Alternatively, the loss-of signal (LOSIN) input can force a loss-of-signal condition. This signal is compared internally against the LOSREF input reference voltage. This input can be set to meet the conditions shown in Figure 10. If the zero to peak signal level drops below the LOSREF/20 voltage level for more than 100 to 200 bit intervals, a loss of signal condition will be indicated on the LOSOUT pin and the PLL will change its reference from the serial data stream to the reference clock. When the peak input voltage is greater than LOSREF/10, the loss of signal condition will be deasserted and the PLL will recover the clock from the serial data inputs.

In clock recovery mode, the receiver PLL also monitors the reference clock with respect to the VCO. If the VCO drifts away from the local reference clock by more than 1000 ppm the PLL will re-lock to the reference clock and the LOSOUT will be set to the active low condition.

The LOSOUT will return to the High or inactive state and the PLL will again lock to the data if the serial data contains sufficient transition density (less than 100 to 200 bit times between rising edges), and the serial clock is within 250 ppm of the reference clock determined frequency.

In NRZ mode, a logic Low level on the LOSOPT input will cause the PLL to change its reference to the reference clock. This pin should be driven by a PECL compatible level signal detect signal from the fiber optic receiver.

Serial Clock Output to Data Output Timing

The serial data is clocked out on the falling edge of RSCLKOP. (See Figure 11.) This timing is valid in both NRZ and CMI modes.

Serial to Parallel Converter

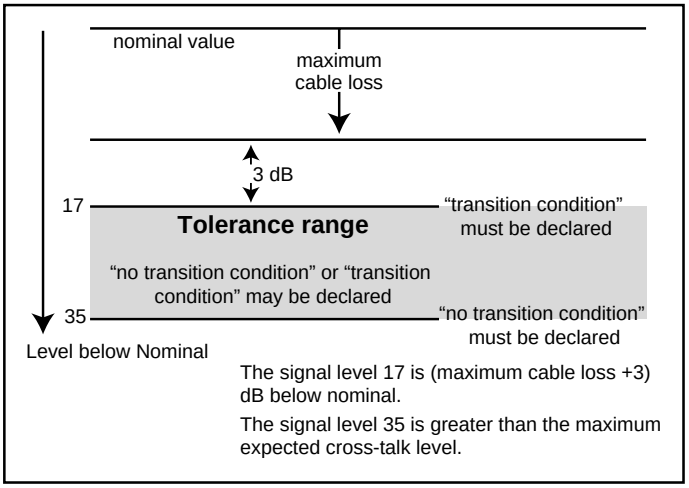
The Serial to Parallel Converter consists of two 4-bit registers. The first is a serial-in, parallel-out shift register, which performs serial to parallel conversion clocked by the clock recovery block. The second is the output holding register. On the falling edge of the free running POCLK, the data in the serial-in, parallel-out register is transferred to the output holding register which drives POUT[3:0].

Input Jitter Tolerance

Input jitter tolerance is defined as the peak to peak amplitude of sinusoidal jitter applied on the input signal that causes an equivalent 1 dB optical/electrical power penalty. OC-3 and E-4 input jitter tolerance requirements are shown in Figure 12.

The S3031B PLL complies with the minimum jitter tolerance for clock recovery proposed for SONET/SDH equipment defined by the Bellcore TA-NWT-000253 standard when used as shown in Figure 12. The S3031B PLL also complies with the minimum jitter tolerance for clock recovery as defined in the ITU-T E4 specification when used as shown in Figure 19.

Figure 10. Criteria for Determination of Transition Conditions. Compliant to G.775.



Reference Clock Input

The reference clock input seen in Figure 9 provides backup reference clock signals to the clock recovery block when the clock recovery block detects a loss of signal condition. It contains a counter that divides the clock output from the clock recovery block down to the same frequency as the Reference Clock (REFCLK).

Figure 11. S3031B Clock to Data Timing

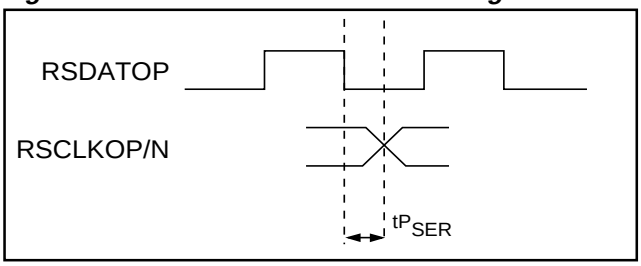
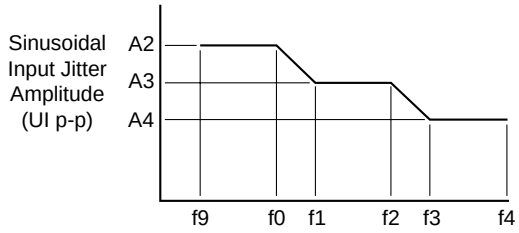


Figure 12. Clock Recovery Jitter Tolerance Compliant to G.823 and G.825



	f9 (Hz)	f0 (Hz)	f1 (Hz)	f2 (kHz)	f3 (kHz)	f4 (MHz)	A2	A3	A4
OC-3	10	30	300	6.5	65	—	15	1.5	0.15
STM-1 (Optical)	0.125	19.3	500	6.5	65	1.3	39[1]	1.5	0.15
STM-1 (Electrical)	0.125	19.3	500	6.5	65	1.3	39[1]	1.5	0.15
E4	TBD	TBD	200	0.5	10	3.5	15	1.5	0.075

Note:
1. Only tested to 20 due to test equipment limitation.

Table 2. Transmitter Input Pin Assignment and Description

Pin Name	Level	I/O	Pin #	Description
TSTCLKEN	TTL	I	26	Test Clock Enable. Active High. Enables the TESTCLK clock to be used in place of the VCO for testing. Allows a means of testing the functions of the chip without the use of the PLL.
DLCV	Single-ended PECL	I	86	Diagnostic Line Code Violation. Set High to force a CMI line code violation. DLCV is only active in CMI mode. DLCV is sampled on the falling edge of TSCLKOP. DLCV does not affect XFRMSTATB or XFRMSTATB.
CMISEL	TTL	I	27	CMI Select. Used to select a CMI or NRZ. A logic High selects CMI mode. A logic Low selects NRZ mode. Both the TSDATOP/N and the XFRMDRV outputs are controlled by CMISEL.
TXRSTB	TTL	I	97	Transmitter Reset. Active Low. Initializes the device to a known state. Serial data outputs are held to zero, and the Transformer Driver and Status outputs are forced Low.
CAP1 CAP2		I	21 22	Loop Filter Capacitor Network. The loop filter capacitor network is connected to these pins. The capacitor value should be 1.0 µF ±10%, X7R dielectric. The resistors should be 100 Ω for serial mode and 1000 Ω for nibble mode operation. See Figure 18.
XFRMENA	TTL	I	92	Transformer Driver Enable. Used to enable the transformer driver output. A logic Low enables XFRMDRVA. A logic High turns off the transformer driver output.
XFRMENB	TTL	I	94	Transformer Driver Enable.Used to enable the transformer driver output. A logic Low enables XFRMDRVB. A logic High turns off the transformer driver output.
SERDATEN	TTL	I	8	Serial Data Enable. Used to enable the transmit serial data outputs. A logic Low enables TSDATOP/N. A logic High turns off the serial data outputs.
PIN3 PIN2 PIN1 PIN0	TTL	I	1 100 99 98	Parallel Data Input. A 38.88 Mbyte/sec 4-bit wide Nibble aligned to the REFCLK reference clock. REFSEL and SERDSEL must both be at logic Low for transmitter operation with the nibble inputs.
TSDATIP TSDATIN	Diff. PECL	I	15 16	Transmit Serial Data In. The transmit clock is derived from transitions on these inputs when SERDSEL is High. No phase relationship to REFCLK is required. Either 19.44 MHz or 38.88 MHz reference operation may be selected. SERDSEL must be at logic High for transmitter operation with the serial data input.

Table 3. Transmitter Output Pin Assignment and Description

Pin Name	Level	I/O	Pin #	Description
TSDATOP TSDATON	Diff. PECL	O	12 13	Transmit Serial Data Out. In NRZ mode, this signal is the delayed version of the incoming data stream (TSDATIP/N) updated on the falling edge of Serial Clock Out (TSCLKOP). In CMI mode, this signal is the CMI-encoded version of TSDATIP/N.
TSCLKOP TSCLKON	Diff. PECL	O	9 10	Transmit Serial Clock Out. This signal is a 155.52 MHz clock that is phase–aligned with Transmit Serial Data Out in NRZ mode. In CMI mode, TSCLKOP/N cannot be used.
TREFCLKOUT	TTL	O	95	Transmit Reference Clock Out. Single-ended TTL reference clock output.
XFRMDRVA	Analog	O	89	Transformer Driver A. Used to drive the transformer of the electrical interface. For E4 operation this output should be connected per Figure 19 to provide the correct G.703 compatible output levels from the transformer when connected to the specified 75Ω cable.
XFRMDRVB	Analog	O	88	Transformer Driver B. Used to drive the monitor transformer of the electrical interface. This output should be connected per Figure 19 to provide the correct output levels from the transformer when connected to the specified 75Ω cable.
XFRMSTATA	TTL	O	93	Transformer Drive A Status. When High, the XFRMDRVA output is enabled, CMI mode is correctly selected, and the PLL is locked to switching data at the TSDATIP/N or PIN[3:0] input. Logic Low indicates deselection or code error.
XFRMSTATB	TTL	O	91	Transformer Drive B Status. When High, the XFRMDRVB output is enabled, CMI mode is correctly selected, and the PLL is locked to switching data at the TSDATIP/N or PIN[3:0] input. Logic Low indicates deselection or code error.

Table 4. Receiver Input Pin Assignment and Description

Pin Name	Level	I/O	Pin #	Description
BUFINA BUFINB	Analog	I	30 31	Buffer Inputs. Inputs to the equalizer network buffer circuit. This circuit provides a high impedance load to the transformer termination network in order to comply with the required return loss specifications. These pins should be connected as shown in Figure 19. These pins are electrically equivalent.
ANDATIN	Analog	I	46	Analog Data In. This is the serial data input from the equalizer circuit. It must be connected to the output of the equalizer circuit as shown in Figure 19. When the S3031B is used with a fiber optic receiver this input should be left open and the RSDATIP/N inputs should be used.
EQUALSEL	TTL	I	51	Equalization Select Used to select RSDATIP/N or ANDATIN. A logic High selects ANDATIN.
RSDATIP RSDATIN	Diff. PECL	I	66 65	Receive Serial Data In. Clock is recovered from transitions on these inputs when selected by EQUALSEL.
RXRSTB	TTL	I	75	Receiver Reset. Active Low. Initializes the device to a known state, shuts off RSCLKOP/N, and forces the PLL to acquire to the reference clock. A reset of at least 16 ms should be applied at power-up and whenever it is necessary to reacquire to the reference clock. The S3031B will also reacquire to the reference clock if the serial data is held quiescent (constant ones or constant zeros), or LOSIN or LOSOPT are activated for at least 224 bit intervals.
GIN	Analog	I	36	Input to 25dB gain block for internal equalizer function.
LOSIN	Analog	I	48	Loss of Signal In. A single-ended input that indicates a loss of received signal. When the signal level at LOSIN drops below the voltage level set by LOSREF for greater than 100 to 200 bit intervals, the data on Serial Data Out (RSDATOP/N) will be forced to a constant low, and the PLL will change its reference from the serial data stream to the reference clock. This input is to be driven by the external bandpass filter and peak detect circuit as shown in Figure 19. This signal must be used to assure correct automatic reaquisition to serial data following an interruption and subsequent reconnection of the data path. This will assure that the PLL does not “ wander” out of reaquisition range when no signal is applied. When LOSIN is inactive, data on the RSDATIP/N pins will be processed normally.

Table 4. Receiver Input Pin Assignment and Description (Continued)

Pin Name	Level	I/O	Pin #	Description
LOSOPT	PECL	I	52	Loss of Optical Signal. Active Low. This input has the same functionality as LOSIN, except that it is used in optical mode instead of electrical. It should be driven by the external optical receiver module to indicate a loss of received optical power.
LOSREF	Analog	I	49	Loss of Signal Reference. Sets the comparator levels for LOSIN. (See Table 11.)
CAP3 CAP4		I	60 59	Loop Filter Capacitor Network. The loop filter capacitor network is connected to these pins. The capacitor value should be 1.0µF ± 10% tolerance, X7R dielectric. The resistors should be 51 Ω. See Figure 18.

Table 5. Receiver Output Pin Assignment and Description

Pin Name	Level	I/O	Pin #	Description
LOSOUT	TTL	O	74	Clock recovery indicator. Active Low. Set High when the internal clock recovery has locked onto the incoming datastream. LOSOUT is an asynchronous output. This output is deasserted when there is no incoming serial data input or when the received signal has dropped below the reference voltage set by LOSREF for more than 100 to 200 bit intervals. In this case the PLL locks to the reference clock. In clock recovery mode, the receiver PLL also monitors the reference clock with respect to the VCO. If the VCO drifts away from the local reference clock by more than 1000 ppm the PLL will re-lock to the reference clock and the LOSOUT will be set to the active Low condition. The LOSOUT will return to the High or inactive state and the PLL will again lock to the data if the serial data contains sufficient transition density (less than 100 to 200 bit times between rising edges), and the serial clock is within 250 ppm of the reference clock determined frequency.
RSDATOP RSDATON	Diff. PECL	O	69 68	Receive Serial Data Out. This signal is the NRZ data output. It can be either a delayed version of the NRZ data input (NRZ mode) or the decoded CMI data (CMI mode). RSDATOP/N is updated on the falling edge of RSCLKOP as shown in Figure 11.
RSCLKOP RSCLKON	Diff. PECL	O	72 71	Receive Serial Clock Out. This signal is phase–aligned with Serial Data Out (RSDATOP). (See Figure 11 and Table 7 for timing.)
LCV	Single-Ended PECL	O	73	Line Code Violation. Set High to indicate that the current bit contains a CMI line code violation in CMI mode. LCV is updated on the falling edge of RSCLKOP/N. LCV output is undefined when running in NRZ mode.
BUFOUT	Analog	O	33	Buffer Output to the equalizer network buffer circuit. This circuit provides a low impedance driver to the equalizer circuit. This pin should be connected as shown in Figure 19 to drive the equalizer network.
POUT3 POUT2 POUT1 POUT0	TTL	O	79 80 81 82	Parallel 4-bit wide output data bus, aligned to the parallel output clock (POCLK). POUT3 is the first bit transmitted, POUT0 is the fourth bit transmitted. POUT[3:0] is updated on the falling edge of POCLK.
POCLK	TTL	O	78	Parallel Output Clock. A 38.88 MHz nominally 50% duty cycle, nibble rate output clock that is aligned to the POUT[3:0] nibble serial output data.
GOUT	Analog	O	44	Output of 25dB gain block for the internal equalizer function. To be AC coupled to ANDATIN. See Figure 19.

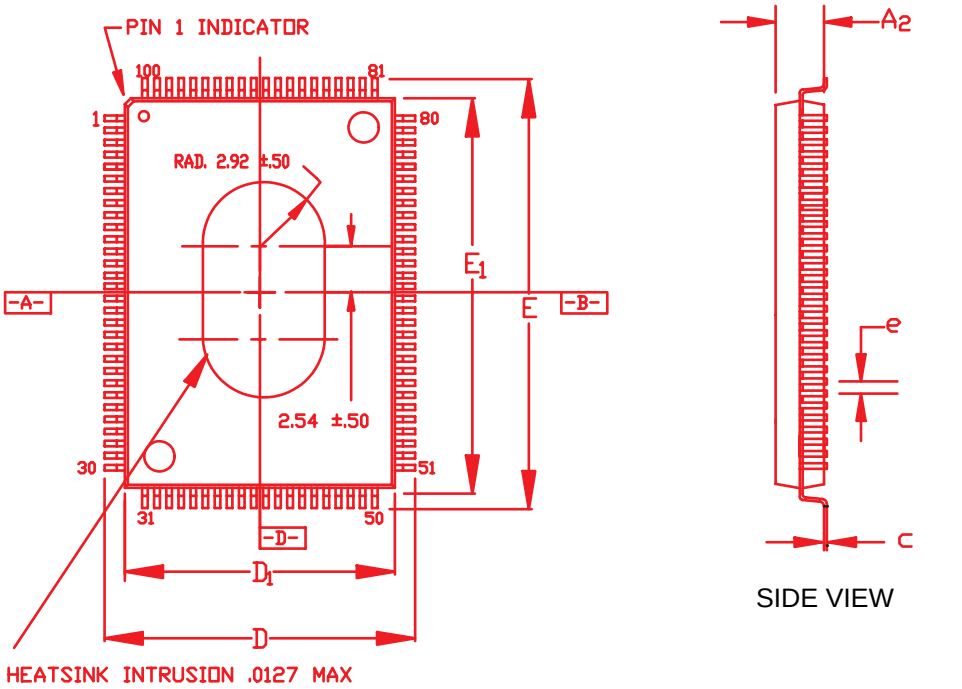
Table 6. Common Pin Assignment and Description

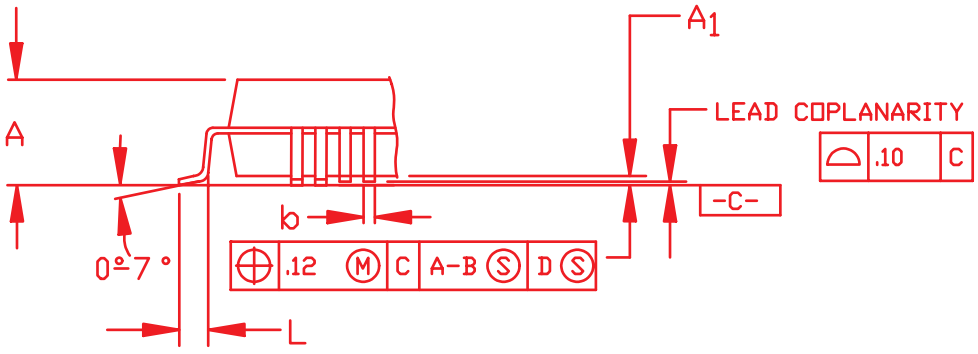
Pin Name	Level	I/O	Pin #	Description
REFCLK	TTL	I	6	Reference Clock. Input used as the reference for the receiver VCO in the absence of received serial data. Used as the reference for the transmitter VCO in the serial input mode and in the absence of transmitter serial input data. In parallel transmit interface mode REFCLK is used as the reference for the internal bit clock frequency synthesizer and as the parallel load clock for the PIN[3:0] data.
REFSEL	TTL	I	53	Reference Select. Used to select the reference clock frequency. A logic Low selects 38.88 or 34.816 MHz reference, and logic High selects 19.44 or 17.408 MHz.
SERDSEL	TTL	I	96	Serial Data Select. Active High. Used to select the Transmit Serial Data inputs (TSDATIP/N) and enable the Receiver Serial Data outputs (RSDATOP/N). In this mode the POUT[3:0] outputs are held Low. When SERDSEL is held at logic Low, the parallel inputs PIN[3:0] are selected and the the parallel outputs POUT[3:0] are enabled.
DLEB	TTL	I	85	Diagnosatic Loopback Enable. Active High. Selects diagnostic loopback. When DLEB is Low, the S3031B receiver section uses the RSDATIP/N or ANDATIN data inputs. When High, the S3031B receiver section uses the data from the transmitter section output.
LLEB	TTL	I	84	Line Loopback Enable. Active High. Selects Line Loopback. When LLEB is High the S3031B will route the data from the selected RSDATIP/N or ANDATIN inputs directly to the TSDATOP/N or XFRMDRVA/B outputs as selected.
TESTCLK	TTL	I	28	Test Clock. Used during device testing to bypass the VCO of the PLLs.
TXCRVEE TSVEE AVEE1 AVEE0 AVEE4 AVEE5 AVEE6 AVEE7 RXCRVEE AVEE2 AVEE3 RSVEE RXIOVEE TXIOVEE TXINVEE	GND		5 14 19 24 32 37, 38 39 50 54 57 62 64 76 90 2	Ground 0V

Table 6. Common Pin Assignment and Description (Continued)

Pin Name	Level	I/O	Pin #	Description
TXCRVCC TSVCC AVCC1 AVCC0 AVCC4 AVCC5 AVCC6 AVCC7 RXCRVCC AVCC2 AVCC3 RSVCC RXIOVCC TXIOVCC TXINVCC	VCC		4 11 18 25 29 34, 35 43 47 55 56 63 67 77 87 3	Power Supply (5V)
REFGND	GND		7	Ground (0V)
GND	GND		17 45 70 83	Gound (0V)
CGND	GND		20 23 58 61	Ground (0V)
NC			40 41 42	Not Connected.

Figure 13. 100-Pin PQFP/TEP Package





DIMENSIONS (are in millimeters)

UNIT	A	A_1	A_2	D	D_1	E	E_1	L	e	b
MIN		0.25	1.90	17.00	13.90	23.00	19.90	0.78	0.65 BASIC	0.25
NOM			2.00	17.20	14.00	23.20	20.00	0.88		0.30
MAX	2.35	0.50	2.10	17.40	14.10	23.40	20.10	1.03		0.35

Thermal Management

Device	Power	Θja Still Air w/DW0045-28	Max Still Air[1] w/DW0045-28
S3031	1.92W	19˚C/W	85˚C

1. Max ambient temperature permitted in still air to maintain Tj < 130˚C.

Figure 14. Heat Sink Drawing DW0045-28

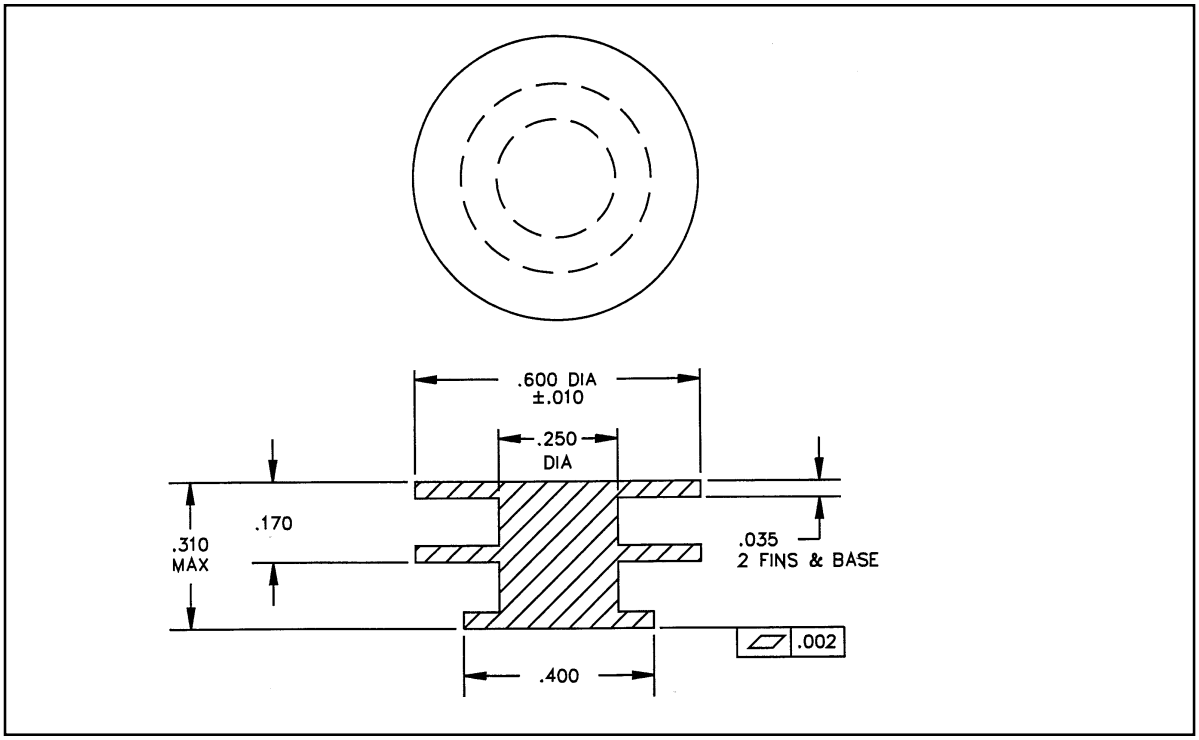


Figure 15. S3031B Pinout

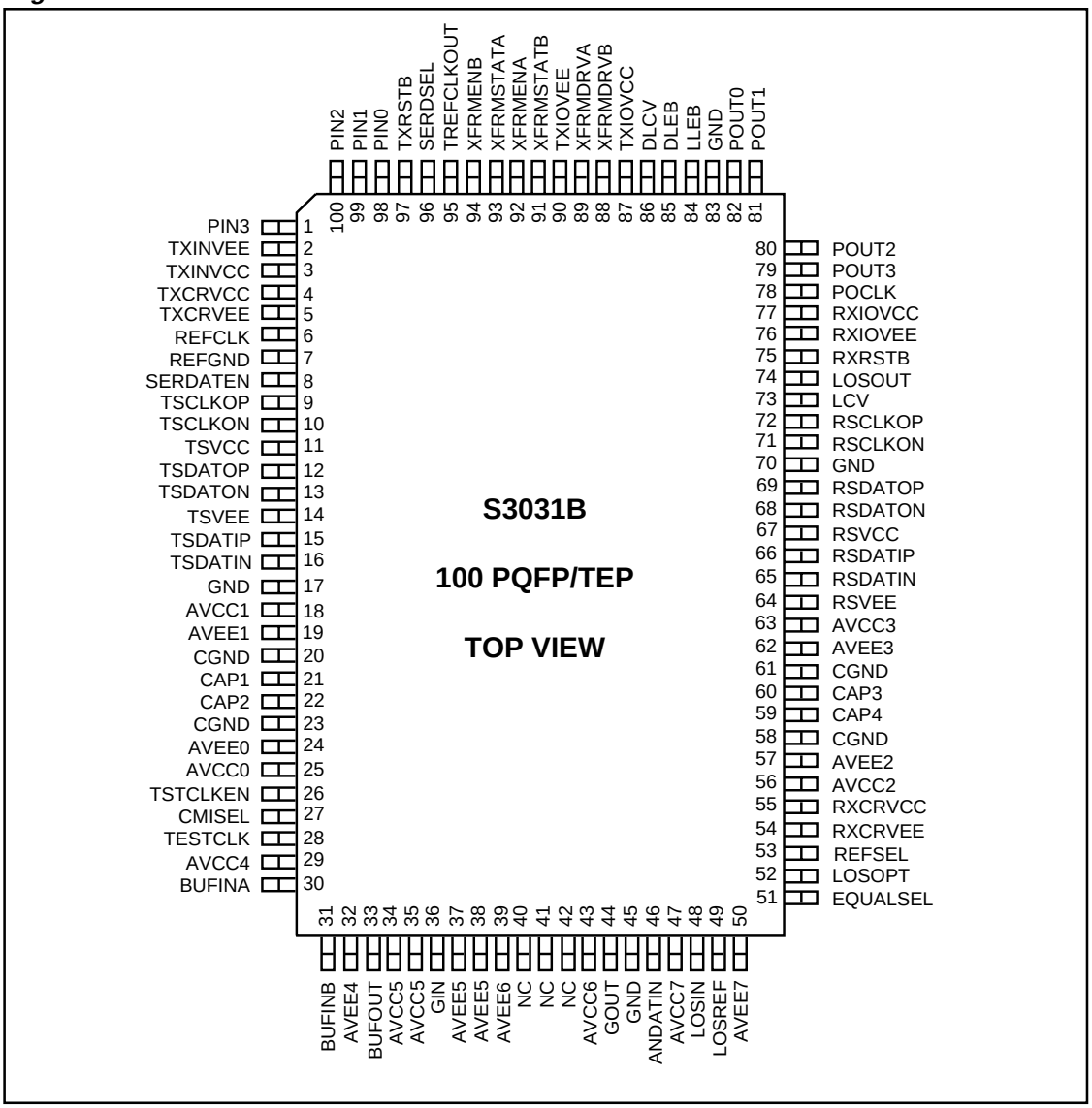


Table 7. S3031B Clock Recovery Mode Performance Specifications

Parameter	Min	Typ	Max	Units	Condition
Nominal VCO Center Frequency		622.08		MHz	Given REFCLK = VCO ÷32
OC–3/STS–3		+8, -12		%	With respect to fixed reference frequency.
Acquisition Lock Time[1]			64	µsec	With device already powered up and valid REFCLK.
Reference Clock Input Duty Cycle	30		70	% of UI	
Reference Clock Rise & Fall Times			5.0	ns	20% to 80% of amplitude.
PECL Output Rise & Fall Times			850	ps	20% to 80%, 50Ω load, 5 pF cap.
Reference Clock Frequency Tolerance	-100		100	ppm	
tP_{SER} RSCLKOP Falling to RSDATO Valid Prop Delay	100		1000	ps	See Figure 11.

1. Specification based on design values. Not tested.

Table 8. S3031B Clock Synthesis Mode Performance Specifications

Parameter	Min	Typ	Max	Units	Condition
PECL Data Output Jitter (RSDATOP/N) OC-3/STS-3			64	ps (rms)	In CSU mode, Given • 56 ps rms jitter on REFCLK in 12kHz to 1MHz band
E4-STS-3 CMI			32		• 28 ps rms jitter on REFCLK in 12kHz to 1MHz band
Reference Clock Frequency Tolerance Clock Synthesis	-20		+20	ppm	Required to meet SONET output jitter generation specification.

Table 9. Electrical Characteristics for Transformer Driver[1]

(V_{CC} = +5V, T_A = +25°C, input AC coupled unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Condition
Operating Frequency		155.52		MHz	270Ω 11 3pF load.
VSWR [2]		1.3:1	1.5:1		75Ω AC Coupled Termination.

1. For output waveform characteristics, see Figures 7 and 8. The S3031B is compliant with these masks on an individual waveform basis. The total cycle-to-cycle wideband jitter is less than 350 ps peak-to-peak. Total transmitted jitter per ITU G.825 is less than 0.075 UI peak-to-peak.
2. Up to 250 MHz.

Table 10. Electrical Characteristics for ANDATIN Input

(V_{CC} = +5V, T_A = +25°C, input AC coupled unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Peak-to-Peak Input Voltage Range	V_{iptp}			1.3	V	
Common-Mode Rejection Ratio	CMRR[1]	40			dB	
Power-Supply Rejection Ratio	PSRR[1]	40			dB	
Input Sensitivity	S_{IN}	110			mV	T_A = Min to Max
DC Offset at Input [2]				Vcc -1V	V	

1. Up to 300 kHz.
2. Signal is undefined if left floating.

Table 11. Electrical Characteristics for LOSIN Input

(V_{CC} = +5V, T_A = +25°C, input AC coupled unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Peak-to-Peak Input Voltage Range	V_{iptp}			1.1	V	
Common-Mode Rejection Ratio	CMRR[1]	40			dB	
Power-Supply Rejection Ratio	PSRR[1]		35		dB	
Signal Level for LOS Detected[3]		LOS-REF/30	LOS-REF/20	LOS-REF/10	V/V	T_A = Min to Max
Signal Level for LOS Cleared[3]		LOS-REF/15	LOS-REF/10	LOS-REF/5	V/V	T_A = Min to Max
Hysterisis between "Trans. Cond." and "No Trans. Cond."[2]		4	6		dB	

1. Up to 300 kHz.
2. LOSREF >0.5 volts.
3. LOS detected and LOS cleared will maintain 2:1 ratio ±5%.

Table 12. Typical Operating Conditions

Voltage Applied at LOSREF	Compare Voltage #1	Compare Voltage #2	Hysterisis
1.4 Volts	140 mV ± 0.6dB	70 mV ± 1dB	6dB +1.6 -1.4dB
0.7 Volts	70 mV ± 1dB	35 mV ± 1.6dB	6dB +2.7 -2.0dB
0.3 Volts	30 mV ± 1.6dB	15 mV ± 3.5dB	6dB +6.0 -3.7dB

Table 13. Electrical Characteristics for BUFIN, BUFOUT

(At V_{CC} = +5VDC, R_{LOAD} = 75Ω AC coupled and T_A = 25˚C unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Output Characteristics (BUFOUT) Voltage Output: Output Resistance:		 ±0.6 1	 ±0.8 3	 8	 V Ω	
Transfer Characteristics Gain (BUFIN to BUFOUT)[1]		0.85	0.93	1.1	V/V	
VSWR[2]	VSWR		1.3:1	1.5:1		With 75Ω AC Coupled termination
Harmonic Distortion[2]	HD	35 30 25	40 35 30		dBc	Input = 0.3V p-p Input = 0.6V p-p Input = 1.2V p-p
DC Input Bias		Vcc -0.85			V	Input externally AC Coupled
DC Output Bias		Vcc -2.5			V	Output externally AC Coupled

1. Up to 300 MHz.
2. Up to 250 MHz.

Table 14. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Storage Temperature	-65		150	˚C
Voltage on V_{CC} with respect to Ground	-0.5		+7.0	V
Voltage on any TTL Input Pin	-0.5		+5.5	V
Voltage on any PECL Input Pin	Vcc -3		Vcc	V
TTL Output Sink Current			20	mA
TTL Output Source Current			10	mA
High Speed PECL Output Source Current			50	mA
Static Discharge Voltage[1]	500			V

1. Human body model.

Table 15. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Ambient Temperature Under Bias	-20		85	˚C
Junction Temperature Under Bias	-10		+130	˚C
Voltage on any V_{CC} with respect to Ground	4.75	5.0	5.25	V
Voltage on any TTL Input Pin	0		V_{CC}	V
Voltage on any PECL Input Pin	V_{CC} -2		V_{CC}	V
S3031B ICC		336	365	mA

Table 16. TTL Input/Output DC Characteristics

(T_A = -20°C to +85°C, V_{CC} = 5 V ±5%)

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	V_{IL} [1]			0.8	V	Guaranteed Input Low Voltage
Input High Voltage	V_{IH} [1]	2.0			V	Guaranteed Input High Voltage
Input Low Current	I_{IL}	-400.0			µA	V_{CC} = MAX, V_{IN} = 0.5 V
Input High Current	I_{IH}			50.0	µA	V_{CC} = MAX, V_{IN} = 2.7 V
Input High Current at max V_{CC}	I_I			1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V
Output Short Circuit Current	I_{OS}	-100.0		-25.0	mA	V_{CC} = MAX, V_{OUT} = 0.5 V
Input Clamp Diode Voltage	V_{IK}	-1.2			V	V_{CC} = MIN, I_{IN} = -18 mA
Output Low Voltage	V_{OL}			0.5	V	V_{CC} = MIN, I_{OL} = 4 mA
Output High Voltage	V_{OH}	2.7			V	V_{CC} = MIN, I_{OH} = -1 mA

1. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

Table 17. PECL Input/Output DC Characteristics[1,2]

(T_A = -20°C to +85°C, V_{CC} = 5 V ±5%)

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	V_{IL}	V_{CC} -2.000		V_{CC} -1.441	V	Guaranteed Input Low Voltage for single-ended inputs
Input High Voltage	V_{IH}	V_{CC} -1.225		V_{CC} -0.570	V	Guaranteed Input High Voltage for single-ended inputs
Input Low Voltage	V_{IL}	V_{CC} -2.000		V_{CC} -0.700	V	Guaranteed Input Low Voltage for differential inputs
Input High Voltage	V_{IH}	V_{CC} -1.750		V_{CC} -0.450	V	Guaranteed Input High Voltage for differential inputs
Input Differential Voltage	V_{ID}	0.250	0.500	1.400	V	Differential Input Voltage
Input High Current	I_{IH}	-0.500		20.000	µA	V_{ID} = 500 mV
Input Low Current	I_{IL}	-0.500		20.000	µA	V_{ID} = 500 mV
Output Low Voltage	V_{OL}	V_{CC} -2.000		V_{CC} -1.500	V	50 Ω termination to V_{CC} -2V
Output High Voltage	V_{OH}	V_{CC} -1.110		V_{CC} -0.670	V	50 Ω termination to V_{CC} -2V
Output Differential Voltage	V_{OD}	0.390		1.330	V	Differential Output Voltage

1. These conditions will be met with no airflow.
2. When not used, tie the positive differential PECL pin to V_{CC} and the negative differential ECL pin to ground via a 3.9 kΩ resistor.

Figure 16. Differential ECL Input Application

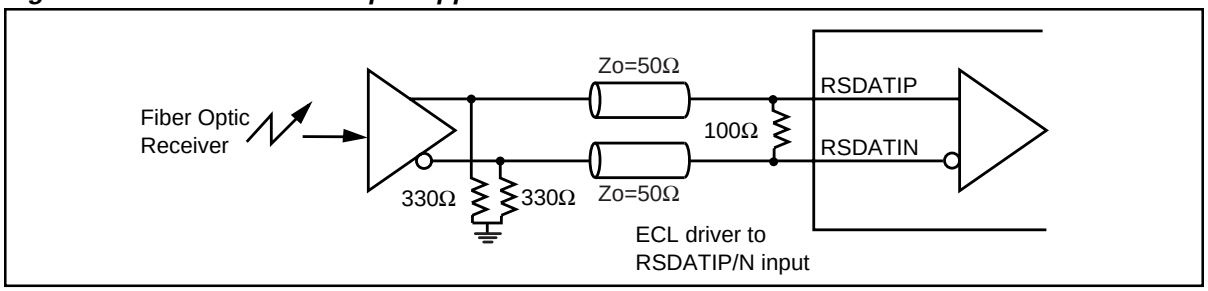


Figure 17. S3031B Differential ECL Output Application

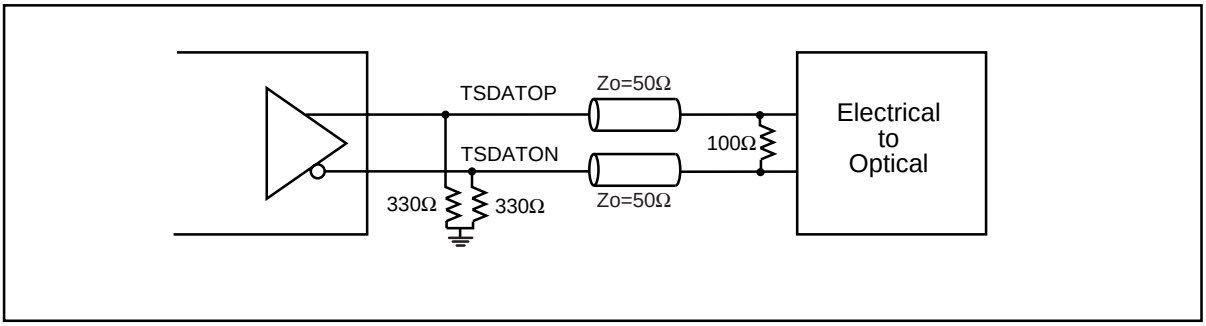
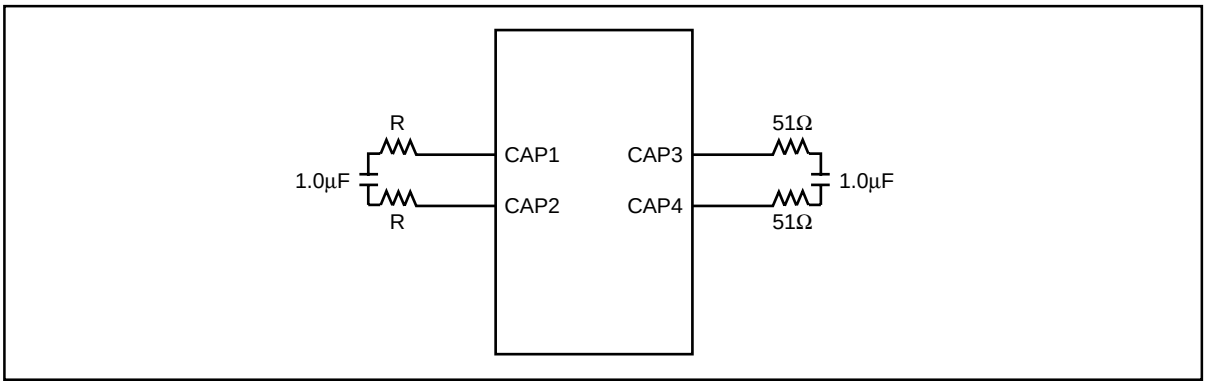


Figure 18. Loop Filter Capacitor Connections



Note: R = 100Ω for serial mode, and R = 1000Ω for nibble mode.

Figure 19. S3031B Transformer Input and Output Application

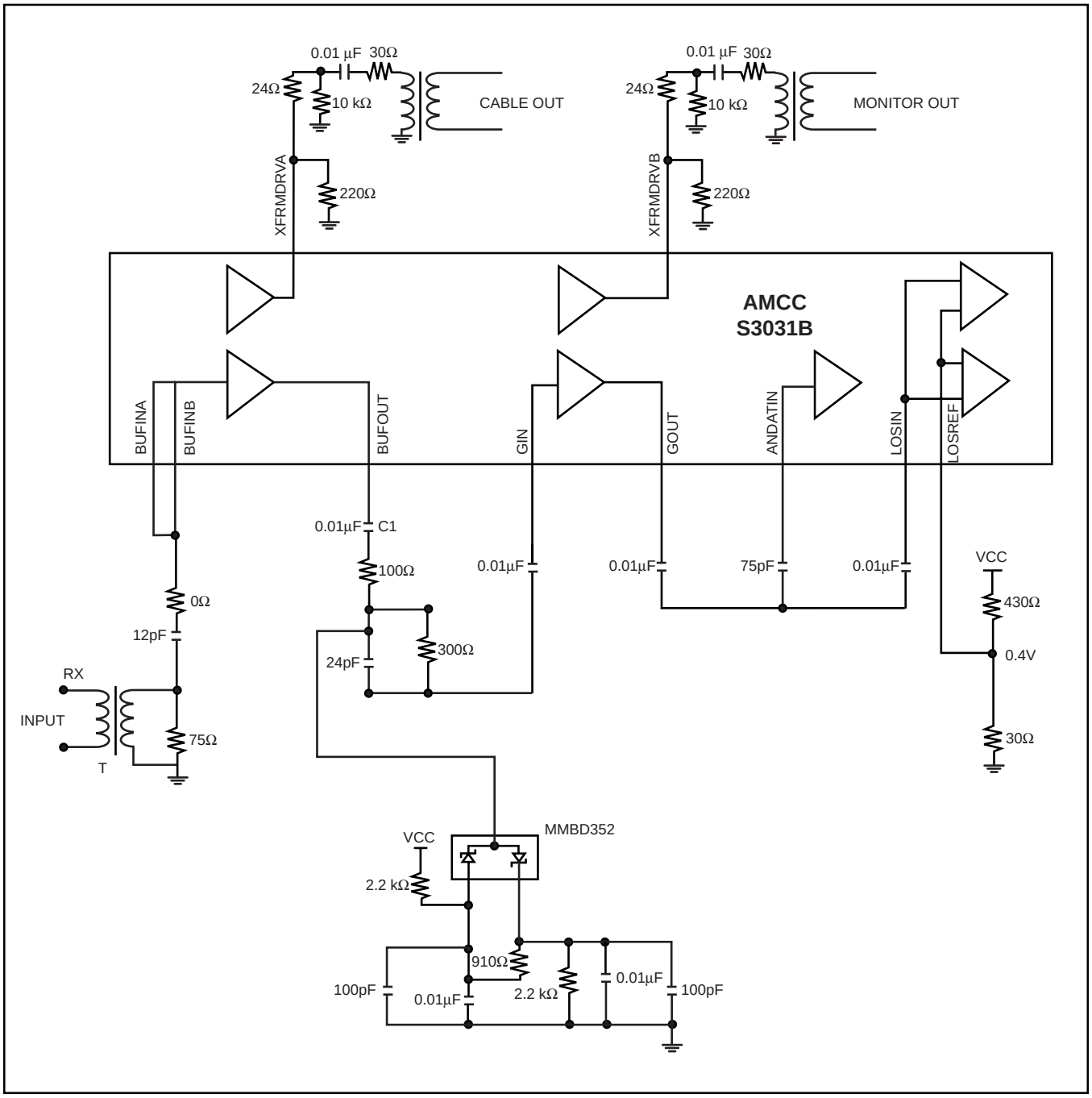


Figure 20. OC-3 Application

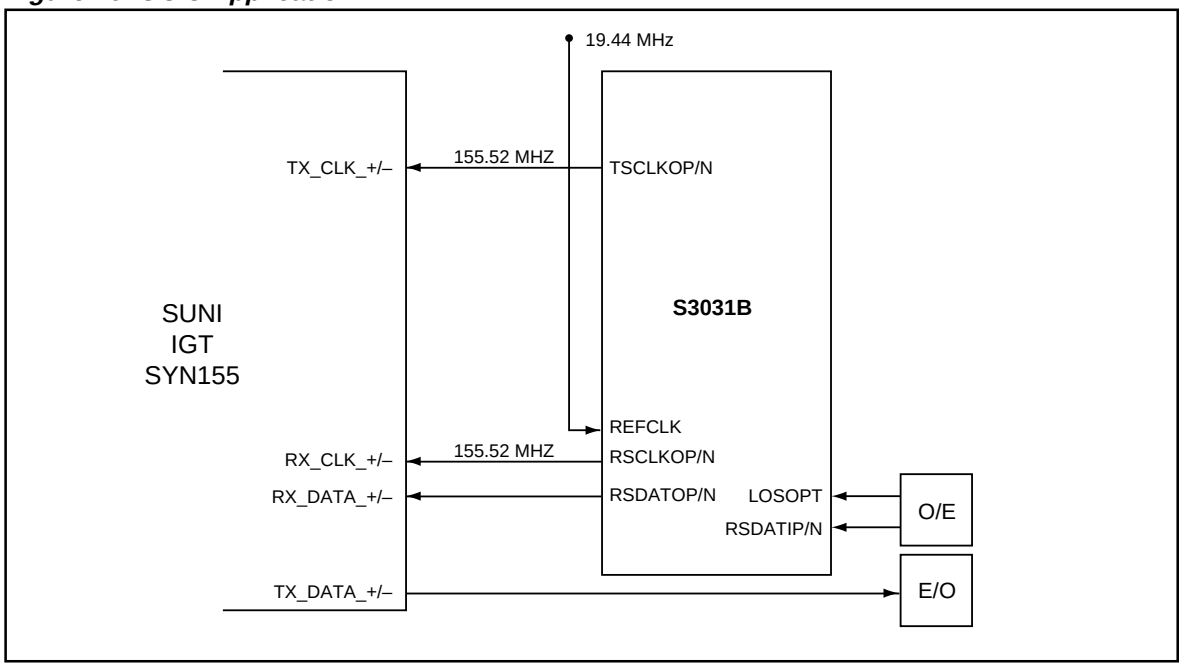


Figure 21. STM-1 CMI, E4 Application

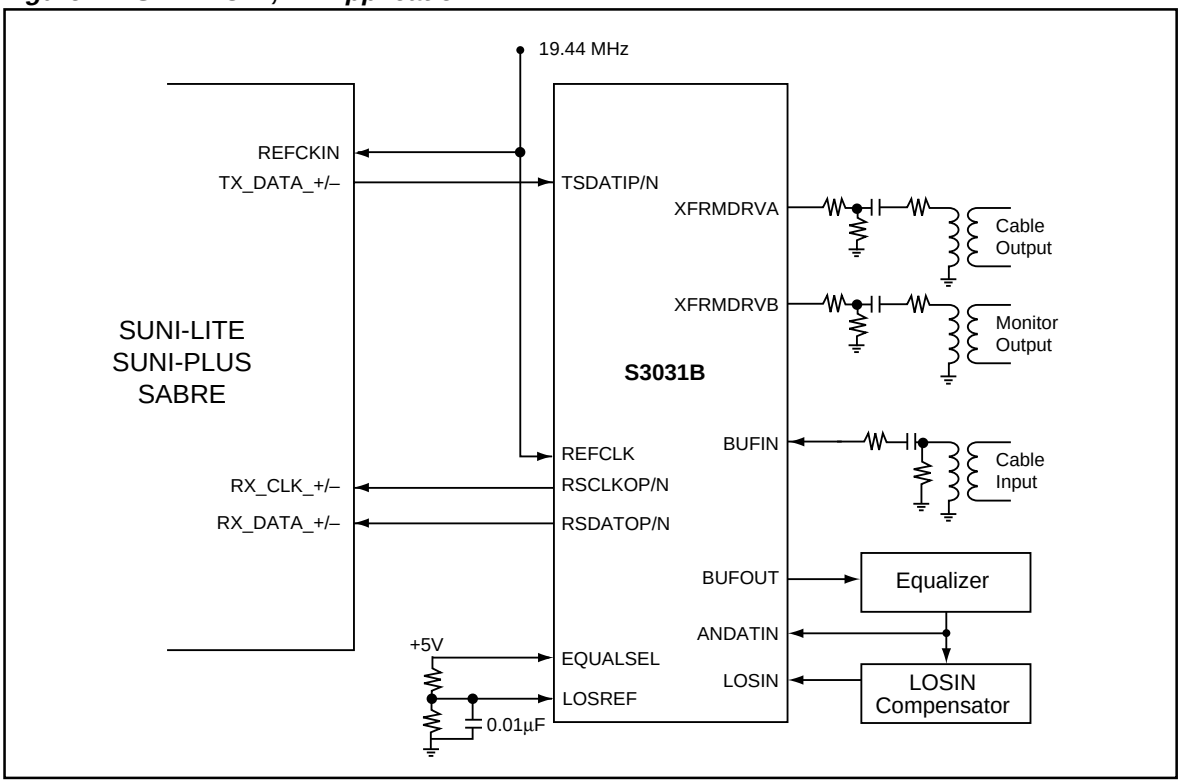
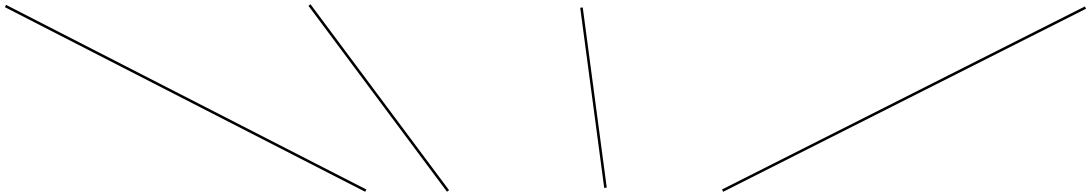


Table 18. Suggested Interface Devices

Processor Interface		
PMC PM5345	SUNI	Saturn User Network Interface
PMC PM5346	SUNI-Lite	Saturn User Network Interface
PMC PM5347	SUNI-Plus	Saturn User Network Interface
IGT WAC-013-A		SONET LAN ATM Processor
TRANSWITCH SYN155		155 Mbps Synchronizer
TI SABRE TDC 1500		155 Mbps Processor
Electrical Interface		
Motorola	MMBD352	Dual Diode
Mini-Circuits	MCL TXI-R5	Wideband RF Transformer (Surface Mount)
Mini-Circuits	MCL TO-75	Wideband RF Transformer (Through-Hole)
Optical Interface		
HP HFBR-520x	155 Mbps	Fiber Optic Transceiver
CTS ODL-1408X	155 Mbps	Fiber Optic Transceiver
Sumitomo SDM4123-XC	155 Mbps	Fiber Optic Transceiver
AMP 269039-1	155 Mbps	Fiber Optic Transceiver

Ordering Information

GRADE	RECEIVER	PACKAGE	OPTION
S – industrial	3031	B – 100 PQFP/TEP w/DW0045-28 heatsink unattached	H0 – No Heatsink



X XXXX X / XX

Grade Part number Package H0 for no heatsink (identifier not marked on part)

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