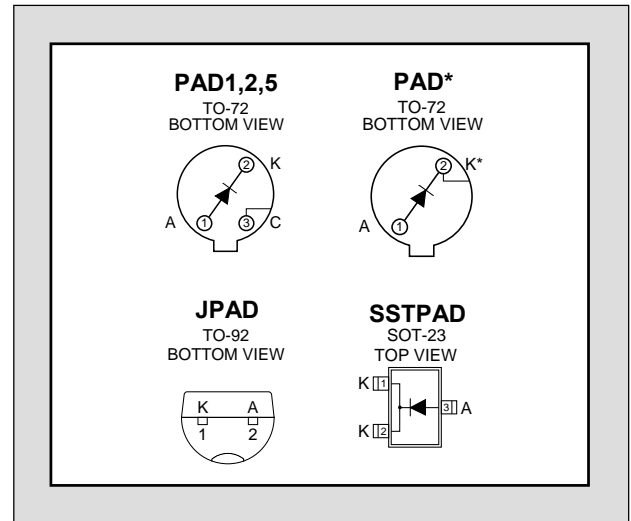


PAD SERIES

PICO AMPERE DIODES

| FEATURES | |
|---|----------------------|
| DIRECT REPLACEMENT FOR SILICONIX PAD SERIES | |
| REVERSE BREAKDOWN VOLTAGE | $BV_R \geq -30V$ |
| REVERSE CAPACITANCE | $C_{RSS} \leq 2.0pF$ |
| ABSOLUTE MAXIMUM RATINGS¹ | |
| @ 25 °C (unless otherwise stated) | |
| Maximum Temperatures | |
| Storage Temperature | -65 to +150 °C |
| Operating Junction Temperature | -55 to +135 °C |
| Maximum Power Dissipation | |
| Continuous Power Dissipation (PAD) | 300mW |
| Continuous Power Dissipation (J/SSTPAD) | 350mW |
| Maximum Currents | |
| Forward Current (PAD) | 50mA |
| Forward Current (J/SSTPAD) | 10mA |



* Cathode tied to Case

COMMON ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

| SYMBOL | CHARACTERISTIC | MIN | TYP | MAX | UNITS | CONDITIONS | |
|-----------|---------------------------|------------|-----|-----|-------|-----------------|-----------------------|
| BV_R | Reverse Breakdown Voltage | ALL PAD | -45 | | V | $I_R = -1\mu A$ | |
| | | ALL SSTPAD | -30 | | | | |
| | | ALL JPAD | -35 | | | | |
| V_F | Forward Voltage | | 0.8 | 1.5 | | $I_F = 5mA$ | |
| C_{RSS} | Total Reverse Capacitance | PAD1,5 | | 0.5 | 0.8 | pF | $V_R = -5V, f = 1MHz$ |
| | | All Others | | 1.5 | 2 | | |

SPECIFIC ELECTRICAL CHARACTERISTICS @ 25 °C (unless otherwise stated)

| SYMBOL | CHARACTERISTIC | PAD ² | JPAD ² | SSTPAD ² | UNITS | CONDITIONS | |
|---------------|--|------------------|-------------------|---------------------|-------|------------|--------------|
| I_R | Maximum Reverse Leakage Current ² | (SST/J)PAD1 | -1 | | | pA | $V_R = -20V$ |
| | | (SST/J)PAD2 | -2 | | | | |
| | | (SST/J)PAD5 | -5 | -5 | -5 | | |
| | | (SST/J)PAD10 | -10 | -10 | -10 | | |
| | | (SST/J)PAD20 | -20 | -20 | -20 | | |
| | | (SST/J)PAD50 | -50 | -50 | -50 | | |
| | | (SST/J)PAD100 | -100 | -100 | | | |
| | | (SST/J)PAD200 | | -200 | | | |
| (SST/J)PAD500 | | -500 | | | | | |

Figure 1. Operational Amplifier Protection

Input Differential Voltage limited to 0.8V (typ) by JPADs D₁ and D₂. Common Mode Input voltage limited by JPADs D₃ and D₄ to ±15V.

Figure 2. Sample and Hold Circuit

Typical Sample and Hold circuit with clipping. JPAD diodes reduce offset voltages fed capacitively from the JFET switch gate.

FIGURE 1

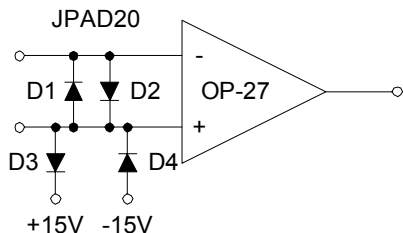
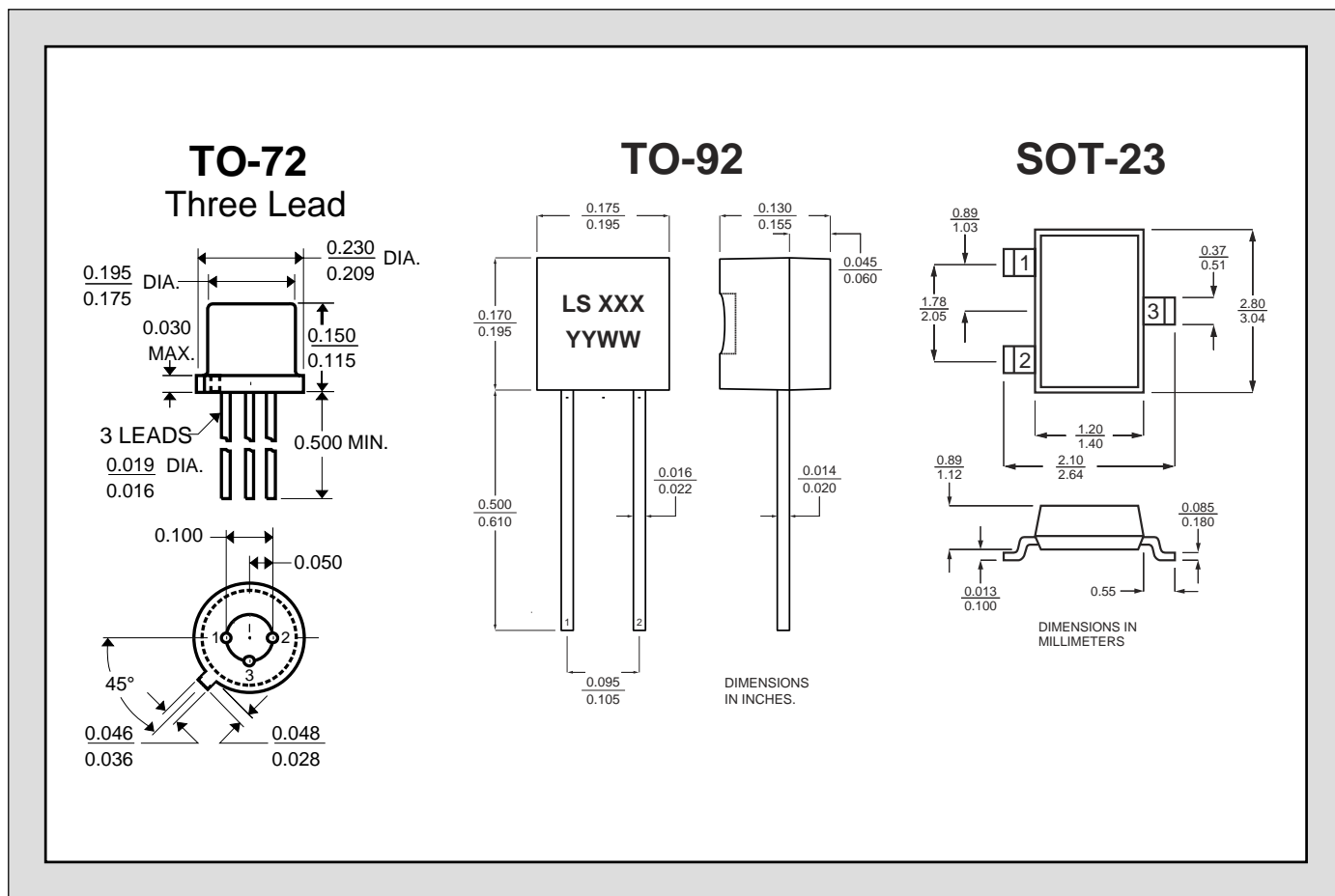
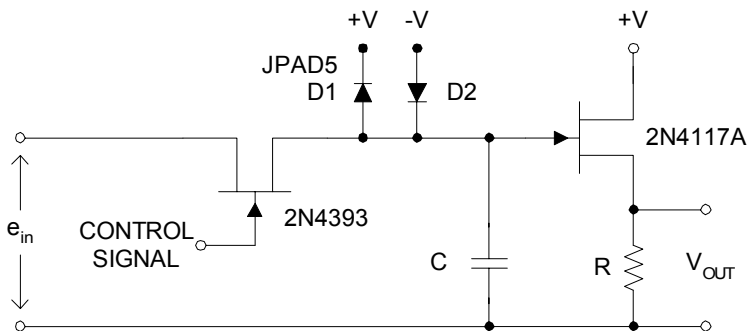


FIGURE 2



1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. The PAD type number denotes its maximum reverse current value in pico amperes. Devices with I_R values intermediate to those shown are available upon request.

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