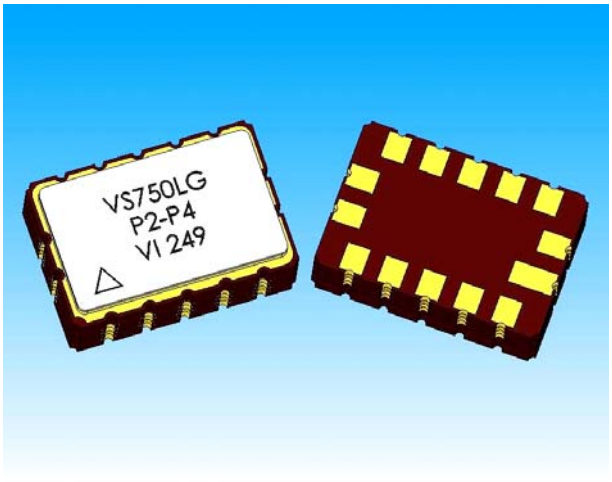
VS-750
Dual Frequency VCSO



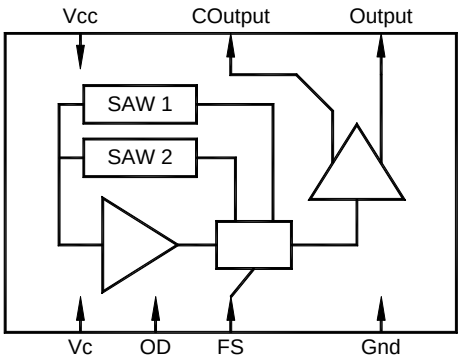
Features

- 5 x 7.5 x 2.5 mm Package
- Output Frequencies from 500 MHz to 850 MHz
- 3.3 V Operation
- Low Jitter < 0.25 ps-rms across 50 kHz to 80 MHz
- LV-PECL Configuration with Fast Transition Times
- Complementary Outputs
- Frequency Select
- Output Disable
- Patent Pending Technology
- Pb Product is free of lead and compliant to EC RoHS Directive

Applications

PLL circuits for Clock Smoothing and Frequency Translation

Description	Standard
1-2-4 Gigabit Fibre Channel	INCITS 352-2002
10 Gigabit Fibre Channel	INCITS 364-2003
10GbE LAN / WAN	IEEE 802.3ae
OC-192	ITU-T G.709
SONET / SDH	GR-253-CORE Issue3



Description

The VS-750 is a SAW based voltage controlled oscillator that operates at the fundamental frequencies of the internal SAW filters. These SAW filters are high-Q quartz devices that enable the circuit to achieve low phase jitter performance over a wide operating temperature range. The dual oscillator is housed in a hermetically sealed leadless surface mount package offered on tape and reel. It has a frequency select function that enables either “Frequency 1” or “Frequency 2.” It also has an output disable to facilitate on-board testing.

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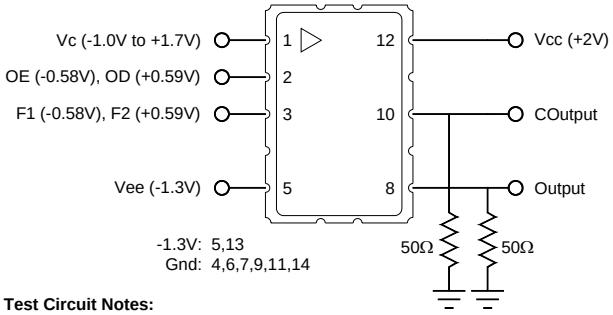
Electrical Performance

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Frequency						
Nominal Frequency	f_N		500 - 850		MHz	1,2,3
Absolute Pull Range	APR	±50			ppm	1,2,3,8
Linearity	Lin		±5		%	2,4,8
Gain Transfer (See Pg 5)	K_V		+405		ppm/V	2,8
Temperature Stability	f_{STAB}		±100		ppm	1,6
Transition Time			4		µsec	6
Supply						
Voltage	V_{CC}	2.97	3.3	3.63	V	2,3
Current (No Load)	I_{CC}		55	70	mA	3
Outputs						
Mid Level		V_{CC}-1.4	V_{CC}-1.3	V_{CC}-1.2	V	2,3
Swing		550	650	950	mV-pp	2,3
Current	I_{OUT}			20	mA	6
Rise Time	t_R		250	400	ps	5,6
Fall Time	t_F		250	400	ps	5,6
Symmetry	SYM	45	50	55	%	2,3
Spurious Suppression		50	60		dBc	6
Jitter (See Pg 5)	ϕJ		0.130	0.250	ps-rms	6,7
Control Voltage						
Input Impedance	Z_c		100		kΩ	6
Modulation Bandwidth	BW		500		kHz	6
Operating Temperature	T_{OP}	-40		85	°C	1,3
Package Size			5.0 x 7.5 x 2.5		mm	

1. See Standard Frequencies and Ordering Information (Pg 7).
2. Parameters are tested with production test circuit below (Fig 1).
3. Parameters are tested at ambient temperature with test limits guardbanded for specified operating temperature.
4. Measured as the maximum deviation from the best straight-line fit, per MIL-0-55310.
5. Measured from 20% to 80% of a full output swing (Fig 2).
6. Not tested in production, guaranteed by design, verified at qualification.
7. Integrated across 50 kHz to 80 MHz, per GR-253-CORE Issue3.
8. Tested with Vc = 0.3V to 3.0V.



Test Circuit Notes:
1) To Permit 50Ω Measurement of Outputs, all DC Inputs are Biased Down 1.3V.
2) All Voltage Sources Contain Bypass Capacitors to Minimize Supply Noise.
3) 50Ω Terminations are Within Test Equipment.

Figure 1. Test Circuit

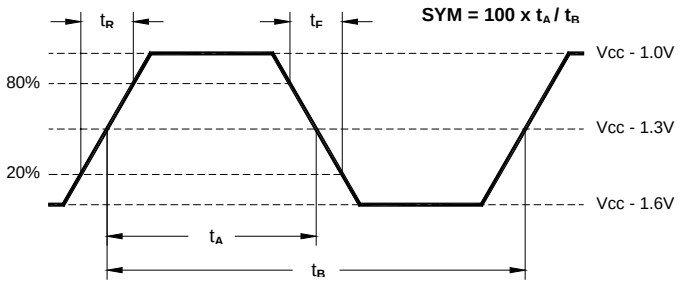


Figure 2. 10K LV-PECL Waveform

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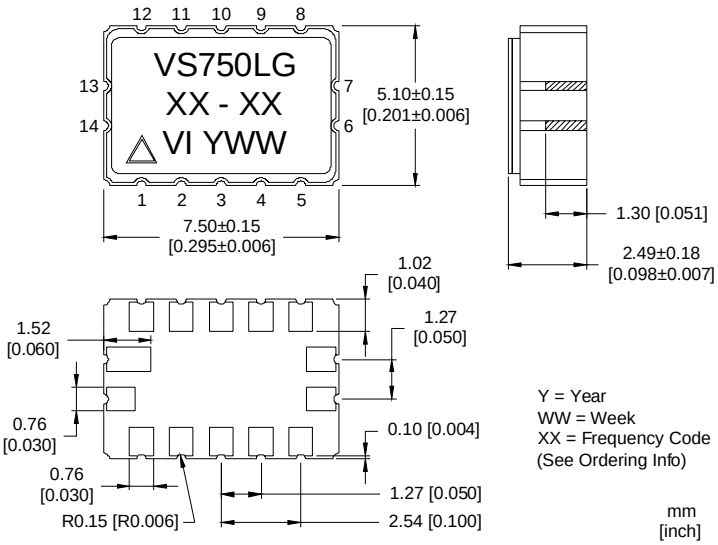
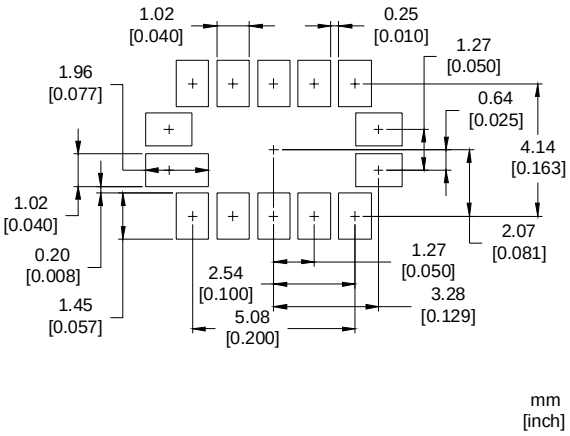
Outline Diagram



Pad Layout



Pin Out

Pin	Symbol	Function
1	V_C	VCSO Control Voltage
2	OD	Output Disable (See Control Logic)
3	FS	Frequency Select (F1 or F2)
4,6,7,9,11,14	NC	No Connection (Suggest to Gnd)
5,13	Gnd	Case and Electrical Ground
8	Output	VCSO Output
10	COutput	VCSO Complementary Output
12	V_{CC}	Power Supply Voltage (3.3 V ±10%)

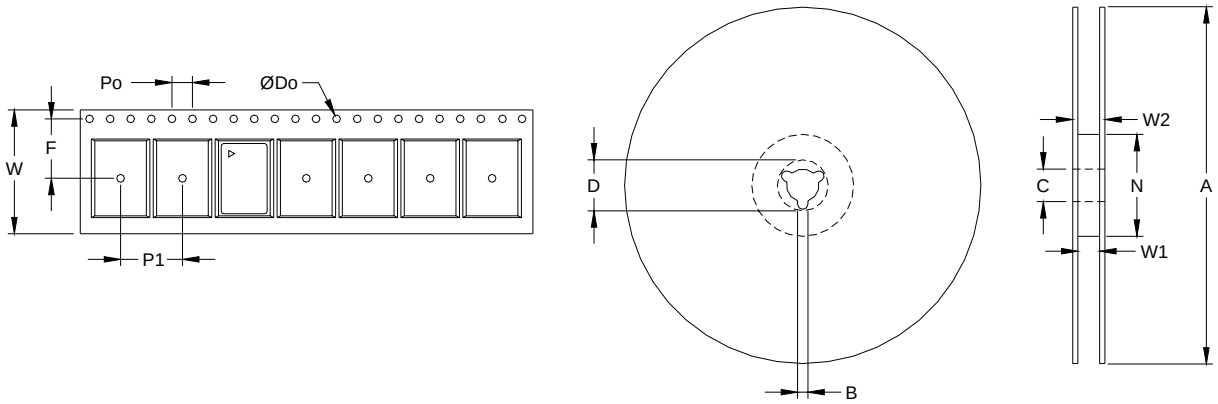
Marking Key

Position 6	Position 7
L = LFF	G = GNN
	H = HNN

Control Logic (LV-CMOS)

OD	FS	Operation
0	0	F1
0	1	F2
1	0	Disabled

Tape and Reel (EIA-481-2-A)



Tape Dimensions (mm) / Reel Dimensions (mm)

Dimension	W	F	Do	Po	P1	A	B	C	D	N	W1	W2	# Per
Tolerance	Typ	Typ	Typ	Typ	Typ	Typ	Min	Typ	Min	Min	Typ	Max	Reel
VS-750	16	7.5	1.5	4	8	178	1.5	13	20.2	50	16.4	22.4	200

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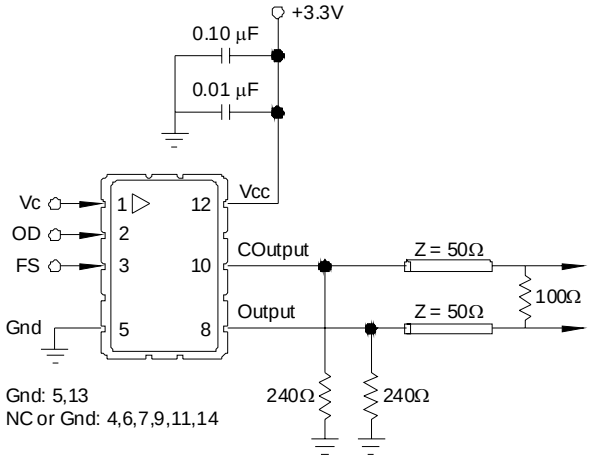
Absolute Maximum Ratings

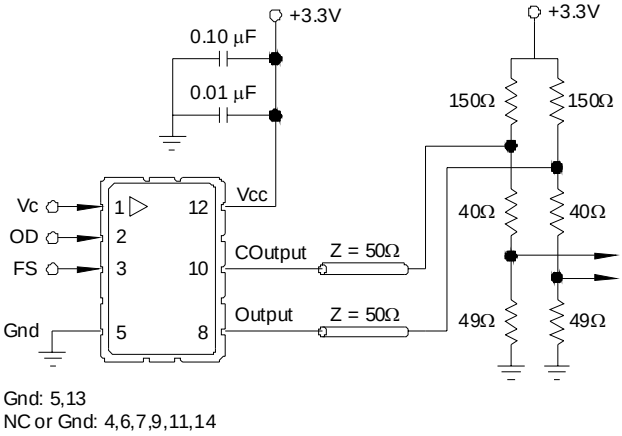
Parameter	Symbol	Ratings	Unit
Power Supply	V_{CC}	0 to 6	V
Input Current	I_{IN}	100	mA
Output Current	I_{OUT}	25	mA
Voltage Control Range	V_C	0 to V_{CC}	V
Storage Temperature	T_{STR}	-55 to 125	°C
Soldering Temperature / Duration	T_{PEAK} / t_P	260 / 40	°C / sec

Stresses in excess of these absolute maximum ratings can permanently damage the device. Also, exposure to these absolute maximum ratings for extended periods can adversely affect device reliability. Functional operation is not implied at these or any other conditions in excess of those represented in the operational sections of this datasheet. Permanent damage is also possible if any device input (Vc, FS, or OD) draws greater than 100 mA.

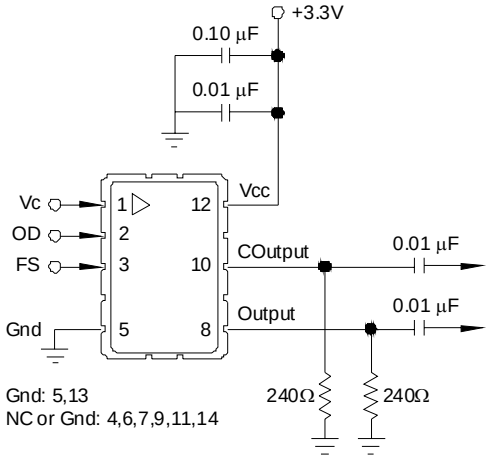
Suggested Output Load Configurations



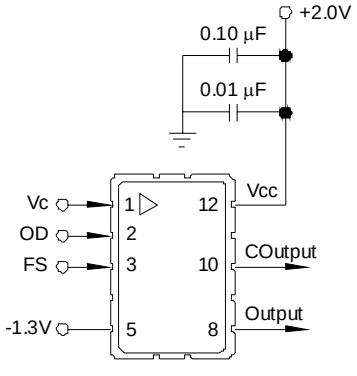
LV-PECL to LV-PECL: For short transmission lengths, the power consumption could be reduced by removing the 100Ω resistor and doubling the value of the pull down resistors.



LV-PECL to LVDS: Restricted for short transmission lengths. Configuration may require modification depending on LVDS receiver.



Functional Test: Allows standard power supply configuration. Since AC coupled, the LV-PECL levels cannot be measured.



Production Test: Allows direct DC coupling into 50Ω measurement equipment. Must bias the power supplys as shown. Similar to Figure 1.

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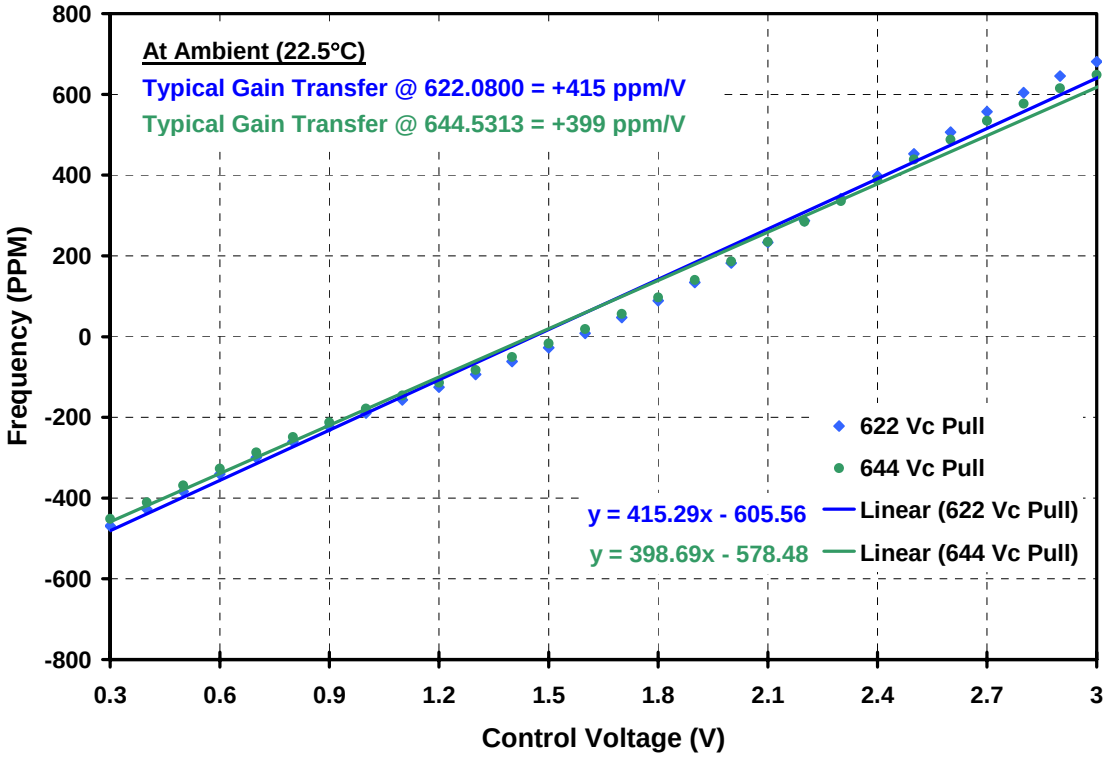
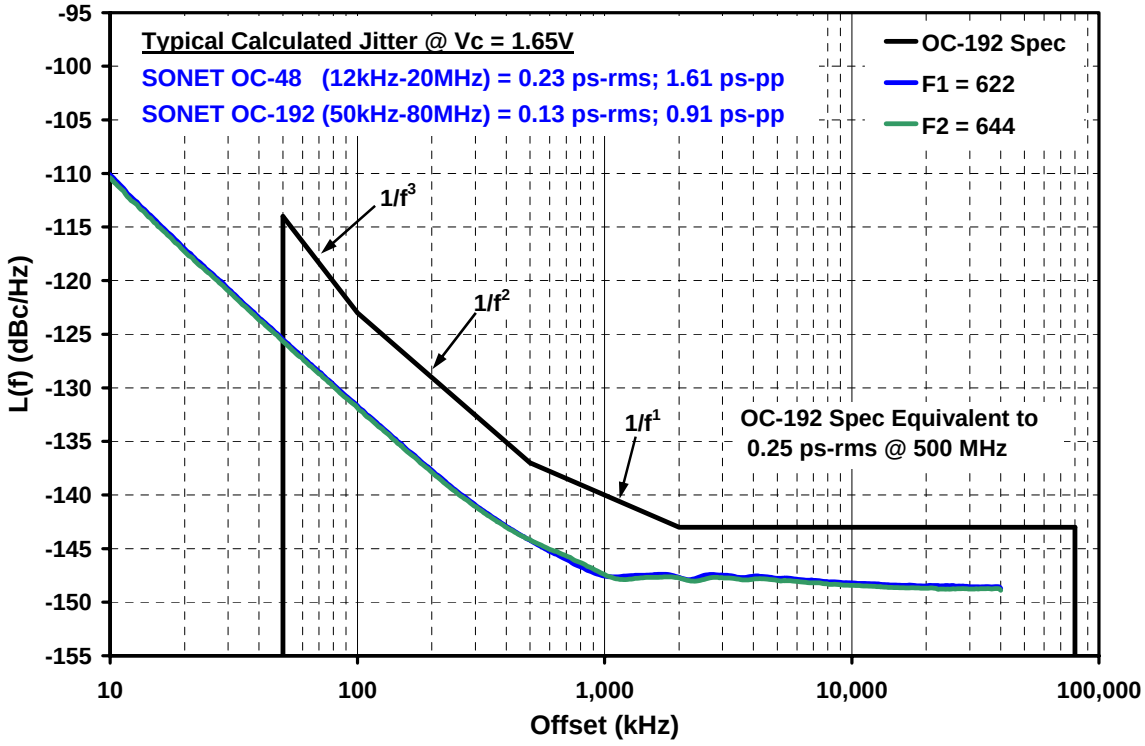
Typical Characteristics





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Reliability

VI qualification includes aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The VS-750 family is capable of meeting the following qualification tests:

Environmental Compliance

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2016

Handling Precautions

Although ESD protection circuitry has been designed into the VS-750 proper precautions should be taken when handling and mounting. VI employs a human body model (HBM) and a man man model (MM) for ESD susceptibility testing and design protection evaluation.

ESD Ratings

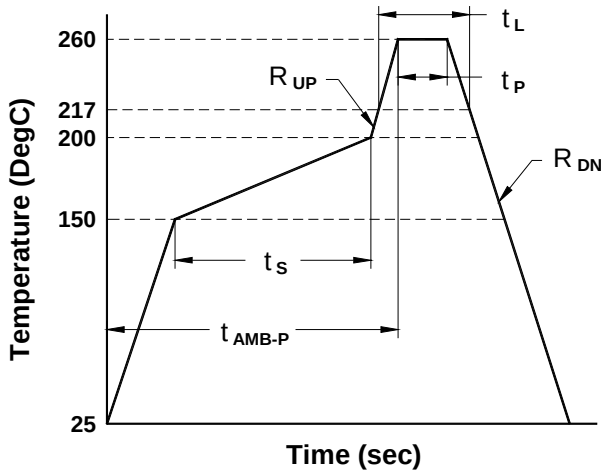
Model	Minimum	Conditions
Human Body Model	1500 V	MIL-STD 883, Method 3015
Man Man Model	200 V	V/JESD22-A115-A

Reflow Profile (IPC/JEDEC J-STD-020C)

Parameter	Symbol	Value
PreHeat Time	t_S	60 sec Min, 180 sec Max
Ramp Up	R_{UP}	3 °C/sec Max
Time Above 217 °C	t_L	60 sec Min, 150 sec Max
Time To Peak Temperature	t_{AMB-P}	480 sec Max
Time At 260 °C	t_P	20 sec Min, 40 sec Max
Ramp Down	R_{DN}	6 °C/sec Max

The device has been qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The temperatures refer to the topside of the package, measured on the package body surface. The VS-750 device is hermetically sealed so an aqueous wash is not an issue.

Terminal Plating: Electroless Gold Plate over Nickel Plate



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Standard Frequencies (MHz)

531.2500 **P8**	569.1964 **P9**	622.0800 **P2**	624.6938 **PD**	625.0000 **P3**	627.3296 **P7**
629.9878 **PA**	644.5313 **P4**	647.2508 **PK**	657.4219 **PB**	666.5143 **P5**	669.3266 **R3**
669.6429 **R1**	672.1627 **R5**	690.5692 **R4**	693.4830 **R6**	693.7500 **R8**	704.3806 **TG**
707.3527 **TC**	777.6000 **T4**	805.6641 **TA**			

1. **Other frequencies available upon request, please contact VI for details.**
2. **Frequency 1 must be lower than Frequency 2. Not all combinations are available.**

Ordering Information

VS - 750 - L F F - H N N - P2 - P4

Product Family
VS: VCSO

Package
750: 5 x 7.5 x 2.5 mm

Input
L: 3.3 V

Output
F: LV-PECL

Operating Temperature
F: -40 to 85 °C

Absolute Pull Range
G: +/- 50 ppm
H: +/- 100 ppm

Other (Future Use)
N: N/A

Other (Future Use)
N: N/A

Frequency 1
See Above

Frequency 2
See Above

For Additional Information, Please Contact:

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