Genesys Logic, Inc.

GL424

SD/MMC Flash Card Controller

Datasheet
Revision 1.00
Apr. 18, 2007

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Revision History

Revision	Date	Description
0.90	04/06/2006	First formal release
1.00	04/18/2007	Add Die Pad, 46 PIN LGA, 51PIN LGA 1. Pin Assignment, p.11 2. Package Dimension, p.30

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CHAPTER 1 GENERAL DESCRIPTION

GL424 is a single-chip controller for SD and MMC memory cards. It is designed based on SD1.0/SD1.1/SD2.0 and MMC3.3/MMC4.0 specification. Its unique RAM based firmware strategy provides flexibility for fast compatibility and performance improvement, therefore, give customers strong support to win in today's fast-changing market. With its simple interface, customers can easily apply it to SD and MMC memory cards manufacturing at the same time.

GL424 manages interface protocol, data storage and retrieval, error detection and correction, defect handling and diagnostic, as well as power management. With a built-in flash management algorithm, GL424 is applicable for most types of flash in the market: SAMSUNG, MICRON, ST, TOSHIBA, HYNIX and RENESAS.

GL424 is packaged LQFN-46 and VFBGA-54. Both die and LQFN/VFBGA package are available and completely meet SD and MMC memory card mechanical thickness requirement. The pin assignment that fits to card sockets provides easy PCB layout.

GL424 is unique in its three advanced features:

(1) Dual-channel solution as well as normal single channel solution with top access speed;

(2) Dual voltage for both 1.8V and 3.3V interface;

(3) 8KV-ESD protecting the whole card.

VFBGA54 packaged GL424 has a dual channel flash access interface, which remarkably speed up read/write performance. It supports 16-bit flash also.

GL424 provides 8KV ESD (human body mode) and 15KV ESD (mechanical mode) protection. Especially, GL424 can also provide such high voltage ESD protection to FLASH on the whole SD/MMC card. Therefore, greatly improved SD/MMC card's reliability and high quality in unpredictable application environment.

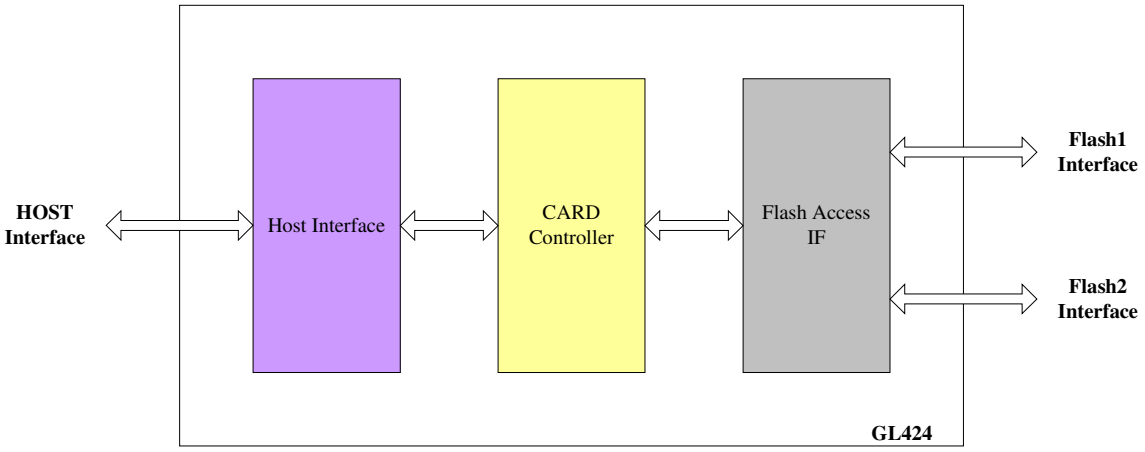


Figure 1. 1 - GL424 Block Diagram

1.1 CARD Interface

The card controller, complied with SD/MMC specification, explains commands from SD/MMC host and transfers data between SD/MMC host and flash.

1.2 Flash Access Interface

The flash access interface communicates with CPU. It also manages two channels of flash, based on flash commands. Moreover, it implements defect processing, ECC, and address mapping, etc.

1.3 Embedded CPU

Embedded CPU performs arithmetic and logical operations. In addition, it extracts instruction from ROM and SRAM, decodes and executes them. It also manages control and status signals between flash access interface and itself.

CHAPTER 2 FEATURES

2.1 SD Host Interface

- Complies with SD Specification, Version 2.0
- Complies with SD Specification, Version 1.1
- Complies with SD Specification, Version 1.0
- Supports SPI mode and CPRM functions
- Supports clock rate up to 25 MHz for SD1.0
- Supports clock rate up to 52 MHz for SD1.1 and SD2.0
- Buffers for multi-block flash memory programming
- DMA operation between buffers and flash memory
- Supports automatic CRC16 generation and verification on DATA3-0
- Supports SD card exceed 4Gbytes capacity

2.2 MMC Host Interface

- Complies with MultiMediaCard System Specification, Version 4.0
- Complies with MultiMediaCard System Specification, Version 3.3
- Supports SPI mode and CPRM functions
- Supports clock rate up to 20 MHz for MMC3.3
- Supports clock rate up to 52 MHz for MMC4.0
- Buffers for multi-block flash memory programming
- DMA operation between buffers and flash memory
- Supports automatic CRC16 generation and verification on DATA7-0

2.3 Flash Memory Interface

- Direct interface to NAND/AND flash chips (SAMSUNG / TOSHIBA / HITACHI / RENESAS / MICRON / ST / HYNIX)
- Supports dual-channel, 16 bits flash (VFBGA54 package and die)
- Drives up to 4 flash memory chips, respectively (VFBGA54 package and die)
- Supports 64M / 128M / 256M / 512M / 1G / 2G / 4G / 8G bits flash chips
- Embedded firmware support for flash file system (FTL)
- Built-in flash management algorithm
- Powerful ECC for error detection and correction up to 6 bytes per 512bytes

2.4 Micro Controller and Analog System

- RISC core with fast speed and less code size
- Flexibility to update system code
- Ability to add customers' own feature

2.5 8KV-ESD protection

- 8KV human body ESD protection (contact discharge mode) for the whole card (not only controller chip itself)
- 15KV mechanical mode ESD protection (air discharge mode) for the whole card (not only controller chip itself)

2.6 Dual Channel FLASH to reach top Read/Write Speed

- GL424 provides dual channel flash access solution. This can reach the read/write speed almost doubled compared with single channel solution.

2.7 Dual voltage application

- GL424 provides the solution for dual voltage application. This means MMC4.0 card with GL424 can work with either 1.8V or 3.3V host interface.

2.8 Product Packages

- 46-pin LQFN package
- 54-pin VFBGA package
- 46-pin LGA package
- 51-pin LGA package

2.9 Technology

- 0.18um process

2.10 Manufacture

- Easy firmware development environment
- Supports firmware upgrade tool via PC

CHAPTER 3 PIN ASSIGNMENT

3.1 Pinout

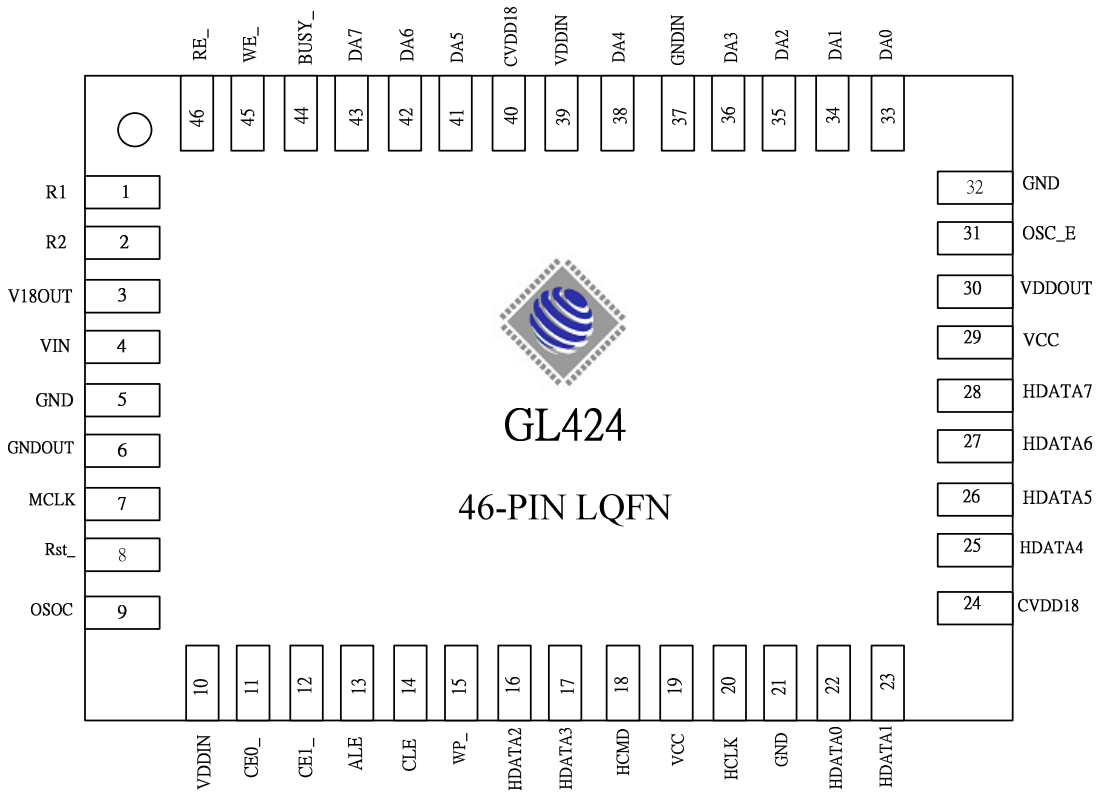


Figure 3.1 - 46 Pin LQFN Pinout

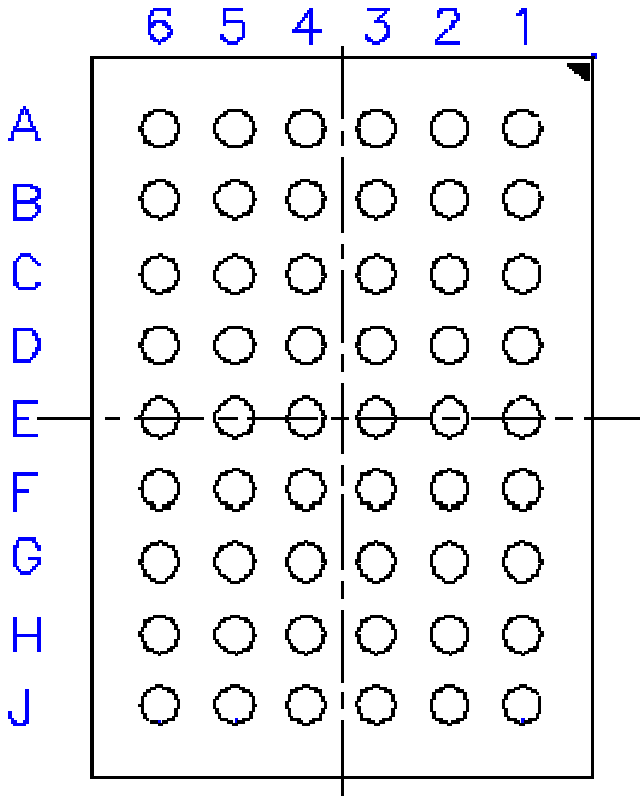


Figure 3.2 - 54 Pin VFBGA Pinout

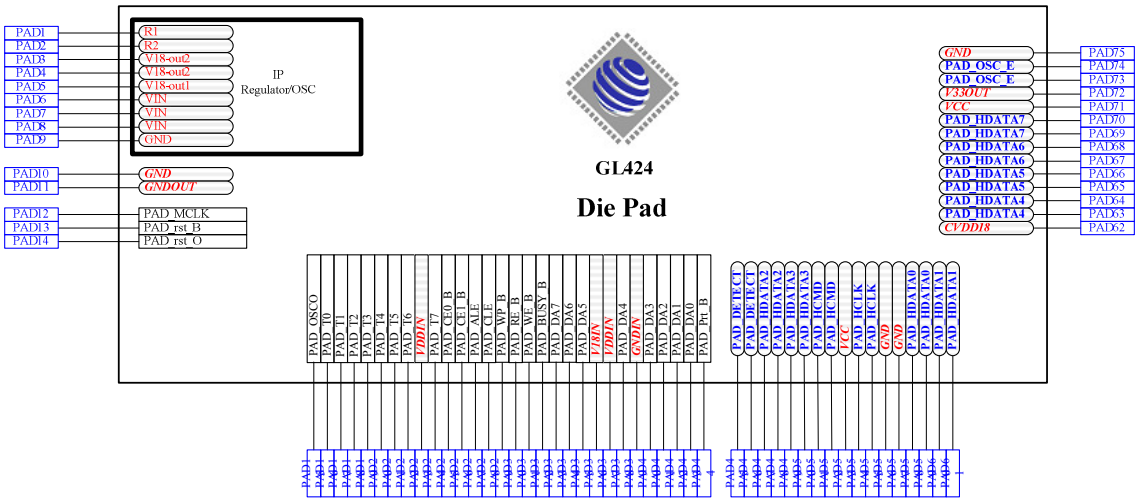


Figure 3.3 – Die Pad Pinout

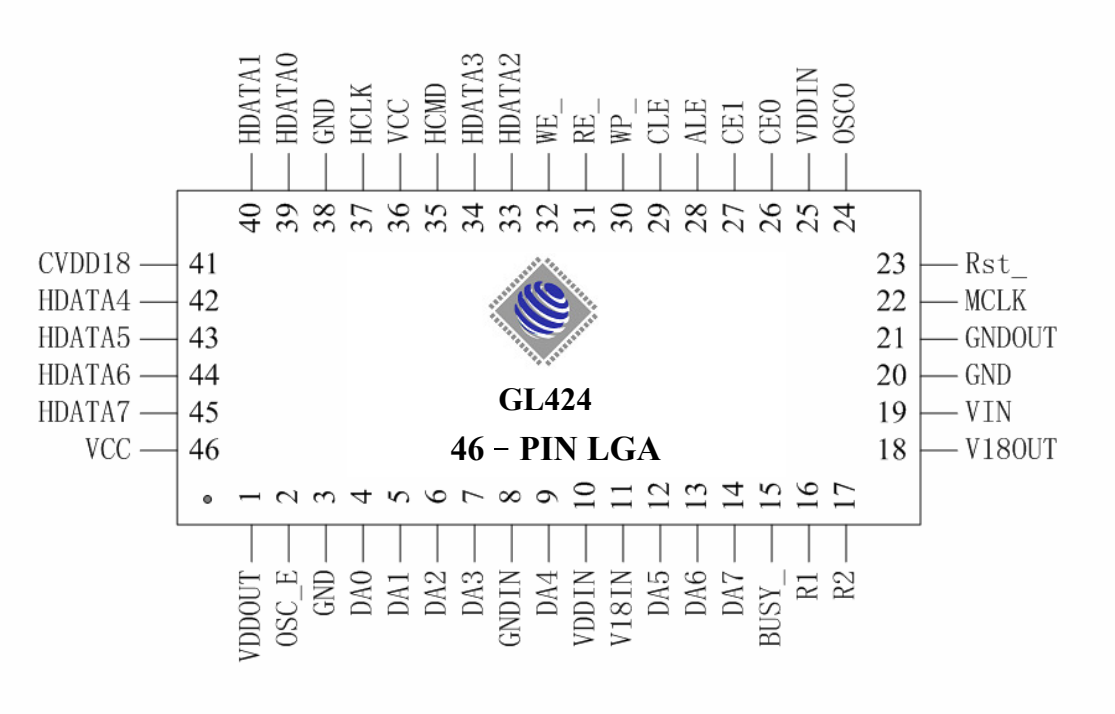


Figure 3.4 – 46 Pin LGA Pinout

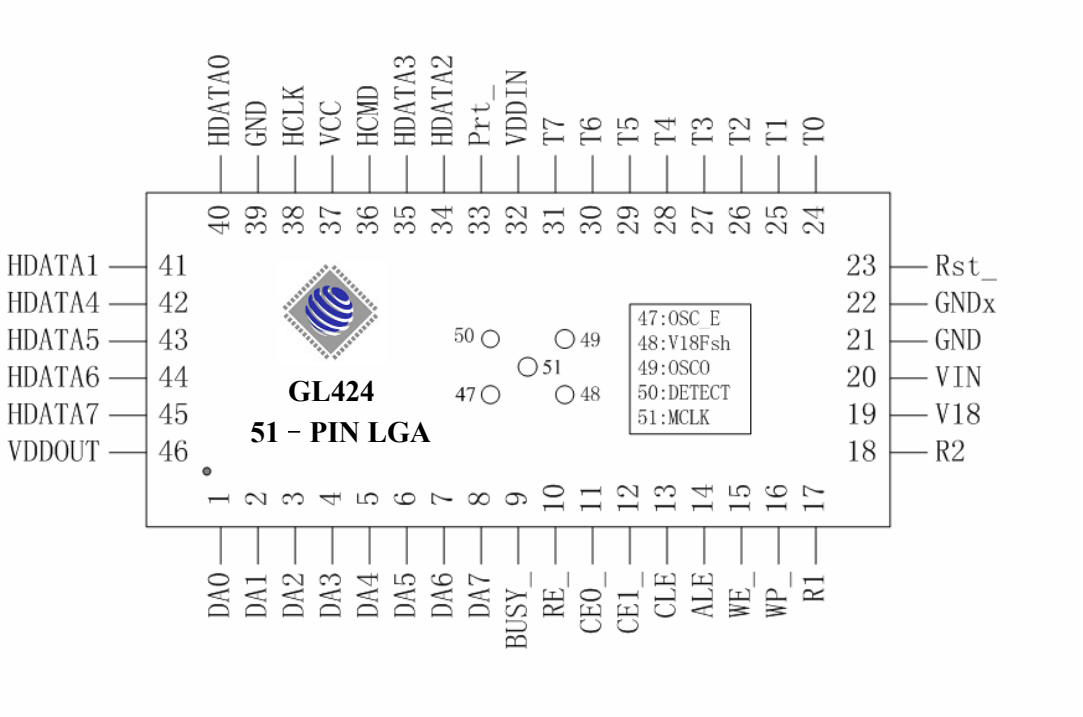


Figure 3.5 – 51 Pin LGA Pinout

3.2 Pin Descriptions

3.2.1 Regulator Interface

Table 3.1 - 46 PIN LQFN Regulator Interface

Pin No.	Pin Name	Type	Description
1	R1	A	External Resistor pad
2	R2	A	External Resistor pad
3	V18OUT	O	1.8V output (Max.100mA)
4	VIN	P	3.3V power
5	GND	P	Ground
6	GNDOUT	P	Ground output

Table 3.2 - 54 PIN VFBGA Regulator Interface

Pin No.	Pin Name	Type	Description
A6	R1	A	External Resistor pad
A5	R2	A	External Resistor pad
B5	V18OUT	O	1.8V output (Max.100mA)
C4	V18Fsh	O	1.8V output (Max.30mA)
A4	VIN	P	3.3V power
B4	GND	P	Ground
G5	GNDX	P	Ground

Table 3.3 – Die Pad Regulator Interface

Pad No.	Pad Name	Type	Description
PAD1	R1	A	External Resistor pad
PAD2	R2	A	External Resistor pad
PAD3	V18-out2	O	1.8V output (Max.100mA) (Double Bonding)
PAD4	V18-out2	O	Regulator 1.8V output (Double Bonding)
PAD5	V18-out1	O	1.8V output (Max.40mA)

PAD6	VIN	P	3.3V power (Tri-bonding)
PAD7	VIN	P	3.3V power (Tri-bonding)
PAD8	VIN	P	3.3V power (Tri-bonding)
PAD9	GND	P	Ground (Double Bonding)
PAD10	GND	P	Ground (Double Bonding)
PAD11	GNDOUT	P	Ground output when enhanced 8KV-ESD protected

Table 3.4 – 46 PIN LGA Regulator Interface

Pin No.	Pin Name	Type	Description
16	R1	A	External Resistor pad
17	R2	A	External Resistor pad
18	V18OUT	O	1.8V output (Max.100mA)
19	VIN	P	3.3V power
20	GND	P	Ground
21	GNDOUT	P	Ground

Table 3.5 – 51 PIN LGA Regulator Interface

Pin No.	Pin Name	Type	Description
17	R1	A	External Resistor pad
18	R2	A	External Resistor pad
19	V18	O	1.8V output (Max.100mA)
48	V18Fsh	O	1.8V output (Max.30mA)
20	VIN	P	3.3V power
21	GND	P	Ground
22	GNDX	P	Ground

Note : **A: Analog**

I: Input

O: Output

P: Power supply

B: Bi-direction

3.2.2 Card Interface

Table 3.3 - 46 PIN LQFN Card Interface

Pin No.	Pin Name	Type	Description
20	HCLK	I	HCLK from HOST
18	HCMD	B	SD/MMC mode: HCMD from/to HOST SPI mode: Data-in signal from HOST
22	HDATA0	B	SD/MMC mode: HDATA0 from/to HOST. SPI mode: Data-out signal to HOST
23	HDATA1	B	SD/MMC mode: HDATA1 from/to HOST. SPI mode: not connected
16	HDATA2	B	SD/MMC mode: HDATA2 from/to HOST. SPI mode: not connected
17	HDATA3	B	SD/MMC mode: HDATA3 from/to HOST. SPI mode: CS signal
25	HDATA4	B	MMC mode: HDATA4 from/to HOST.
26	HDATA5	B	MMC mode: HDATA5 from/to HOST.
27	HDATA6	B	MMC mode: HDATA6 from/to HOST.
28	HDATA7	B	MMC mode: HDATA7 from/to HOST.

Table 3.4 - 54 PIN VFBGA Card Interface

Pin No.	Pin Name	Type	Description
H1	HCLK	I	HCLK from HOST
F2	HCMD	B	SD/MMC mode: HCMD from/to HOST SPI mode: Data-in signal from HOST
J2	HDATA0	B	SD/MMC mode: HDATA0 from/to HOST. SPI mode: Data-out signal to HOST

J1	HDATA1	B	SD/MMC mode: HDATA1 from/to HOST. SPI mode: not connected
E1	HDATA2	B	SD/MMC mode: HDATA2 from/to HOST. SPI mode: not connected
F1	HDATA3	B	SD/MMC mode: HDATA3 from/to HOST. SPI mode: CS signal
J3	HDATA4	B	MMC mode: HDATA4 from/to HOST.
H2	HDATA5	B	MMC mode: HDATA5 from/to HOST.
H4	HDATA6	B	MMC mode: HDATA6 from/to HOST.
H3	HDATA7	B	MMC mode: HDATA7 from/to HOST.

Table 3.5 – Die Pad Card Interface

Pad No.	Pad Name	Type	Description
PAD54	PAD_HCLK	B	HCLK from HOST
PAD55	PAD_HCLK	B	Backup PAD (No Bonding)
PAD51	PAD_HCMD	B	SD/MMC mode: HCMD from/to HOST SPI mode: Data-in signal from HOST
PAD52	PAD_HCMD	B	Backup PAD (No Bonding)
PAD59	PAD_HDATA0	B	SD/MMC mode: HDATA0 from/to HOST. SPI mode: Data-out signal to HOST
PAD58	PAD_HDATA0	B	Backup PAD (No Bonding)
PAD61	PAD_HDATA1	B	SD/MMC mode: HDATA1 from/to HOST. SPI mode: not connected
PAD60	PAD_HDATA1	B	Backup PAD (No Bonding)
PAD47	PAD_HDATA2	B	SD/MMC mode: HDATA2 from/to HOST. SPI mode: not connected
PAD48	PAD_HDATA2	B	Backup PAD (No Bonding)

Table 3.6 - 46 PIN LGA Card Interface

Pin No.	Pin Name	Type	Description
37	HCLK	I	HCLK from HOST
35	HCMD	B	SD/MMC mode: HCMD from/to HOST SPI mode: Data-in signal from HOST
39	HDATA0	B	SD/MMC mode: HDATA0 from/to HOST. SPI mode: Data-out signal to HOST
40	HDATA1	B	SD/MMC mode: HDATA1 from/to HOST. SPI mode: not connected
33	HDATA2	B	SD/MMC mode: HDATA2 from/to HOST. SPI mode: not connected
34	HDATA3	B	SD/MMC mode: HDATA3 from/to HOST. SPI mode: CS signal
42	HDATA4	B	MMC mode: HDATA4 from/to HOST.
43	HDATA5	B	MMC mode: HDATA5 from/to HOST.
44	HDATA6	B	MMC mode: HDATA6 from/to HOST.
45	HDATA7	B	MMC mode: HDATA7 from/to HOST.

Table 3.7 - 51 PIN LGA Card Interface

Pin No.	Pin Name	Type	Description
38	HCLK	I	HCLK from HOST
36	HCMD	B	SD/MMC mode: HCMD from/to HOST SPI mode: Data-in signal from HOST
40	HDATA0	B	SD/MMC mode: HDATA0 from/to HOST. SPI mode: Data-out signal to HOST
41	HDATA1	B	SD/MMC mode: HDATA1 from/to HOST. SPI mode: not connected
34	HDATA2	B	SD/MMC mode: HDATA2 from/to HOST. SPI mode: not connected
35	HDATA3	B	SD/MMC mode: HDATA3 from/to HOST. SPI mode: CS signal
42	HDATA4	B	MMC mode: HDATA4 from/to HOST.
43	HDATA5	B	MMC mode: HDATA5 from/to HOST.

44	HDATA6	B	MMC mode: HDATA6 from/to HOST.
45	HDATA7	B	MMC mode: HDATA7 from/to HOST.

3.2.3 Flash Interface

Table 3.8 - 46 PIN LQFN Flash Interface

Pin No.	Pin Name	Type	Description
11	CE0_	B	'0' for FLASH chip 0 to select active (low-active).
12	CE1_	B	'0' for FLASH chip 1 to select active (low-active).
14	CLE	B	FLASH command latch enable
13	ALE	B	FLASH address latch enable
46	RE_	B	FLASH read enable (low active)
45	WE_	B	FLASH write enable (low active)
44	BUSY_	B	FLASH ready when high, busy when low.
15	WP_	B	FLASH write protect (low active)
33	DA0	B	FLASH bus bit0
34	DA1	B	FLASH bus bit1
35	DA2	B	FLASH bus bit2
36	DA3	B	FLASH bus bit3
38	DA4	B	FLASH bus bit4
41	DA5	B	FLASH bus bit5
42	DA6	B	FLASH bus bit6
43	DA7	B	FLASH bus bit7

Table 3.9 - 54 PIN VFBGA Flash Interface

Pin No.	Pin Name	Type	Description
B6	CE0_	B	'0' for FLASH chip 0 to select active (low-active).
C5	CE1_	B	'0' for FLASH chip 1 to select active (low-active).
C6	ALE	B	FLASH address latch enable
D5	CLE	B	FLASH command latch enable
D6	RE_	B	FLASH read enable (low active)
E6	WE_	B	FLASH write enable (low active)

E5	BUSY_	B	FLASH ready when high, busy when low.
D4	WP_	B	FLASH write protect (low active)
J5	DA0	B	FLASH bus bit0
J6	DA1	B	FLASH bus bit1
H5	DA2	B	FLASH bus bit2
H6	DA3	B	FLASH bus bit3
G6	DA4	B	FLASH bus bit4
F5	DA5	B	FLASH bus bit5
F6	DA6	B	FLASH bus bit6
E4	DA7	B	FLASH bus bit7

Table 3.10 – Die Pad Flash Interface

Pad No.	Pad Name	Type	Description
PAD25	PAD_CE0_B	B	'0' for FLASH chip 0 to select active (low-active).
PAD26	PAD_CE1_B	B	'0' for FLASH chip 1 to select active (low-active).
PAD28	PAD_CLE	B	FLASH command latch enable
PAD27	PAD_ALE	B	FLASH address latch enable
PAD30	PAD_RE_B	B	FLASH read enable (low active)
PAD31	PAD_WE_B	B	FLASH write enable (low active)
PAD32	PAD_BUSY_B	B	FLASH ready when high, busy when low.
PAD29	PAD_WP_B	B	FLASH write protect (low active)
PAD43	PAD_DA0	B	FLASH bus bit0
PAD42	PAD_DA1	B	FLASH bus bit1
PAD41	PAD_DA2	B	FLASH bus bit2
PAD40	PAD_DA3	B	FLASH bus bit3
PAD38	PAD_DA4	B	FLASH bus bit4
PAD35	PAD_DA5	B	FLASH bus bit5
PAD34	PAD_DA6	B	FLASH bus bit6
PAD33	PAD_DA7	B	FLASH bus bit7

Table 3.11 – 46 PIN LGA Flash Interface

Pin No.	Pin Name	Type	Description
26	CE0_	B	'0' for FLASH chip 0 to select active (low-active).
27	CE1_	B	'0' for FLASH chip 1 to select active (low-active).
28	ALE	B	FLASH address latch enable
29	CLE	B	FLASH command latch enable
31	RE_	B	FLASH read enable (low active)
32	WE_	B	FLASH write enable (low active)
15	BUSY_	B	FLASH ready when high, busy when low.
30	WP_	B	FLASH write protect (low active)
4	DA0	B	FLASH bus bit0
5	DA1	B	FLASH bus bit1
6	DA2	B	FLASH bus bit2
7	DA3	B	FLASH bus bit3
9	DA4	B	FLASH bus bit4
12	DA5	B	FLASH bus bit5
13	DA6	B	FLASH bus bit6
14	DA7	B	FLASH bus bit7

Table 3.12 – 51 PIN LGA Flash Interface

Pin No.	Pin Name	Type	Description
11	CE0_	B	'0' for FLASH chip 0 to select active (low-active).
12	CE1_	B	'0' for FLASH chip 1 to select active (low-active).
14	ALE	B	FLASH address latch enable
13	CLE	B	FLASH command latch enable
10	RE_	B	FLASH read enable (low active)
15	WE_	B	FLASH write enable (low active)
9	BUSY_	B	FLASH ready when high, busy when low.
16	WP_	B	FLASH write protect (low active)
1	DA0	B	FLASH bus bit0
2	DA1	B	FLASH bus bit1
3	DA2	B	FLASH bus bit2

4	DA3	B	FLASH bus bit3
5	DA4	B	FLASH bus bit4
6	DA5	B	FLASH bus bit5
7	DA6	B	FLASH bus bit6
8	DA7	B	FLASH bus bit7

3.2.4 System Interface

Table 3.13 - 46 PIN LQFN System Interface

Pin No.	Pin Name	Type	Description
7	MCLK	I	Main clock input.
8	Rst_	I	Power-on reset, low active
9	OSCO	O	Main clock output
31	OSC_E	I	Oscillator enable
10	VDDIN	P	Power supply for IO
39	VDDIN	P	Power supply for IO
40	V18IN	P	Digital 1.8V power supply
37	GNDIN	P	Digital GND
19	VCC	P	3.3V power supply
29	VCC	P	3.3V power supply
21	GND	P	Ground
32	GND	P	Ground
24	CVDD18	P	1.8V power supply
30	VDDOUT	P	3.3V power output

Table 3.14 - 54 PIN VFBGA System Interface

Pin No.	Pin Name	Type	Description
B3	MCLK	I	Main clock input.
A3	Rst_	I	Power-on reset, low active
C3	OSCO	O	Main clock output
E2	OSC_E	I	Oscillator enable
D2	VDDIN	P	Power supply for flash interface IO

F4	V18IN	P	Digital 1.8V power supply
F3	VCC	P	3.3V power supply
G3	VCC	P	3.3V power supply
G4	GND	P	Ground
G2	CVDD18	P	1.8V power supply
J4	VDDOUT	P	3.3V power output
E3	Prt_	B	Protect
G1	DETECT	O	Power detect

Table 3.15 - Die Pad System Interface

Pad No.	Pad Name	Type	Description
PAD13	PAD_rst_B	I	Power-on reset input, low active
PAD14	PAD_rst_o	O	Power-on reset output
PAD44	PAD_Prt_B	B	Protect
PAD15	PAD_OSCO	O	Clock output for test
PAD12	PAD_MCLK	I	Main clock input.
PAD45	PAD_DETECT	B	Card detect
PAD46	PAD_DETECT	B	Backup PAD (No Bonding)
PAD74	PAD_OSC_E	I	Oscillator enable
PAD73	PAD_OSC_E	I	Backup PAD (No Bonding)
PAD23	VDDIN	P	Power supply for flash interface IO
PAD37	VDDIN	P	Power supply for flash interface IO
PAD36	V18IN	P	Digital 1.8V power supply
PAD39	GNDIN	P	Ground input
PAD53	VCC	P	3.3V power supply
PAD56	GND	P	Ground
PAD57	GND	P	Ground
PAD62	CVDD18	P	1.8V power supply
PAD71	VCC	P	3.3V power supply
PAD72	V33OUT	P	3.3V power output when enhanced 8KV-ESD protected
PAD75	GND	P	Ground

Table 3.16 - 46 PIN LGA System Interface

Pin No.	Pin Name	Type	Description
22	MCLK	I	Main clock input.
23	Rst_	I	Power-on reset, low active
24	OSCO	O	Main clock output
2	OSC_E	I	Oscillator enable
10	VDDIN	P	Power supply for flash interface IO
25	VDDIN	P	Power supply for flash interface IO
1	VDDOUT	P	3.3V power output
36	VCC	P	3.3V power supply
46	VCC	P	3.3V power supply
3	GND	P	Ground
38	GND	P	Ground
8	GNDIN	P	Ground
11	V18IN	P	1.8V power supply
41	CVDD18	P	1.8V power supply

Table 3.17 - 51 PIN LGA System Interface

Pin No.	Pin Name	Type	Description
51	MCLK	I	Main clock input.
23	Rst_	I	Power-on reset, low active
49	OSCO	O	Main clock output
47	OSC_E	I	Oscillator enable
32	VDDIN	P	Power supply for flash interface IO
37	VCC	P	3.3V power supply
39	GND	P	Ground
46	VDDOUT	P	3.3V power output
33	Prt_	B	Protect
50	DETECT	O	Power detect

3.2.5 Test Interface

Table 3.18 - 54 PIN VFBGA Test Interface

Pin No.	Pin Name	Type	Description
A1	T0	B	Flash2 bus bit0 to bit7 when dual channel mode; Flash bus bit8 to bit15 when 16-bit flash mode; Test mode input when testing mode. (On-chip pulled-up).
A2	T1	B	
B2	T2	B	
B1	T3	B	
C2	T4	B	
C1	T5	B	
D3	T6	B	
D1	T7	B	

Table 3.19 - Die Pad Test Interface

Pad No.	Pad Name	Type	Description
PAD16	PAD_T0	B	Flash2 bus bit0 to bit7 when dual channel mode; Flash bus bit8 to bit15 when 16-bit flash mode; Test mode input when testing mode. (On-chip pulled-up).
PAD17	PAD_T1	B	
PAD18	PAD_T2	B	
PAD19	PAD_T3	B	
PAD20	PAD_T4	B	
PAD21	PAD_T5	B	
PAD22	PAD_T6	B	
PAD24	PAD_T7	B	

CHAPTER 4 ELECTRICAL CHARACTERISTICS

4.1 Absolute Maximum Ratings

Table 4.1 - Absolute Maximum Ratings

Parameter	Symbol	Min	Max.	Unit	Remark
Supply Voltage	V_{DD}	2.0	3.6	V	CMD0, 15,55, ACMD41
Supply Voltage Differentials (V_{ss1}, V_{ss2})		-0.3	0.3	V	
Storage Temperature		-40	85	°C	
Junction Temperature			95	°C	

4.2 Bus Operating Conditions

Table 4.2 - Bus Operating Conditions

Parameter	Symbol	Min	Max.	Unit	Remark
Peak Voltage on all Lines	V_{DD}	2.6	3.6	V	
Ground Voltage		0		V	
Operation Temperature		-25	85	°C	
Operation Moisture and Corrosion			95%		Rel. humidity

4.3 D.C. Characteristics

Table 4.3 - D.C. Characteristics

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Supply voltage	V_{CC}		2.0	3.3	3.6	V
Input Leakage Current (HCLK, HCMD and HDATA2-0 to Ground)	I_I	$0< V_{IN} < V_{CC}$	0.2	-	0.3	µA
Input Leakage Current (HCLK, HCMD and HDATA2-0 to V_{DD})	I_I	$0< V_{IN} < V_{CC}$	0.2	-	0.3	µA
Input Leakage Current at HDATA3 to Ground	I_I	$0< V_{IN} < V_{CC}$	-	-	0.43	µA

Output High Voltage at HCMD	V_{OH}	Clock = 20MHz	-	-	3588	mV
Output High Voltage at HDATA	V_{OH}	Clock = 20MHz	-	-	3586	mV
Output Low Voltage at HCMD	V_{OL}	Clock = 20MHz	39	-	-	mV
Output Low Voltage at HDATA	V_{OL}	Clock = 20MHz	39	-	-	mV
Read/Write Current	I_{CC}		-	-		mA

CHAPTER 5 PACKAGE DIMENSION

SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	0.61 (24)	0.66 (26)	0.70 (28)
A1	0.00 (0)	0.02 (0.8)	0.05 (2)
A3	0.13 (5) REF		
b	0.13 (5)	0.20 (8)	0.25 (10)
D	6.40 (252)	6.50 (256)	6.60 (260)
E	4.40 (173)	4.50 (177)	4.60 (181)
D2	5.00 (197)	5.10 (201)	5.20 (205)
E2	3.00 (118)	3.10 (122)	3.20 (126)
e	0.40 (16) BSC		
L	0.30 (12)	0.40 (16)	0.50 (20)
y	---	0.08 (3)	---
k	0.30 (12)	---	---

NOTE: 1. ALL DIMENSIONS IN MILLIMETERS.

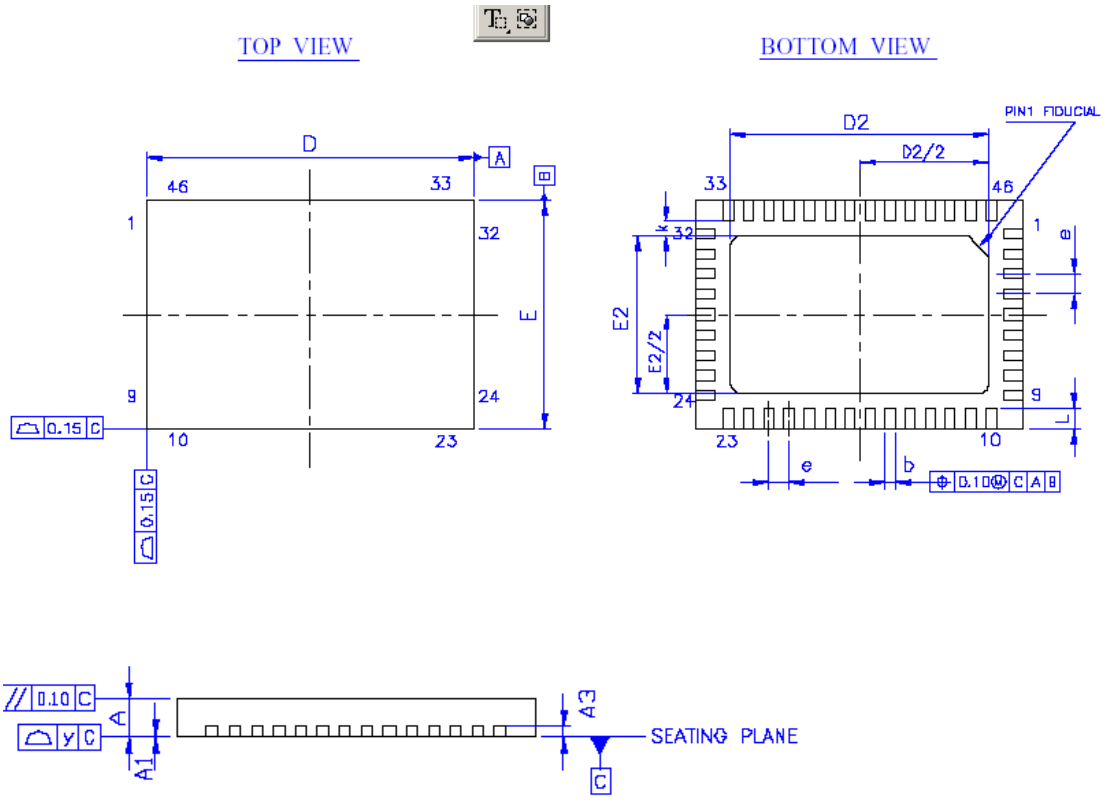
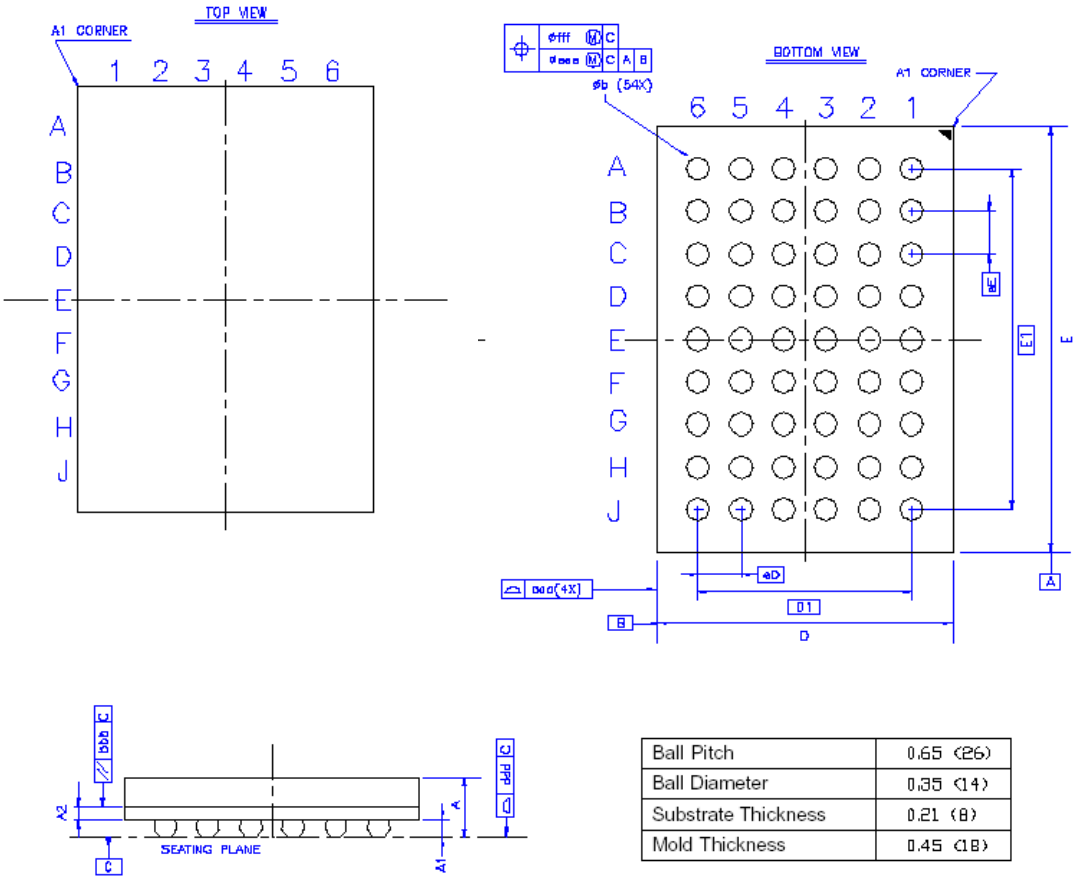


Figure 5.1- 46 Pin LQFN Package Dimension

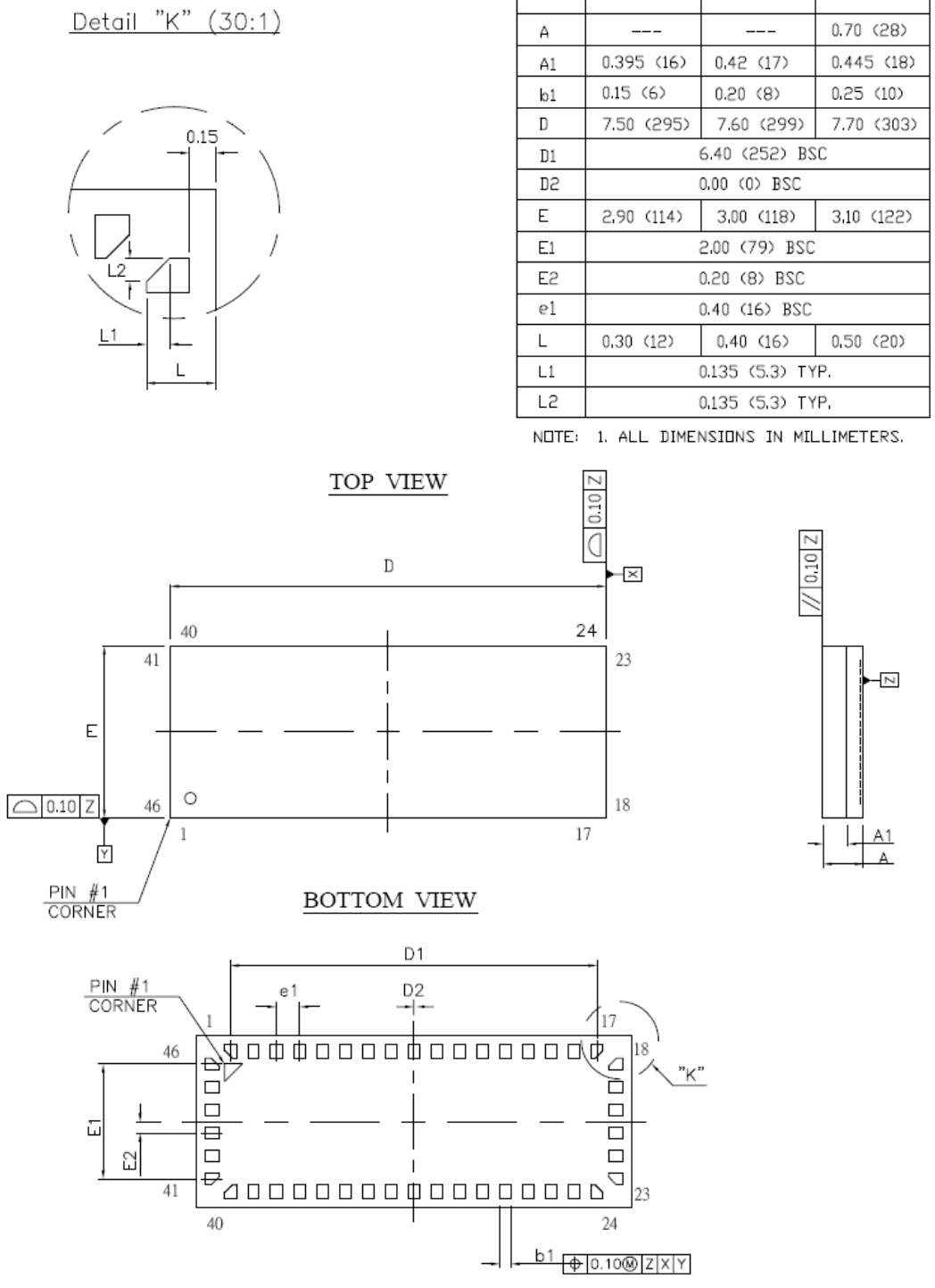
SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A			1.00 (39)
A1	0.22 (9)		0.32 (13)
A2		0.21 (8)	
b	0.32 (13)		0.42 (17)
D		4.5 (177)	
E		6.5 (256)	
eD	0.65 (26) BSC		
D1	3.25 (128) BSC		
eE	0.65 (26) BSC		
E1	5.20 (205) BSC		
aaa	0.10 (4)		
bbb	0.10 (4)		
ddd	0.08 (3)		
eee	0.15 (6)		
fff	0.08 (3)		

NOTE: 1. ALL DIMENSIONS IN MILLIMETERS.



Ball Pitch	0.65 (26)
Ball Diameter	0.35 (14)
Substrate Thickness	0.21 (8)
Mold Thickness	0.45 (18)

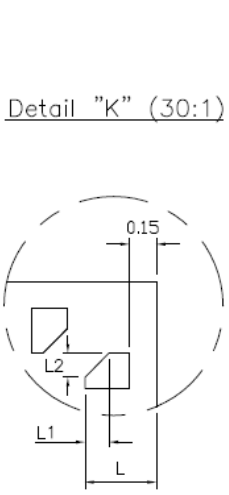
Figure 5.2- 54 Pin VFBGA Package Dimension



SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	---	---	0.70 (28)
A1	0.395 (16)	0.42 (17)	0.445 (18)
b1	0.15 (6)	0.20 (8)	0.25 (10)
D	7.50 (295)	7.60 (299)	7.70 (303)
D1	6.40 (252) BSC		
D2	0.00 (0) BSC		
E	2.90 (114)	3.00 (118)	3.10 (122)
E1	2.00 (79) BSC		
E2	0.20 (8) BSC		
e1	0.40 (16) BSC		
L	0.30 (12)	0.40 (16)	0.50 (20)
L1	0.135 (5.3) TYP.		
L2	0.135 (5.3) TYP.		

NOTE: 1. ALL DIMENSIONS IN MILLIMETERS.

Figure 5.3- 46 PIN LGA Package Dimension



SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	---	---	0.70 (28)
A1	0.395 (16)	0.42 (17)	0.445 (18)
b1	0.15 (6)	0.20 (8)	0.25 (10)
b2	0.20 (8)	0.25 (10)	0.30 (21)
D	7.50 (295)	7.60 (299)	7.70 (303)
D1	6.40 (252) BSC		
D2	0.00 (0) BSC		
E	2.90 (114)	3.00 (118)	3.10 (122)
E1	2.00 (79) BSC		
E2	0.20 (8) BSC		
e1	0.40 (16) BSC		
e2	0.50 (20) BSC		
L	0.30 (12)	0.40 (16)	0.50 (20)
L1	0.135 (5.3) TYP.		
L2	0.135 (5.3) TYP.		

NOTE: 1. ALL DIMENSIONS IN MILLIMETERS.

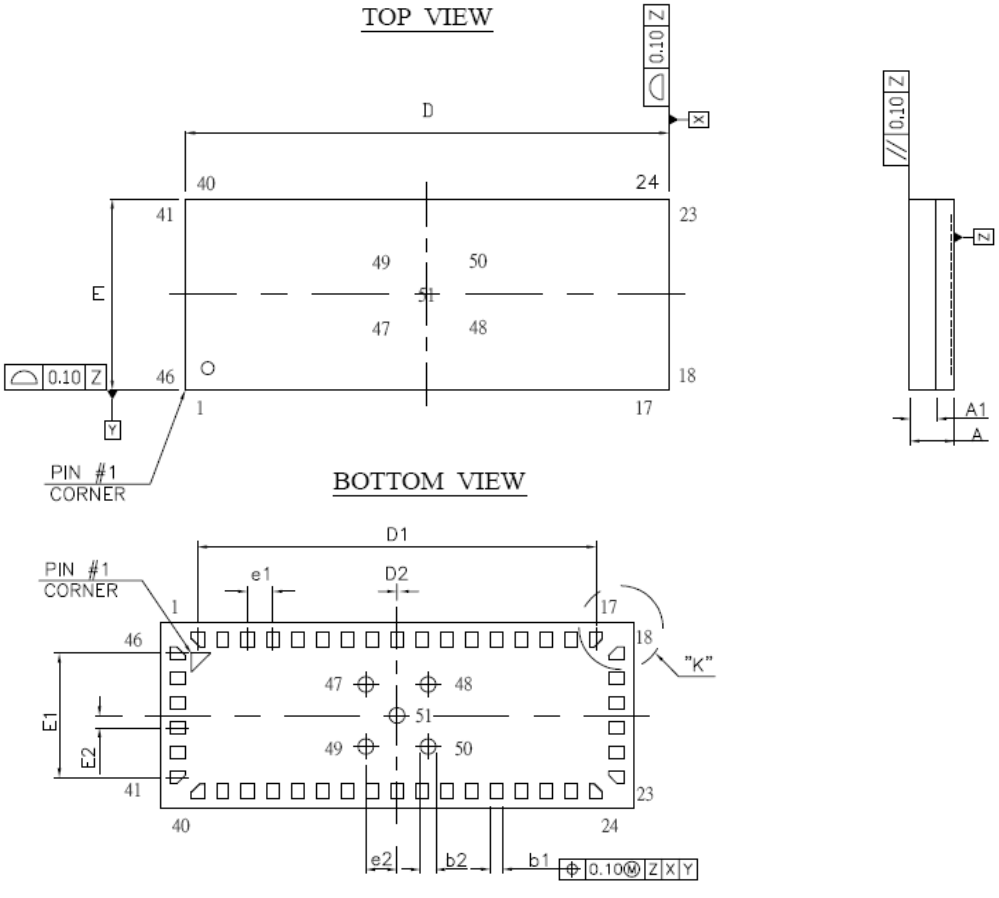


Figure 5.4- 51 PIN LGA Package Dimension

CHAPTER 6 ORDERING INFORMATION

Table 6.1- Ordering Information

Part Number	Package	Normal/Green	Version	Status
GL424-PMGXX	46-Pin LQFN	Green Package	XX	Available
GL424-PMGXX	54-Pin VFBGA	Green Package	XX	Available
GL424-WMGXX	46-Pin LGA	Green Package	XX	Available
GL424-WOGXX	51-Pin LGA	Green Package	XX	Available