Description

The VS-709 is a Voltage Controlled SAW Oscillator that operates at the fundamental frequency from one of the two internal SAW filters. The SAW filters are high-Q Quartz devices that enable the circuit to achieve low phase jitter performance over a wide operating temperature range. A divider circuit is deployed for output frequencies less than 600 MHz. The selectable dual oscillator is housed in a hermetically sealed leadless surface mount package and offered on tape and reel. It has a tri-state Frequency Select function that provides one of three conditions: Frequency 1, Output Disable, or Frequency 2.

Features

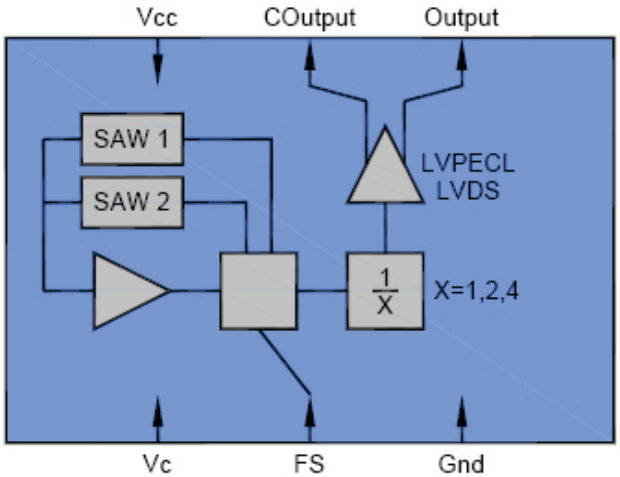
- Industry Standard Package, 5.0 x 7.0 x 1.8 mm
- 5th Generation ASIC Technology for Ultra Low Jitter
  120 fs-rms (fN = 622.08 MHz, 12 kHz to 20 MHz)
  105 fs-rms (fN = 622.08 MHz, 50 kHz to 80 MHz)
- Output Frequencies from 150 MHz to 1000 MHz
- Spurious Suppression, 90 dBc Typical
- 2.5V or 3.3V Supply Voltage
- LVPECL or LVDS Output Configurations
- Tri-State Frequency Select (F1, OD, F2)
- Compliant to EC RoHS6 Directive

Applications

PLL circuits for clock smoothing and frequency translation

Description	Standard
SONET / SDH	GR-253-CORE
OTN (Optical Transport Network)	ITU-T G.709/Y.1331
10 GbE (Gigabit Ethernet)	IEEE 802.3ae
10 GFC (Gigabit Fibre Channel)	INCITS 364-2003
40 GbE & 100 GbE	IEEE 802.3ba
Synchronous Ethernet	ITU-T G.8261
WiMax	IEEE 802.16

Block Diagram



Performance Specifications

Electrical Performance					
Parameter	Symbol	Min	Typical	Maximum	Units
Frequency					
Nominal Frequency [1, 2, 3]	f_N	150		1000	MHz
Absolute Pull Range [1, 2, 3, 9]	APR	±50			ppm
Linearity [2, 4, 9]	Lin		±7		%
Gain Transfer [2, 9]	K_V		+445		ppm/V
Temperature Stability [1, 7]	f_{STAB}		±100		ppm
Supply					
Voltage (± 10%) [2, 3]	V_{CC}	2.97	3.3	3.63	V
Current (Typical 50Ω Load) [3]	I_{CC}		73		mA
Current (No Load) [3]	I_{CC}		60	75	mA
Outputs					
Mid Level [2, 3]		V_{CC}-1.5	V_{CC}-1.3	V_{CC}-1.1	mV
Single Ended Swing [2, 3]			750		mV-pp
Differential Swing [2, 3]			1.5		V-pp
Current [7]	I_{OUT}			20	mA
Rise Time [6, 7]	t_R		180	250	ps-pp
Fall Time [6, 7]	t_F		180	250	ps-pp
Symmetry [2, 3]	SYM	45	50	55	%
Spurious Suppression [7]		85	90		dBc
Jitter (600 ≤ f_N ≤ 1000) [7, 8]	ϕJ		150		fs-rms
Jitter (300 ≤ f_N ≤ 500) [7, 8]	ϕJ		190		fs-rms
Jitter (150 ≤ f_N ≤ 250) [7, 8]	ϕJ		280		fs-rms
Control Voltage					
Input Impedance (F1 or F2 Enabled) [7]	Z_C		123		kΩ
Input Impedance (Output Disabled) [7]	Z_C		472		kΩ
Modulation Bandwidth [7]	BW		200		kHz
Operating Temperature [1, 3]	T_{OP}	-40		+85	°C
Package Size		5.0 x 7.0 x 1.8			mm

1] See Standard Frequencies and Ordering Information (Pg 8).
2] Parameters are tested with production test circuit (Pg 3).
3] Parameters are tested at ambient temperature with test limits guard-banded for specified operating temperature.
4] Measured as the maximum deviation from the best straight-line fit, per MIL-0-55310.
5] The Vc Model is described below (Fig 1).
6] Parameters are described with waveform diagram below (Fig 2).
7] Not tested in production, guaranteed by design, verified at qualification.
8] For Frequencies > 600 MHz, Jitter is Integrated across 50 kHz to 80 MHz.
For Frequencies < 600 MHz, Jitter is Integrated across 12 kHz to 20 MHz. (Both per GR-253-CORE Issue3).
9] Tested with Vc = 0.3V to 3.0V.

Fig 1: V_C Model - F1 or F2 Enabled

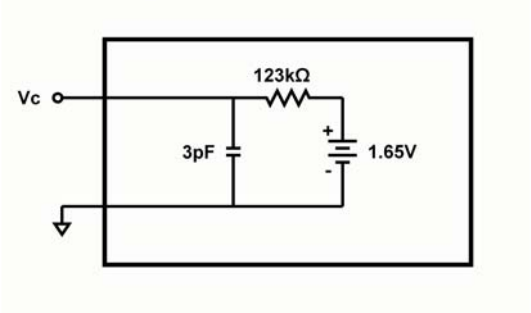
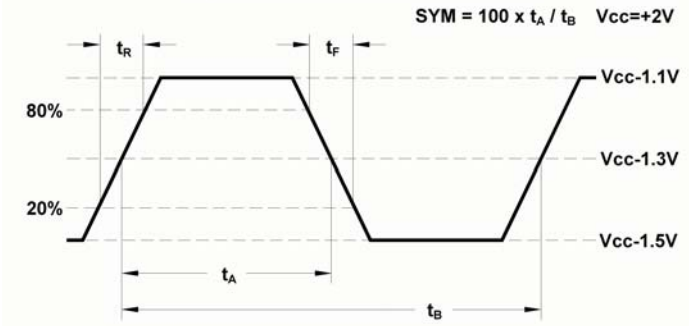


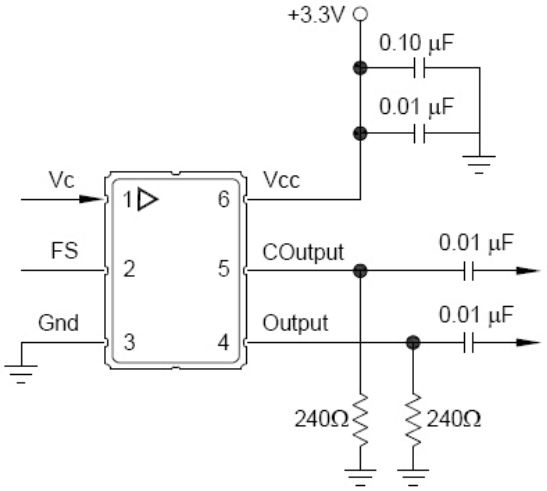
Fig 2: 10K LV-PECL Waveform



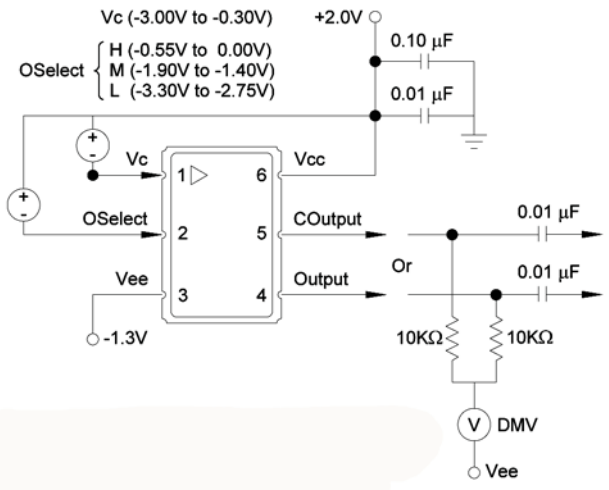
Absolute Maximum Ratings			
Parameter	**Symbol**	**Ratings**	**Unit**
Power Supply	V_{CC}	0 to 6	V
Input Current	I_{IN}	100	mA
Output Current	I_{OUT}	25	mA
Voltage Control Range	V_C	0 to V_{CC}	V
Output Select	OSelect	0 to V_{CC}	V
Storage Temperature	T_{STR}	-55 to 125	°C
Soldering Temperature / Duration	T_{PEAK} / t_P	260 / 40	°C / sec

Stresses in excess of the absolute maximum ratings can permanently damage the device. Also, exposure to these absolute maximum ratings for extended periods may adversely affect device reliability. Functional operation is not implied at these or any other conditions in excess of those represented in the operational sections of this datasheet. Permanent damage is also possible if any device input (Vc or OS) draws >100 mA.

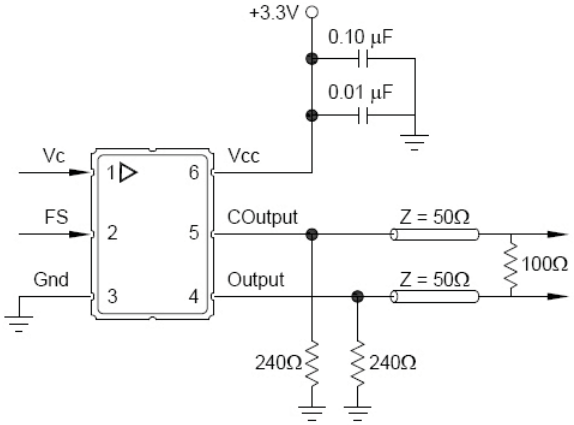
Test Circuits & Output Load Configuration



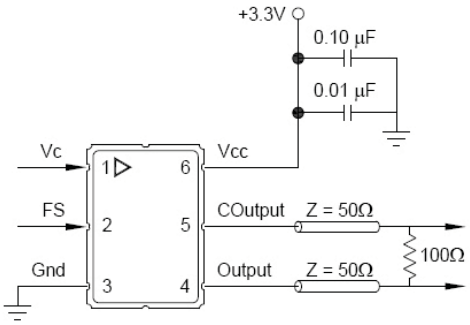
Functional Test: Allows use of standard power supply biasing configuration. Pull down resistors are used for LV-PECL outputs and are removed for LVDS outputs. Since the LVDS outputs are AC coupled, the output DC levels cannots be measured.



Production Test: DC levels shown for VEE, OSelect, & Vc are for devices configured for 3.3V operation. LV-PECL outputs are DC coupled to 50Ω test equipment. LVDS outputs are connected to a digital volt meter, then AC coupled to the test equipment. The digital volt meter allows for Mid Level & Swing measurements.

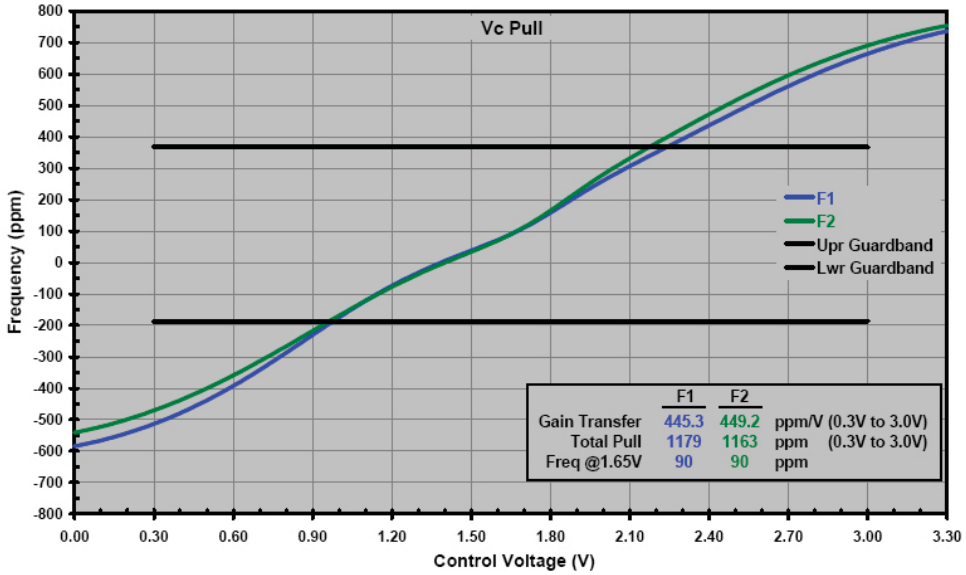


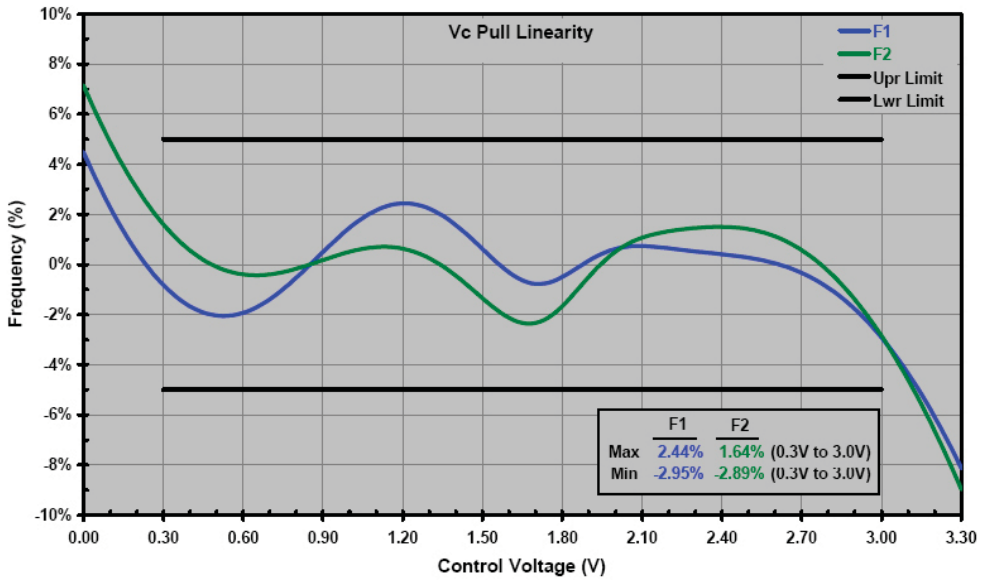
LV-PECL to LV-PECL: For short transmission lengths, the pull down resistor values shown provide reasonable power consumption and waveform performance.

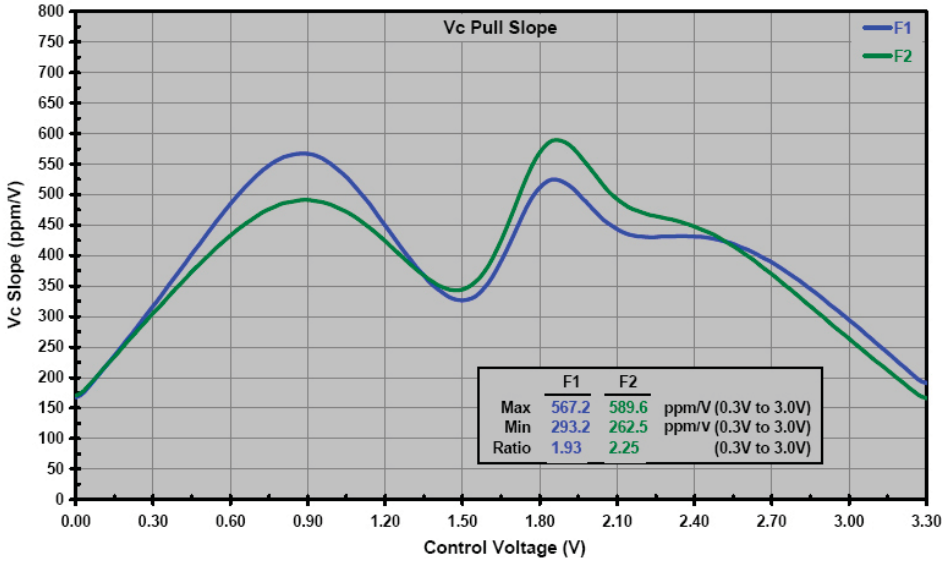


LVDS to LVDS: The 100Ω resistor should be removed if this load is provided internally within the LVDS receiver.

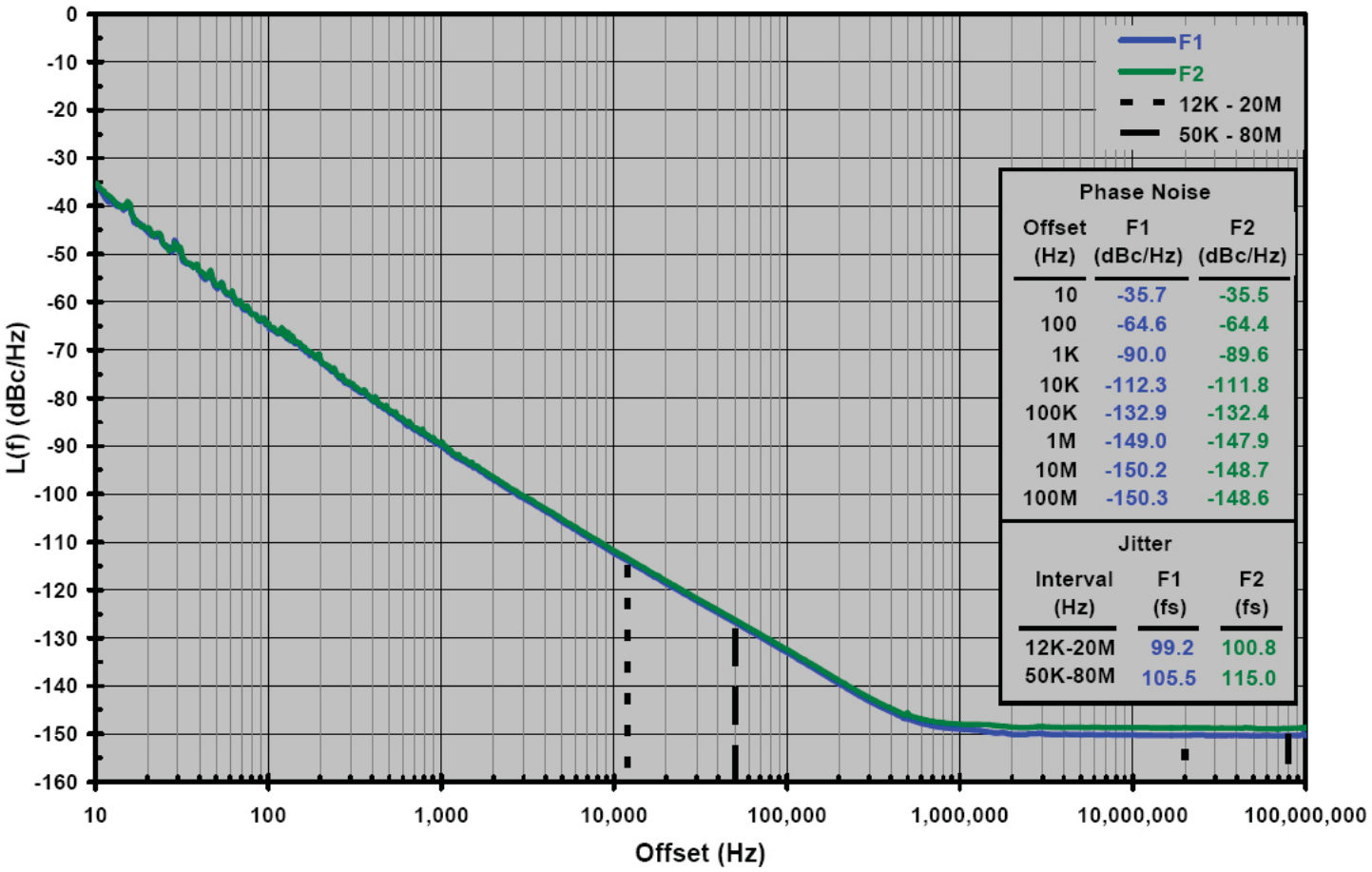
Typical Characteristics: Vc Pull, Vc Pull Linearity, Vc Pull Slope







Typical Characteristics: Phase Noise & Jitter



Phase Noise

Offset (Hz)	F1 (dBc/Hz)	F2 (dBc/Hz)
10	-35.7	-35.5
100	-64.6	-64.4
1K	-90.0	-89.6
10K	-112.3	-111.8
100K	-132.9	-132.4
1M	-149.0	-147.9
10M	-150.2	-148.7
100M	-150.3	-148.6

Jitter

Interval (Hz)	F1 (fs)	F2 (fs)
12K-20M	99.2	100.8
50K-80M	105.5	115.0

Reliability

VI qualification includes aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The VS-705 family is capable of meeting the following qualification tests:

Environmental Compliance	
Parameter	**Conditions**
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2016
Moisture Sensitivity Level	IPC/JEDEC J-STD-020, MSL1

Handling Precautions

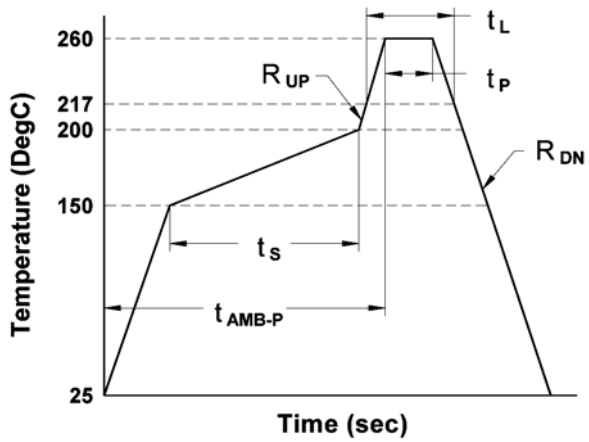
Although ESD protection circuitry has been designed into the VS-709 proper precautions should be taken when handling and mounting. VI employs a human body model (HBM) and a charged-device model (CDM) for ESD susceptibility testing and design protection evaluation.

ESD Ratings		
Model	**Minimum**	**Conditions**
Human Body Model	1500V	MIL-STD-883, Method 3015
Charged Device Model	1000V	JEDEC, JESD22-C101
Machine Model	200 V	JEDEC, JESD22-A115-A

Reflow Profile (IPC/JEDEC J-STD-020)		
Parameter	**Symbol**	**Value**
PreHeat Time	t_S	60 sec Min, 180 sec Max
Ramp Up	R_{UP}	3 °C/sec Max
Time Above 217 °C	t_L	60 sec Min, 150 sec Max
Time To Peak Temperature	T_{AMB-P}	480 sec Max
Time at 260 °C	t_P	20 sec Min, 40 sec Max
Ramp Down	R_{DN}	6 °C/sec Max

The VS-709 has been qualified to meet the JEDEC standard for Pb-Free assembly. The temperatures and time intervals listed are based on the Pb-Free small body requirements. The temperatures refer to the topside of the package, measured on the package body surface. The VS-709 device is hermetically sealed so an aqueous wash is not an issue.

Terminal Plating: Electroless Au > 1.50 µm over
Electroless Ni > 1.90 µm



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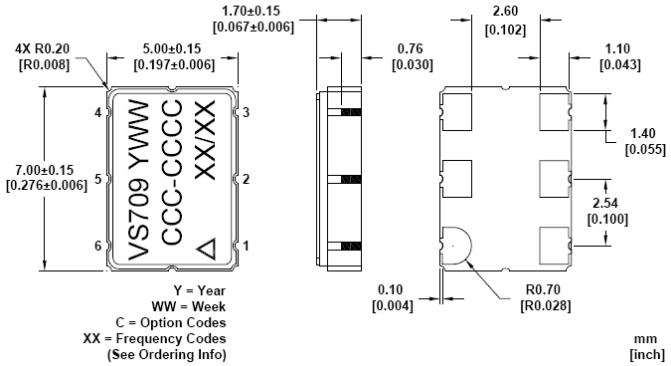
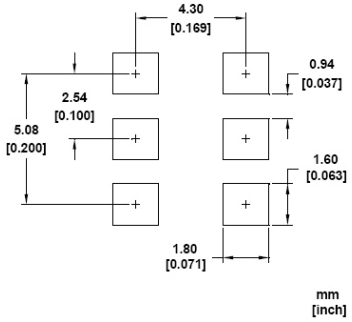
Outline & Marking Diagram



Suggested Pad Layout

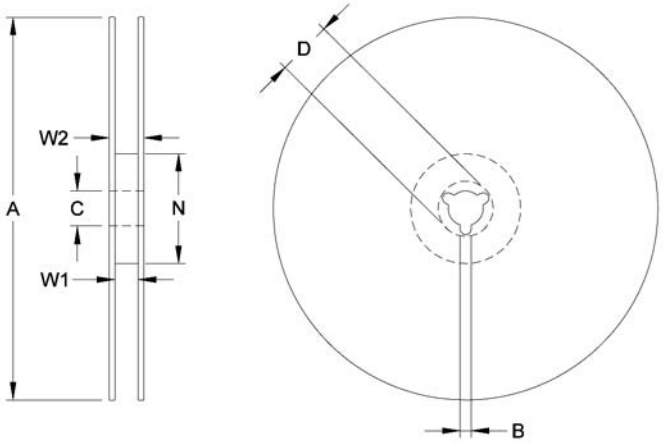


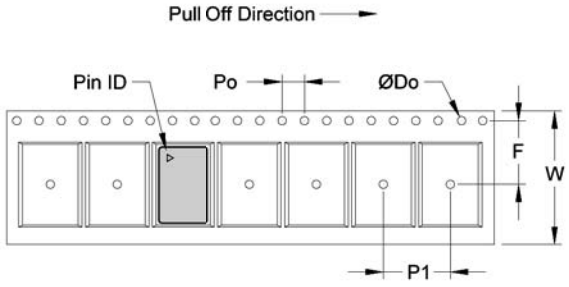
Pin Out		
Pin	**Symbol**	**Function**
1	V_C	Control Voltage
2	FS	Frequency Select
3	GND	Case and Electrical Ground
4	Output	Output
5	COutput	Complementary Output
6	V_{CC}	Power Supply Voltage

Frequency Select (Tri-State LV-CMOS)		
FS	**Voltage Range**	**Result**
H	($5V_{CC}$ / 6) to V_{CC}	F2
M	(V_{CC} / 2) ± 15%(V_{CC} / 2)	OD
L	Gnd to (V_{CC} / 6)	F1

LV-CMOS Tri-State Control
Floating FS Results in OD

Tape & Reel (EIA-481-2-A)





Tape Dimensions (mm)						Reel Dimensions (mm)							
Dimension	**W**	**F**	**Do**	**Po**	**P1**	**A**	**B**	**C**	**D**	**N**	**W1**	**W2**	**# Per Reel**
Tolerance	**Typ**	**Typ**	**Typ**	**Typ**	**Typ**	**Typ**	**Min**	**Typ**	**Min**	**Min**	**Typ**	**Max**	
VS-709	16	7.5	1.5	4	8	178	1.5	13	20.2	50	16.4	22.4	200

Standard Frequencies (MHz)					
155.520000 M2	156.250000 M3	161.132813 M4	166.628572 M5	167.331646 N2	168.040678 N3
173.370748 ND	184.320000 NH	307.200000 RX	311.040000 P1	368.640000 RY	614.400000 RG
622.080000 P2	625.000000 P3	644.531250 P4	657.421875 PB	666.514286 P5	669.326582 R3
672.162712 R5	690.569196 R4	693.482991 R6	696.421478 V1	696.614900 V8	698.812330 VC
699.426250 VM	707.352650 TC	718.863800 V6	737.280000 TL	753.621100 VN	905.499558 V7

Other Frequencies Available Upon Request.

Ordering Information

VS - 709 - E C E - K A A N - P2 / P4

Product Family
VS: VCSO

Package
709: 5.0 x 7.0 x 1.8 mm

Input
E: 3.3 V
H: 2.5V (Future)

Output
C: LVPECL
D: LVDS

Operating Temperature
E: -40 to 85 °C

Frequency 1
(See Above)

Frequency 2
(See Above)

Other (Future Use)
N: N/A

Oscillator Gain
A: Standard
B: Low

Control Logic (Tri-State)
A: L = F1, M = OD, H = F2

Absolute Pull Range
K: ± 50 ppm
S: ± 100 ppm
T: ± 120 ppm

Example1: VS-709-ECE-KAAN-M2/NH
Example2: VS-709-EDE-SAAN-R3/R4

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Revision History

Revision History		
Date	**Approved**	**Description**
15Sep2010	BW	Clarified Floating FS Functionality.
16Jul2010	BW	±120 ppm APR added to ordering information. Standard frequency table updated.
25Jun2010	BW	Standard frequency table updated.
23Mar2010	BW	Official Release