M52743SP/M52744SP

I²C BUS CONTROLLED 3-CHANNEL VIDEO PREAMPLIFIER

DESCRIPTION

M52743SP and M52744SP is semiconductor integrated circuit for CRT display monitor.

It includes OSD blanking, OSD mixing, retrace blanking, wide band amplifre, brightness control.

Main/sub contrast and OSD adjust function can be controlled by I²C bus.

FEATURES

- Frequency band width: RGB.....150MHz (at -3dB)
  OSD.....80MHz
  Input : RGB.....0.7V_{P-P} (typ.)
  OSD.....3V_{P-P} minimum (positive)
  BLK (for OSD).....3V_{P-P} minimum (positive)
  Retrace BLK.....3V_{P-P} minimum (positive)
  Output : RGB.....5.5V_{P-P} (max.)
  OSD.....5V_{P-P} (max.)
- Main contrast and sub contrast can be controlled by I²C bus.
- Include internal and external pedestal clamp circuit.

STRUCTURE

Bipola silicon monolisic IC

APPLICATION

CRT display monitor

RECOMMENDED OPERATING CONDITION

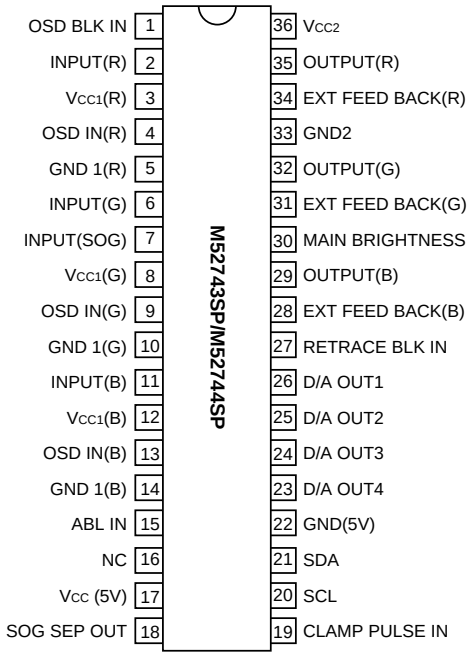
Supply voltage range.....11.5 to 12.5V (V3, V8, V12, V36)
4.5 to 4.4V (V17)

Rated supply voltage.....12.0V (V3, V8, V12, V36)
5.0V (V17)

MAJOR SPECIFICATION

Bus controlled 3ch video pre-amp with OSD mixing function and retrace blanking function

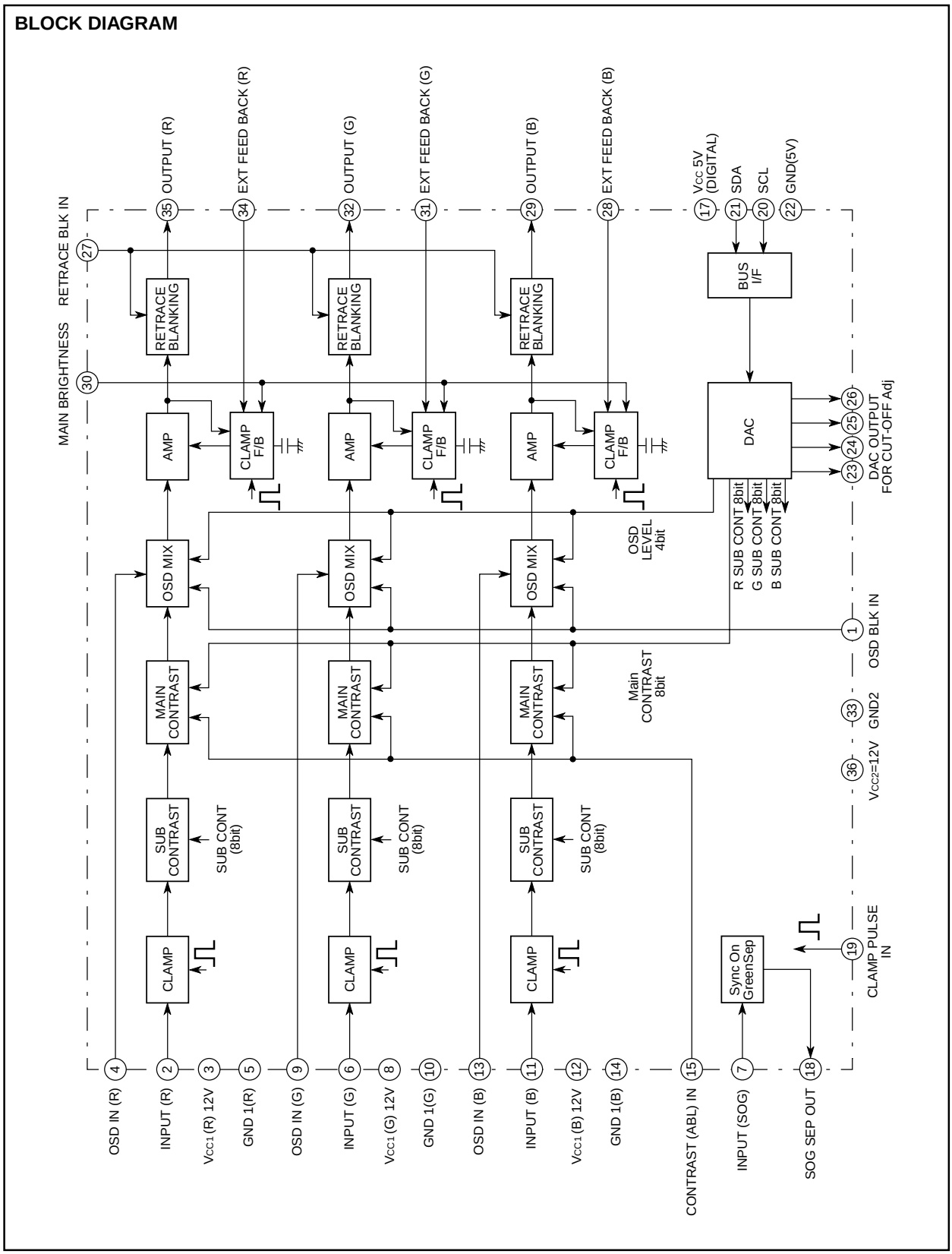
PIN CONFIGURATION (TOP VIEW)



Outline 36P4E

NC:NO CONNECTION

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	13.0	V
P_d	Power dissipation	2403	mW
T_{opr}	Ambient temperature	-20 to +75	°C
T_{stg}	Storage temperature	-40 to +150	°C
V_{opr}	Recommended supply	12.0	V
$V_{opr'}$	Voltage range	10.5 to 12.5	V
θjc	Case temperature	22	°C/W

ELECTRICAL CHARACTERISTICS (V_{CC}=12V, 5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test point (s)	Input							CTL voltage		BUS CTL (H)											Limits			Unit
			2,6,11 RGB in	1 OSD BLK	4,9,13 OSD in	19 CP in	27 ReT BLK	7 SOG in		30 Bri-ght	15 ABL	00H Main cont	01H Sub cont 1	02H Sub cont 2	03H Sub cont 3	04H OSD Adj	05H BLK Adj	06H D/A OUT 1	07H D/A OUT 2	08H D/A OUT 3	09H D/A OUT 4	0BH INT EXT	Min.	Typ.	Max.	
I_{CC1}	Circuit current1	I_A	a	a	a	b SG5	a	a		4.0	5.0	FFH 255	FFH 255	FFH 255	FFH 255	00H 0	00H 0	FFH 255	FFH 255	FFH 255	FFH 255	00H 0	–	110	130	mA
I_{CC2}	Circuit current2	I_B	a	a	a	b SG5	a	a		4.0	5.0												–	18	22	mA
Vomax	Output dynamic range	OUT	b SG2	a	a	b SG5	a	a		Variable	5.0	↓											6.0	8.0	–	V_{P-P}
Vimax	Maximum input	IN OUT	b SG2 Variable	a	a	b SG5	a	a		2.0	5.0	64H 100											1.6	–	–	V_{P-P}
Gv	Maximum gain	OUT	b SG1	a	a	b SG5	a	a		2.0	5.0	FFH 255											16.5	17.7	19.7	dB
ΔGv	Relative maximum gain	–	–	–	–	–	–	–		–	–	–											0.8	1.0	1.2	–
V_{C1}	Main contrast control characteristics1	OUT	b SG1	a	a	b SG5	a	a		2.0	5.0	C8H 200											14.5	16.0	17.5	dB
ΔV_{C1}	Main contrast control relative characteristics1	–	–	–	–	–	–	–		–	–	–											0.8	1.0	1.2	–
V_{C2}	Main contrast control characteristics2	OUT	b SG1	a	a	b SG5	a	a		2.0	5.0	64H 100											8.5	10.0	11.5	dB
ΔV_{C2}	Main contrast control relative characteristics2	–	–	–	–	–	–	–		–	–	–											0.8	1.0	1.2	–
V_{C3}	Main contrast control characteristics3	OUT	b SG1	a	a	b SG5	a	a		2.0	5.0	14H 20											0.2	0.4	0.6	V_{P-P}
ΔV_{C3}	Main contrast control relative characteristics3	–	–	–	–	–	–	–		–	–	–	↓	↓	↓								0.8	1.0	1.2	–
V_{SC1}	Sub contrast control characteristics1	OUT	b SG1	a	a	b SG5	a	a		2.0	5.0	FFH 255	C8H 200	C8H 200	C8H 200								14.8	16.3	17.8	dB
ΔV_{SC1}	Sub contrast control relative characteristics1	–	–	–	–	–	–	–		–	–	–	–	–	–								0.8	1.0	1.2	–
V_{SC2}	Sub contrast control characteristics2	OUT	b SG1	a	a	b SG5	a	a		2.0	5.0	FFH 255	64H 100	64H 100	64H 100								11.1	12.6	14.1	dB
ΔV_{SC2}	Sub contrast control relative characteristics2	–	–	–	–	–	–	–		–	–	–	–	–	–								0.8	1.0	1.2	–
V_{SC3}	Sub contrast control characteristics3	OUT	b SG1	a	a	b SG5	a	a		2.0	5.0	FFH 255	14H 20	14H 20	14H 20								1.4	1.7	2.0	V_{P-P}
ΔV_{SC3}	Sub contrast control relative characteristics3	–	–	–	–	–	–	–		–	–	–	–	–	–			↓	↓	↓	↓	↓	0.8	1.0	1.2	–

ELECTRICAL CHARACTERISTICS (cont.)

Symbol	Parameter	Test point (s)	Input							CTL voltage		BUS CTL (H)											Limits			Unit
			2,6,11 RGB in	1 OSD BLK	4,9,13 OSD in	19 CP in	27 ReT BLK	7 SOG in		30 Bri-ght	15 ABL	00H Main cont	01H Sub cont 1	02H Sub cont 2	03H Sub cont 3	04H OSD Adj	05H BLK Adj	06H D/A OUT 1	07H D/A OUT 2	08H D/A OUT 3	09H D/A OUT 4	0BH INT EXT	Min.	Typ.	Max.	
VMSC	Main/sub contrast control characteristics2	OUT	b SG1	a	a	b SG5	a	a		2.0	5.0	C8H 200	C8H 200	C8H 200	C8H 200	00H 0	00H 0	FFH 255	FFH 255	FFH 255	FFH 255	00H 0	3.2	3.8	4.4	V_{P-P}
ΔVMSC	Main/sub contrast control relative characteristics2	–	–	–	–	–	–	–		–	–	–	–	–	–								0.8	1.0	1.2	–
ABL1	ABL control characteristics1	OUT	b SG1	a	a	b SG5	a	a		2.0	4.0	FFH 255	FFH 255	FFH 255	FFH 255								3.8	4.6	5.4	V_{P-P}
ΔABL1	ABL control relative characteristics1	–	–	–	–	–	–	–		–	–												0.8	1.0	1.2	–
ABL2	ABL control characteristics2	OUT	b SG1	a	a	b SG5	a	a		2.0	2.0												2.2	2.7	3.2	V_{P-P}
ΔABL2	ABL control relative characteristics2	–	–	–	–	–	–	–		–	–												0.8	1.0	1.2	–
V_{B1}	Brightness control characteristics1	OUT	a	a	a	b SG5	a	a		4.0	5.0												3.3	3.7	4.1	V
ΔV_{B1}	Brightness control relative characteristics1	–	–	–	–	–	–	–		–	–												-0.3	0	0.3	–
V_{B2}	Brightness control characteristics2	OUT	a	a	a	b SG5	a	a		2.0	5.0												1.5	1.8	2.1	V
ΔV_{B2}	Brightness control relative characteristics2	–	–	–	–	–	–	–		–	–												-0.3	0	0.3	–
V_{B3}	Brightness control characteristics3	OUT	a	a	a	b SG5	a	a		1.0	5.0												0.7	0.9	1.1	V
ΔV_{B3}	Brightness control relative characteristics3	–	–	–	–	–	–	–		–	–	↓											-0.3	0	0.3	–
F_{C1}	Frequency characteristics1 (f=50MHz)	OUT	b SG3	a	a	a 5V	a	a		Variable	5.0	Variable											-2.0	0	2.5	dB
ΔF_{C1}	Frequency relative characteristics1 (f=50MHz)	–	–	–	–	–	–	–		–	–	–	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	-1.0	0	1.0	dB
$F_{C1'}$	Frequency characteristics1 (f=150MHz)	OUT	b SG3	a	a	a 5V	a	a		Variable	5.0	Variable	FFH 255	FFH 255	FFH 255	00H 0	00H 0	FFH 255	FFH 255	FFH 255	FFH 255	00H 0	-3.0	0	3.0	dB
$\Delta F_{C1'}$	Frequency relative characteristics1 (f=150MHz)	–	–	–	–	–	–	–															-1.0	0	1.0	dB
F_{C2}	Frequency characteristics2 (f=150MHz)	OUT	b SG3	a	a	a 5V	a	a		Variable	5.0												-3.0	3.0	5.0	dB
ΔF_{C2}	Frequency relative characteristics2 (f=150MHz)	–	–	–	–	–	–	–		–	–	↓											-1.0	0	1.0	dB
C.T.1	Crosstalk 1 (f=50MHz)	OUT(29) OUT(32)	2bSG3 6a 11a	a	a	a 5V	a	a		Variable	5.0	FFH 255											–	-25	-20	dB
C.T.1'	Crosstalk 1 (f=150MHz)	OUT(29) OUT(32)	2bSG3 6a 11a	a	a	a 5V	a	a		Variable	5.0												–	-15	-10	dB
C.T.2	Crosstalk 2 (f=50MHz)	OUT(29) OUT(35)	2a 6bSG3 11a	a	a	a 5V	a	a		Variable	5.0												–	-25	-20	dB
C.T.2'	Crosstalk 2 (f=150MHz)	OUT(29) OUT(35)	2a 6bSG3 11a	a	a	a 5V	a	a		Variable	5.0												–	-15	-10	dB
C.T.3	Crosstalk 3 (f=50MHz)	OUT(32) OUT(35)	2a 6a 11bSG3	a	a	a 5V	a	a		Variable	5.0												–	-25	-20	dB
C.T.3'	Crosstalk 3 (f=150MHz)	OUT(32) OUT(35)	2a 6a 11bSG3	a	a	a 5V	a	a		Variable	5.0	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	–	-15	-10	dB

ELECTRICAL CHARACTERISTICS (cont.)

Symbol	Parameter	Test point (s)	Input							CTL voltage		BUS CTL (H)												Limits			Unit
			2,6,11 RGB in	1 OSD BLK	4,9,13 OSD in	19 CP in	27 ReT BLK	7 SOG in		30 Bri-ght	15 ABL	00H Main cont	01H Sub cont 1	02H Sub cont 2	03H Sub cont 3	04H OSD Adj	05H BLK Adj	06H D/A OUT 1	07H D/A OUT 2	08H D/A OUT 3	09H D/A OUT 4	0BH INT EXT			Min.	Typ.	Max.	
Tr	Pulse characteristics1 (4V$_{P-P}$)	OUT	b SG1	a	a	b SG5	a	a		Variable	5.0	Variable	FFH 255	FFH 255	FFH 255	00H 0	00H 0	FFH 255	FFH 255	FFH 255	FFH 255	00H 0			–	1.7	–	ns
Tf	Pulse characteristics2 (4V$_{P-P}$)	OUT	b SG1	a	a	b SG5	a	a		Variable	5.0	Variable													–	3.0	–	ns
VthCP	Clamp pulse threshold voltage	OUT	b SG1	a	a	b SG5 Variable	a	a		2.0	5.0	FFH 255													1.0	1.5	2.0	V
WCP	Clamp pulse minimum width	OUT	b SG1	a	a	b SG5 Variable	a	a		2.0	5.0														0.2	0.5	–	µs
P_{DCH}	Pedestal voltage temperature characteristics1	OUT	b SG1	a	a	b SG5	a	a		2.0	5.0														-3.0	0	0.3	V
P_{DCL}	Pedestal voltage temperature characteristics2	OUT	b SG1	a	a	b SG5	a	a		2.0	5.0					↓									-3.0	0	0.3	V
OTr	OSD pulse characteristics1	OUT	a	a	b SG6	b SG5	a	a		2.0	5.0					08H 8									–	3.0	6.0	ns
OTf	OSD pulse characteristics2	OUT	a	a	b SG6	b SG5	a	a		2.0	5.0					08H 8									–	3.0	6.0	ns
Oaj1	OSD adjust control characteristics1	OUT	a	b SG6	b SG6	b SG5	a	a		2.0	5.0					0FH 15									4.6	5.4	6.2	V$_{P-P}$
ΔOaj1	OSD adjust control relative characteristics1	–	–	–	–	–	–	–		–	–					–									0.8	1.0	1.2	–
Oaj2	OSD adjust control characteristics2	OUT	a	b SG6	b SG6	b SG5	a	a		2.0	5.0					08H 8									2.8	3.3	3.8	V$_{P-P}$
ΔOaj2	OSD adjust control relative characteristics2	–	–	–	–	–	–	–		–	–					–									0.8	1.0	1.2	–
Oaj3	OSD adjust control characteristics3	OUT	a	b SG6	b SG6	b SG5	a	a		2.0	5.0					08H 8									0	0.1	0.5	V$_{P-P}$
ΔOaj3	OSD adjust control relative characteristics3	–	–	–	–	–	–	–		–	–					–									0.8	1.0	1.2	–
VthOSD	OSD input threshold voltage	OUT	a	b SG6	b SG6 Variable	b SG5	a	a		2.0	5.0					08H 8									2.2	2.7	3.2	V
VthBLK	OSD BLK input threshold voltage	OUT	b SG1	b SG6 Variable	a	b SG5	a	a		2.0	5.0					00H 0	↓								2.2	2.7	3.2	V
HBLK1	Retrace BLK characteristics1	OUT	a	a	a	b SG5	b SG7	a		2.0	5.0						0FH 15								1.7	2.0	2.3	V
HBLK2	Retrace BLK characteristics2	OUT	a	a	a	b SG5	b SG7	a		2.0	5.0						06H 6								0.7	1.0	1.3	V
HBLK3	Retrace BLK characteristics3	OUT	a	a	a	b SG5	b SG7	a		2.0	5.0						00H 0								0.1	0.4	0.7	V
VthRET	Retrace BLK input threshold voltage	OUT	a	a	a	b SG5	b SG7 Variable	a		2.0	5.0	↓	↓	↓	↓	↓	08H 8	↓	↓	↓	↓	↓			1.0	1.5	2.0	V
SS-NV	SOG input maximum noize voltage	SonG IN Sync OUT	a	a	a	a	a	b SG4 Variable		2.0	5.0														0	0.01	0.02	V$_{P-P}$
SS-SV	SOG minimum input voltage	SonG IN Sync OUT	a	a	a	a	a	b SG4 Variable		2.0	5.0														0.2	0.3	–	V$_{P-P}$
VSH	Sync output hi level	Sync OUT	a	a	a	a	a	b SG4		2.0	5.0														4.5	4.9	5.0	V
VSL	Sync output lo level	Sync OUT	a	a	a	a	a	b SG4		2.0	5.0														0	0.3	0.6	V
TDS-F	Sync output delay time1	Sync OUT	a	a	a	a	a	b SG4		2.0	5.0														0	60	90	ns

ELECTRICAL CHARACTERISTICS (cont.)

Symbol	Parameter	Test point (s)	Input							CTL voltage		BUS CTL (H)											Limits			Unit
			2,6,11 RGB in	1 OSD BLK	4,9,13 OSD in	19 CP in	27 ReT BLK	7 SOG in		30 Bri-ght	15 ABL	00H Main cont	01H Sub cont 1	02H Sub cont 2	03H Sub cont 3	04H OSD Adj	05H BLK Adj	06H D/A OUT 1	07H D/A OUT 2	08H D/A OUT 3	09H D/A OUT 4	0BH INT EXT	Min.	Typ.	Max.	
TDS-R	Sync output delay time2	Sync OUT	a	a	a	a	a	b SG4		2.0	5.0												0	60	90	ns
VOH	D/A H output voltage	D/A OUT	a	a	a	a	a	a		2.0	5.0	FFH 255	FFH 255	FFH 255	FFH 255	00H 0	00H 0	FFH 255	FFH 255	FFH 255	FFH 255	00H 0	4.5	5.0	5.5	VDC
VOL	D/A L output voltage	D/A OUT	a	a	a	a	a	a		2.0	5.0							00H 0	00H 0	00H 0	00H 0		0	0.5	1.0	VDC
IAO	D/A output current range	D/A OUT	a	a	a	a	a	a		2.0	5.0							Variable	Variable	Variable	Variable		-1.0	–	0.4	mA
DNL	D/A nonlinearity	D/A OUT	a	a	a	a	a	a		2.0	5.0	↓	↓	↓	↓	↓	↓	Variable	Variable	Variable	Variable	↓	-1.0	–	1.0	LSB

ELECTRICAL CHARACTERISTICS TEST METHOD

I_{CC1} Circuit current1

Measuring conditions are as listed in supplementary Table. Mesured with a current meter at test point IA.

I_{CC2} Circuit current2

Measureing conditions are as listed in supplemtary Table. Measured with a current meter at test point IB.

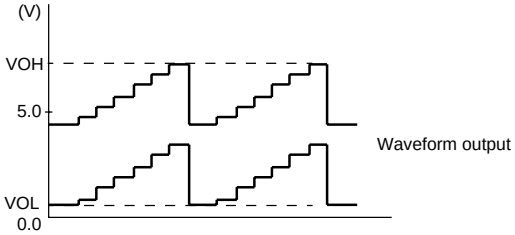
Vomax Output dynamic range

Decrease V30 gradually, and measure the voltage when the bottom of waveform output is distorted. The voltage is called VCL.

Next, increase V30 gradually, and measure the voltage when the top of waveform output is distorted. The voltage is called VOH.

Voltage Vomax is calculated by the equation below:

$$Vomax = VOH - VOL$$



Vimax Maximum input

Increase the input signal (SG2) amplitude gradually, starting from 700mV_{P-P}. Measure the amplitude of the input signal when the output signal starts becoming distorted.

Gv Maximum gain

Input SG1, and read the amplitude output at OUT (29, 32, 35). The amplitude is called VOUT (29, 32, 35). Maximum gain G_V is calculated by the equation below:

$$G_V = 20\text{Log}\frac{VOUT}{0.7}\ \text{(dB)}$$

ΔGv Relative maximum gain

Relative maximum gain ΔG_V is calculated by the equation bellow:

ΔG_V= VOUT (29)/VOUT (32),
VOUT (32)/VOUT (35),
VOUT (35)/VOUT (29)

V_{C1} Main contrast control characteristics1

Measureing the amplitude output at OUT (29, 32, 35). The measured value is called VOUT (29, 32, 35). Main contrast control characterics V_{C1} is calculated by the equation bellow:

$$V_{C1} = 20\text{Log}\frac{VOUT}{0.7}\ \text{(dB)}$$

ΔV_{C1} Main contrast control relative characteristics1

Relative characteristics ΔV_{C1} is calculated by the equation bellow:

ΔV_{C1}=VOUT (29)/VOUT (32),
VOUT (32)/VOUT (35),
VOUT (35)/VOUT (29)

V_{C2} Main contrast control characteristics2

Measuring condition and procedure are the same as described in V_{C1}.

ΔV_{C2} Main contrast control relative characteristics2

Measuring condition and procedure are the same as described in ΔV_{C1}.

V_{C3} Main contrast control characteristics3

Measuring condition and procedure are the same as described in V_{C1}.

ΔV_{C3} Main contrast control relative characteristics3

Measuring condition and procedure are the same as described in ΔV_{C1}.

V_{SC1} Sub contrast control characteristics1

Measur the amplitude output at OUT (29, 32, 35). The measured value is called VOUT (29, 32, 35). Sub contrast control characteristics V_{SC1} is calculated by the equation below:

$$V_{SC1}=20\text{Log}\frac{VOUT}{0.7}\ \text{(dB)}$$

ΔV_{SC1} Sub contrast control relative characteristics1

Relative characteristics ΔV_{SC1} is calculated by the equation below:

$\Delta V_{SC1}=$ VOUT (29)/VOUT (32),
VOUT (32)/VOUT (35),
VOUT (35)/VOUT (29).

V_{SC2} Sub contrast control characteristics2

Measuring condition and procedure are the same as described in V_{SC1}.

ΔV_{SC2} Sub contrast control relative characteristics2

Measuring condition and procedure are the same as described in ΔV_{SC1}.

V_{SC3} Sub contrast control characteristics3

Measuring condition and procedure are the same as described in V_{SC1}.

ΔV_{SC3} Sub contrast control relative characteristics3

Measuring condition and procedure are the same as described in ΔV_{SC1}.

VMSC Main/sub contrast control characteristics2

Measure the amplitude output at OUT (29, 32, 35). The measured value is called VOUT (29, 32, 35). Main/Sub contrast control characteristics VMSC1 is calculated by the equation below:

$$VMSC1=20\text{Log}\frac{VOUT}{0.7}\ \text{(dB)}$$

ΔVMSC Main/sub contrast control relative characteristics2

Relative characteristics ΔVMSC1 is calculated by the equation below:

$\Delta VMSC=$ VOUT (29)/VOUT (32),
VOUT (32)/VOUT (35),
VOUT (35)/VOUT (29)

ABL1 ABL control characteristics1

Measure the amplitude output at OUT (29, 32, 35). The measured value is called VOUT (29, 32, 35), and is ttreated as ABL1.

ΔABL1 ABL control relative characteristics1

Relative characteristics ΔABL1 is calculated by the equation below:

$\Delta ABL1=$ VOUT (29)/VOUT (32),
VOUT (32)/VOUT (35),
VOUT (35)/VOUT (29)

ABL2 ABL control characteristics2

Measuring condition and procedure are the same as described in ABL1.

ΔABL2 ABL control relative characteristics2

Measuring condition and procedure are the same as described in ΔABL1.

V_{B1} Brightness control characteristics1

Measure the DC voltage at OUT (29, 32, 35) with a voltmeter. The measured value is called VOUT (29, 32, 35), and is ttreated as V_{B1}.

ΔV_{B1} Brightness control relative characteristics1

Relative characteristics ΔV_{B1} is calculated by the difference in the output between the channels.

$\Delta V_{B1}=$ VOUT (29)-VOUT (32),
VOUT (32)-VOUT (35),
VOUT (35)-VOUT (29)

V_{B2} Brightness control characteristics2

Measuring condition and procedure are the same as described in V_{B1}.

ΔV_{B2} Brightness control relative characteristics2

Measuring condition and procedure are the same as described in ΔV_{B1}.

V_{B3} Brightness control characteristics3

Measuring condition and procedure are the same as described in V_{B1}.

ΔV_{B3} Brightness control relative characteristics3

Measuring condition and procedure are the same as described in ΔV_{B1}.

F_{C1} Frequency characteristics1 (f=50MHz)

First, SG3 to 1MHz is as input signal. Input a resister that is about 2kΩ to offer the voltage at input pins (2, 6, 11) in order that the bottom of input signal is 2.5V. Control the main contrast in order that the amplitude of sine wave output is 4.0$V_{P\text{-}P}$. Control the brightness in order that the bottom of sine wave output is 2.0$V_{P\text{-}P}$. By the same way, measure the output amplitude when SG3 to 50MHz is as input signal. The measured value is called VOUT (29, 32, 35). Frequency characteristics F_{C1} (29, 32, 35) is calculated by the equation below:

$$F_{C1}=20\text{Log}\frac{VOUT\ V_{P\text{-}P}}{\text{Output amplitude when inputed SG3 (1MHz):4}V_{P\text{-}P}}\ \text{(dB)}$$

ΔF_{C1} Frequency relative characteristics1 (f=50MHz)

Relative characteristics ΔF_{C1} is calculated by the difference in the output between the channels.

F_{C1}' Frequency characteristics1 (f=150MHz)

Measuring condition and procedure are the same as described in F_{C1}, expect SG3 to 150MHz.

ΔF_{C1}' Frequency relative characteristics1 (f=150MHz)

Relative characteristics ΔF_{C1}' is calculated by the difference in the output between the channels.

F_{C2} Frequency characteristics2 (f=150MHz)

SG3 to 1MHz is as input signal. Control the main contrast in order that the amplitude of sine wave output is 1.0V_{P-P}. By the same way, measure the output amplitude when SG3 to 150MHz is as input signal.

The measured value is called VOUT (29, 32, 35). Frequency characteristics F_{C2} (29, 32, 35) is calculated by the equation below:

$$F_{C1}=20\text{Log}\frac{\text{VOUT } V_{P-P}}{\text{Output amplitude when inputed SG3 (1MHz):4}V_{P-P}}\text{(dB)}$$

ΔF_{C2} Frequency relative characteristics2 (f=150MHz)

Relative characteristics ΔF_{C2} is calculated by the difference in the output between the channels.

C.T.1 Crosstalk1 (f=50MHz)

Input SG3 (50MHz) to pin2 only, and then measure the waveform amplitude output at OUT (29, 32, 35). The measured value is called VOUT (29, 32, 35). Crosstalk C.T.1 is calculated by the equation below:

$$\text{C.T.1}=20\text{Log}\frac{\text{VOUT (29, 32)}}{\text{VOUT (35)}}\text{ (dB)}$$

C.T.1' Crosstalk1 (f=150MHz)

Measuring condition and procedure are the same as described in C.T.1, expect SG3 to 150MHz.

C.T.2 Crosstalk2 (f=50MHz)

Input SG3 (50MHz) to pin6 only, and then measure the waveform amplitude output at OUT (29, 32, 35). The measured value is called VOUT (29, 32, 35). Crosstalk C.T.2 is calculated by the equation below:

$$\text{C.T.2}=20\text{Log}\frac{\text{VOUT (29, 35)}}{\text{VOUT (32)}}\text{ (dB)}$$

C.T.2' Crosstalk2 (f=150MHz)

Measuring condition and procedure are the same as described in C.T.2, expect SG3 to 150MHz.

C.T.3 Crosstalk3 (f=50MHz)

Input SG3 (50MHz) to pin11 only, and then measure the waveform amplitude output at OUT (29, 32, 35). The measured value is called VOUT (29, 32, 35). Crosstalk C.T.2 is calculated by the equation below:

$$\text{C.T.3}=20\text{Log}\frac{\text{VOUT (32, 35)}}{\text{VOUT (29)}}\text{ (dB)}$$

C.T.3' Crosstalk3 (f=150MHz)

Measuring condition and procedure are the same as described in C.T.3, expect SG3 to 150MHz.

Tr Pulse characteristics1 (4V_{P-P})

Control the main contrast (00H) in order that the amplitude of output signal is 4.0V_{P-P}.

Control the brightness (V30) in order that the Black level of output signal is 2.0V.

Measure the time needed for the input pulse to rise from 10% to 90 % (Tr1) and for the output pulse to rise from 10% to 90% (Tr2) with an active prove.

Pulse characteristics TR is calculated by the equations below:

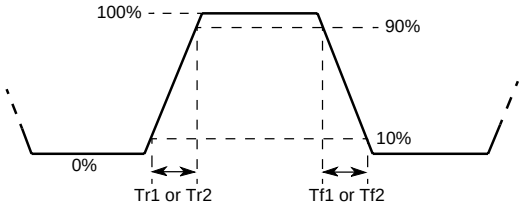
$$TR=\sqrt{[(Tr2)^2-(Tr1)^2]}\text{ (nsec)}$$

Tf Pulse characteristics2 (4V_{P-P})

Measure the time needed for the input pulseto fall from 90% to 10% (Tf1) and for the output pulse to fall from 90% to 10% (Tf2) with an active prove.

Pulse characteristics TF is calculated by the equations below:

$$TR=\sqrt{[(Tf2)^2-(Tf1)^2]}\text{ (nsec)}$$



VthCP Clamp pulse threshold voltage

Turn down the SG5 input level gradually from 5.0V_{P-P}, monitoring the waveform output.

Measure the top level of input pulse when the output pedestal voltage turn decrease with unstable.

WCP Clamp pulse minimum width

Decrease the SG5 pulse width gradually from 0.5μs, monitoring the output. Measure the SG5 pulse width (a point of 1.5V) when the output pedestal voltage turn decrease with unstable.

P_{DCH} Pedestal voltage temperature characteristics1
Measure the pedestal voltage at 25°C. The measured value is called PDC1.
Measure the pedestal voltage at temperature of -20°C.
The measured value is called PDC2.
Pedestal voltage temperature characteristics 1 is calculated by the equation below:

$$P_{DCH}=PDC1-PDC2$$

P_{DCL} Pedestal voltage temperature characteristics2
Measure the pedestal voltage at 25°C. The measured value is called PDC1.
Measure the pedestal voltage at temperature of 75°C.
The measured value is called PDC3.
Pedestal voltage temperature characteristics 2 is calculated by the equation below:

$$P_{DCL}=PDC1-PDC3$$

OTr OSD pulse characteristics1
Measure the time needed for the output pulse to rise from 10% to 90% (OTR) with an active prove.

OTf OSD pulse characteristics2
Measure the time needed for the output pulse to fall from 90% to 10% (OTF) with an active prove.

Oaj1 OSD adjust control characteristics1
Measure the amplitude output at OUT (29, 32, 35). The measured value is called VOUT (29,32,35), and is treated as Oaj1.

ΔOaj1 OSD adjust control relative characteristics1
Relative characteristics ΔOaj1 is calculated by the equation below:

ΔOaj1= VOUT (29)/VOUT (32),
VOUT (32)/VOUT (35),
VOUT (35)/VOUT (29)

Oaj2 OSD adjust control characteristics2
Measuring condition and procedure are the same as described in Oaj1.

ΔOaj2 OSD adjust control relative characteristics2
Measuring condition and procedure are the same as described in ΔOaj1.

Oaj3 OSD adjust control characteristics3
Measuring condition and procedure are the same as described in Oaj1.

ΔOaj3 OSD adjust control relative characteristics3
Measuring condition and procedure are the same as described in ΔOaj1.

VthOSD OSD input threshold voltage
Reduce the SG6 input level gradually, monitoring output. Measure the SG6 level when the output reaches 0V. The measured value is called VthOSD.

VthBLK OSD BLK input threshold voltage
Confirm that output signal is being blanked by the SG6 at the time. Monitoring to output signal, decreasing the level of SG6. Measure the top level of SG6 when the blanking period is disappeared. The measured value is called VthBLK.

HBLK1 Retrace BLK characteristics1
Measure the amplitude output is blanked by the SG7 at OUT (29, 32, 35). The measured value is called VOUT (29, 32, 35), and is treated as HBLK1.

HBLK2 Retrace BLK characteristics2
Measure the amplitude output is blanked by the SG7 at OUT (29, 32, 35). The measured value is called VOUT (29, 32, 35), and is treated as HBLK2.

HBLK3 Retrace BLK characteristics3
Measure the amplitude output is blanked by the SG7 at OUT (29, 32, 35). The measured value is called VOUT (29, 32, 35), and is treated as HBLK3.

VthRET Retrace BLK input threshold voltage
Confirm that output signal is being blanked by the SG7 at the time. Monitoring to output signal, decreasing the level of SG7. Measure the top level of SG7 when the blanking period is disappeared. The measured value is called VthRET.

SS-NV SOG input maximum noize voltage
The sync's amplitude of SG4 be changed all white into all black, increase from 0V_{P-P} to 0.02V_{P-P}. No pulse output permitted.

SS-SV SOG minimum input voltage
The sync's amplitude of SG4 be changed all white or all black, decrease from 0.3V_{P-P} to 0.2V_{P-P}. Confirm no malfunction produced by noise.

VSH Sync output hi level
Measure the high voltage at SyncOUT. The measured value is treated as VSH.

VSL Sync output lo level
Measure the low voltage at SyncOUT. The measured value is treated as VSL.

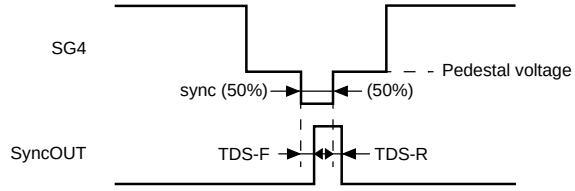
TDS-F Sync output delay time1

SyncOUT becomes High with sync part of SG4.

Measure the time needed for the front edge of SG4 sync to fall from 50% and for SyncOUT to rise from 50% with an active prove. The measured value is treated as TDS-F, less than 90nsec.

TDS-R Sync output delay time2

Measure the time needed for the rear edge of SG4 sync to rise from 50% and for SyncOUT to fall from 50% with an active prove. The measured value is treated as TDS-R, less than 90nsec.



VOH D/A H output voltage

Measure the DC voltage at D/AOUT. The measured value is ttreated as VOH.

VOL D/A L output voltage

Measure the DC voltage at D/AOUT. The measured value is ttreated as VOL.

IAO D/A output current range

Electric current flow from the output of D/AOUT must be less than 1.0mA.

Electric current flow in the output of D/AOUT must be less than 0.4mA.

DNL D/A nonlinearity

The difference of differential non-linearity of D/AOUT must be less than ±1.0LSB.

BUS CONTROL TABLE

(1) Slave address

D7	D6	D5	D4	D3	D2	D1	R/W	
1	0	0	0	1	0	0	0	=88H

(2) Each function's sub address

Function	bit	sub add.	Data byte (up:bit information down: preset)							
			D7	D6	D5	D4	D3	D2	D1	D0
Main contrast	8	00H	A07	A06	A05	A04	A03	A02	A01	A00
			0	1	0	0	0	0	0	0
Sub contrast R	8	01H	A17	A16	A15	A14	A13	A12	A11	A10
			1	0	0	0	0	0	0	0
Sub contrast G	8	02H	A27	A26	A25	A24	A23	A22	A21	A20
			1	0	0	0	0	0	0	0
Sub contrast B	8	03H	A37	A36	A35	A34	A33	A32	A31	A30
			1	0	0	0	0	0	0	0
OSD level	4	04H	–	–	–	–	A43	A42	A41	A40
			0	0	0	0	1	0	0	0
RE-BLK adjust	4	05H	–	–	–	–	A53	A52	A51	A50
			0	0	0	0	1	0	0	0
D/A OUT1	8	06H	A67	A66	A65	A64	A63	A62	A61	A60
			1	0	0	0	0	0	0	0
D/A OUT2	8	07H	A77	A76	A75	A74	A73	A72	A71	A70
			1	0	0	0	0	0	0	0
D/A OUT3	8	08H	A87	A86	A85	A84	A83	A82	A81	A80
			1	0	0	0	0	0	0	0
D/A OUT4	8	09H	A97	A96	A95	A94	A93	A92	A91	A90
			1	0	0	0	0	0	0	0
Pedestal clamp INT/EXT SW	1	0BH	–	–	–	–	–	–	–	AB0
			0	0	0	0	0	0	0	0

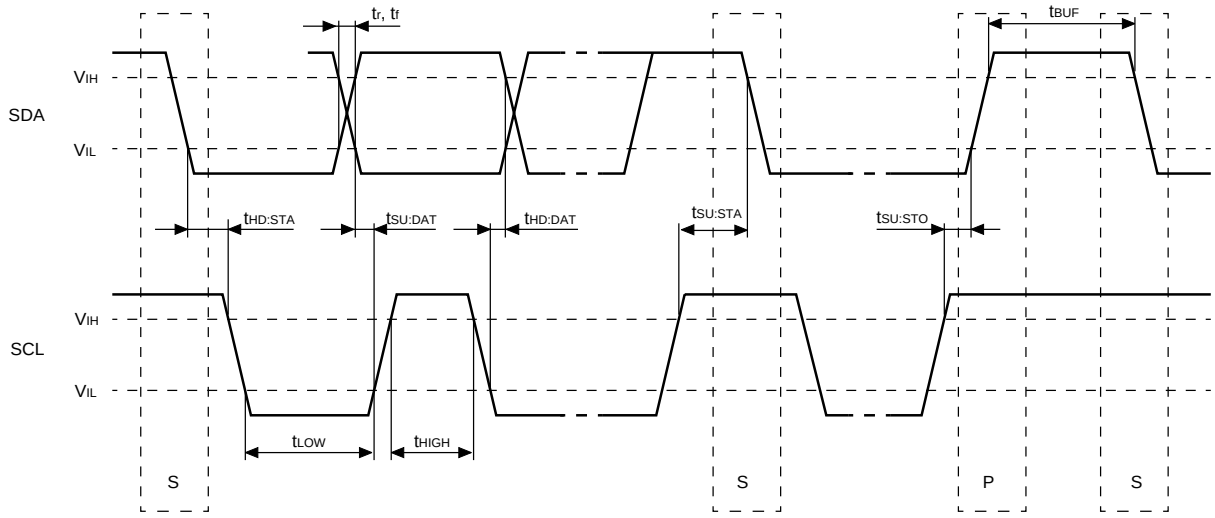
Notes) pedestal level INT/EXT SW

0→INT 1→EXT

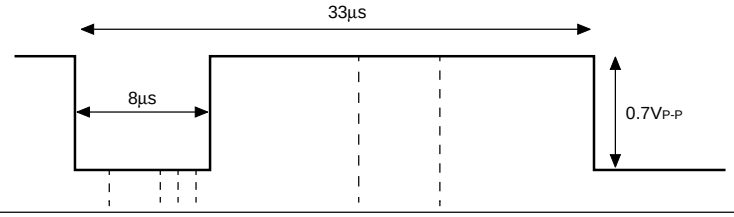
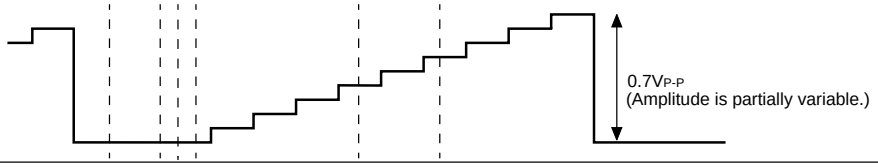
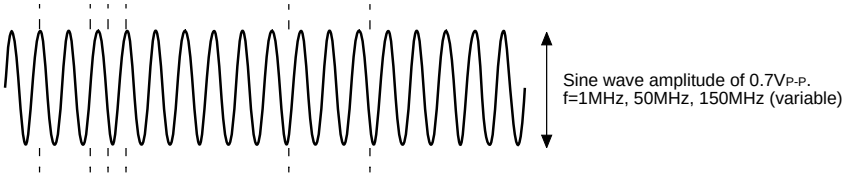
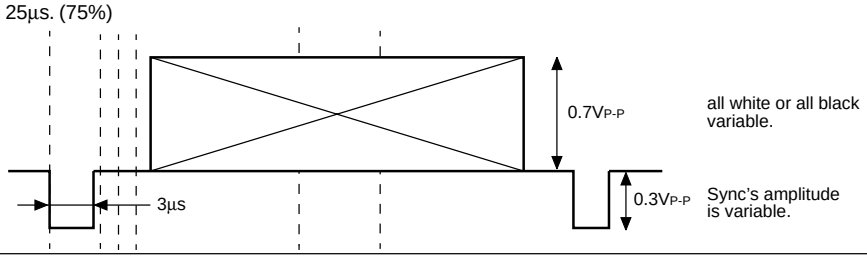
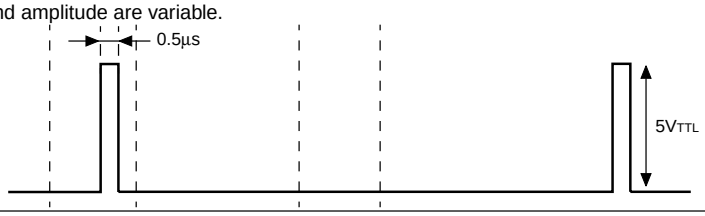
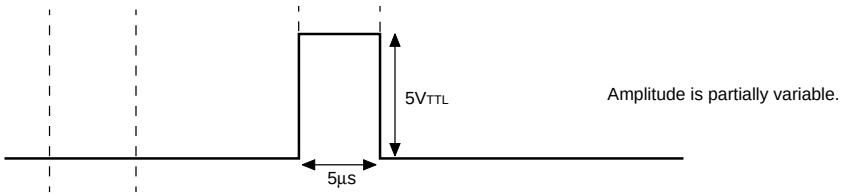
I²C BUS CONTROL SECTION SDA, SCL CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Unit
V_{IL}	min. input LOW voltage	-0.5	1.5	V
V_{IH}	max. input HIGH voltage	3.0	5.5	V
f_{SCL}	SCL clock frequency	0	100	kHz
t_{BUF}	Time the bus must be free before a new transmission can start	4.7	–	µs
$t_{HD:STA}$	Hold time start condition. After this period the first clock pulse is generated	4.0	–	µs
t_{LOW}	The LOW period of the clock	4.7	–	µs
t_{HIGH}	The HIGH period of the clock	4.0	–	µs
$t_{SU:STA}$	Set up time for start condition (Only relevant for a repeated start condition)	4.7	–	µs
$t_{HD:DAT}$	Hold time DATA	0	–	µs
$t_{SU:DAT}$	Set-up time DATA	250	–	ns
t_r	Rise time of both SDA and SCL lines	–	1000	ns
t_f	Fall time of both SDA and SCL lines	–	300	ns
$t_{SU:STO}$	Set-up time for stop condition	4.0	–	µs

TIMING DIAGRAM

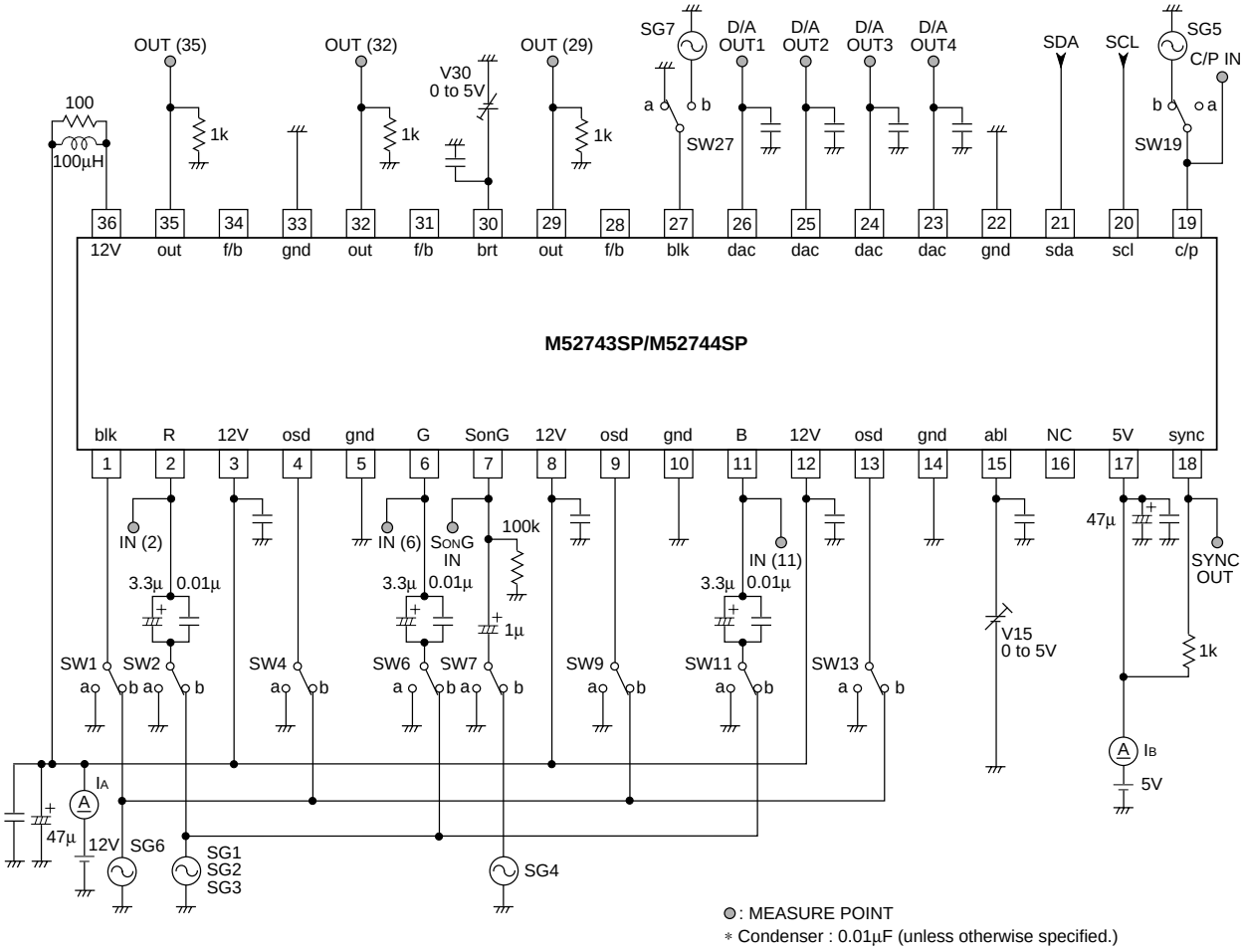


INPUT SIGNAL

SG No.	Signals
SG1 Video signal (all white)	Pulse with amplitude of 0.7V_{P-P} (f=30kHz). Video width of 25µs. (75%) 
SG2 Video signal (step wave)	
SG3 Sine wave (for freq. char.)	
SG4 Video signal (all white, all black)	Video width of 25µs. (75%) 
SG5 Clamp pulse	Pulse width and amplitude are variable. 
SG6 OSD pulse	
SG7 BLK pulse	

∗) f=30kHz

TEST CIRCUIT



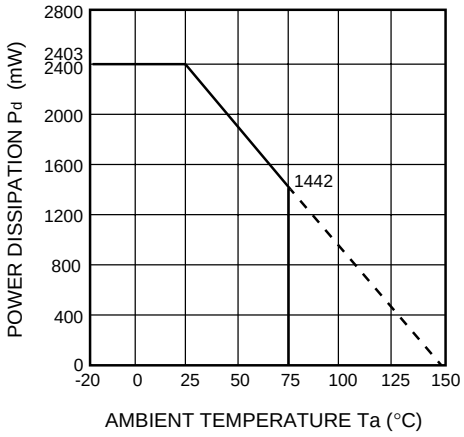
● : MEASURE POINT

∗ Condenser : 0.01µF (unless otherwise specified.)

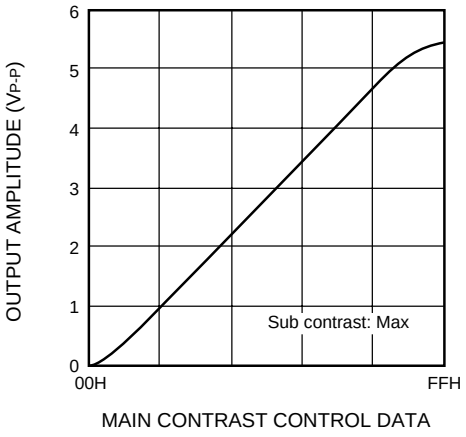
Units Resistance : Ω
Capacitance : F

TYPICAL CHARACTERISTICS

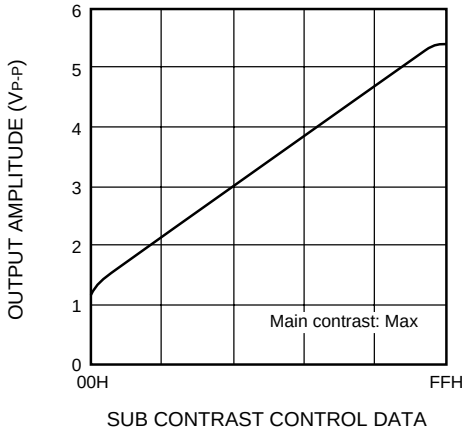
THERMAL DERATING



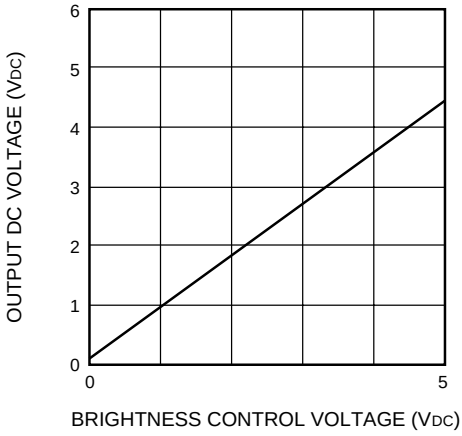
MAIN CONTRAST CONTROL CHARACTERISTICS



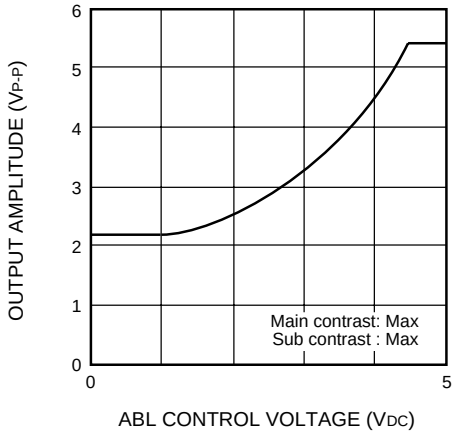
SUB CONTRAST CONTROL CHARACTERISTICS



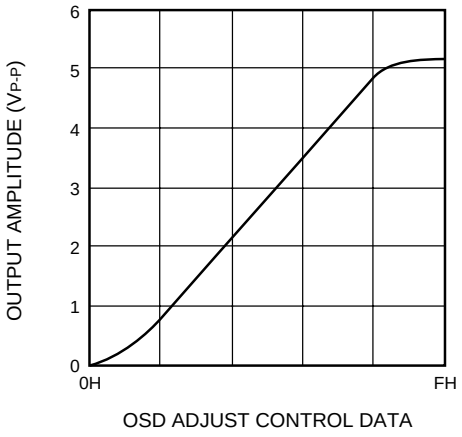
BRIGHTNESS CONTROL CHARACTERISTICS



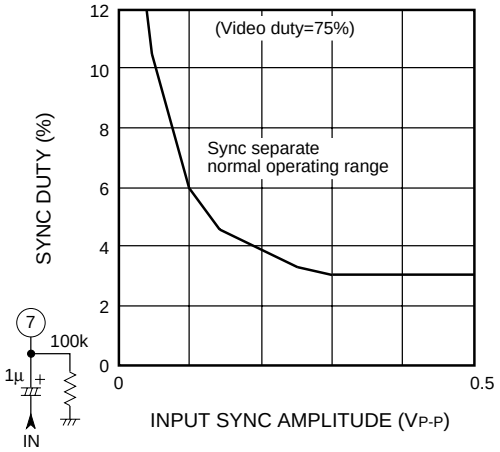
ABL CHARACTERISTICS



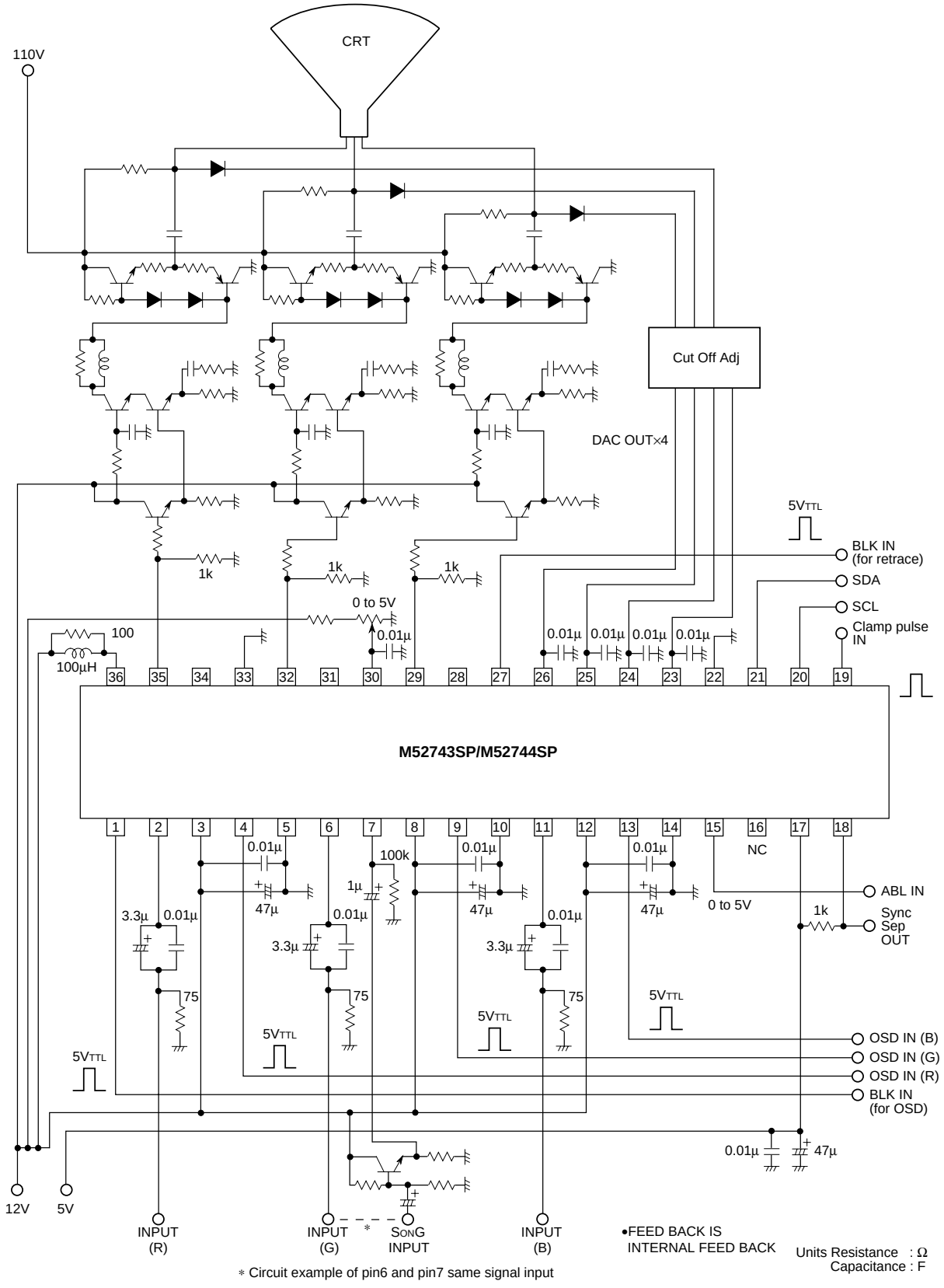
OSD ADJUST CONTROL CHARACTERISTICS



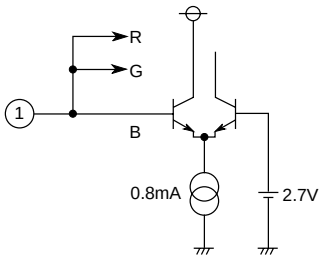
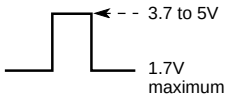
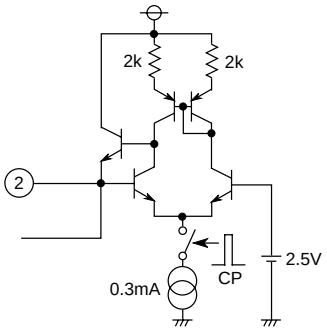
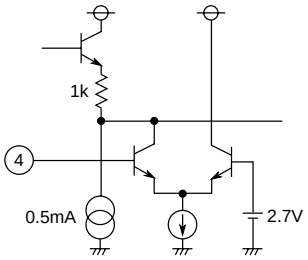
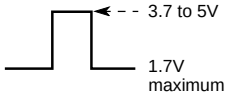
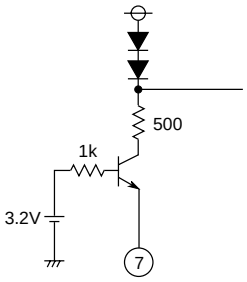
SYNC ON GREEN INPUT MIN. PULSE WIDTH



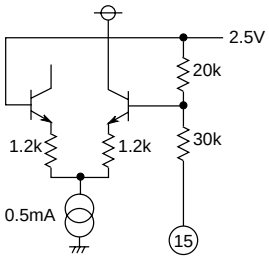
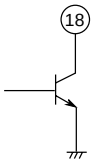
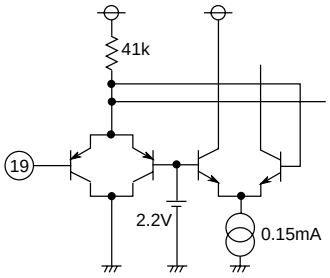
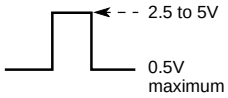
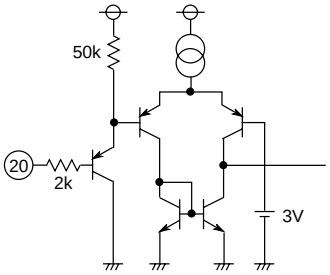
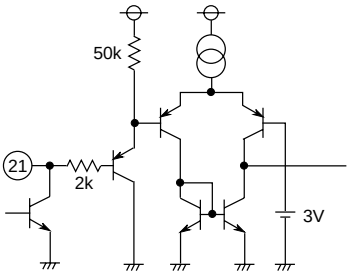
APPLICATION EXAMPLE



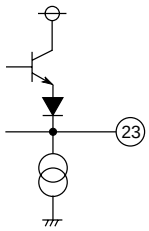
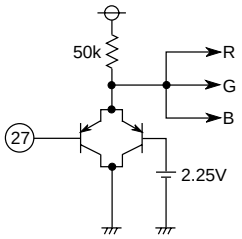
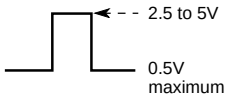
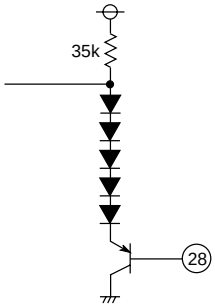
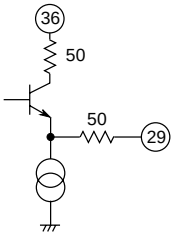
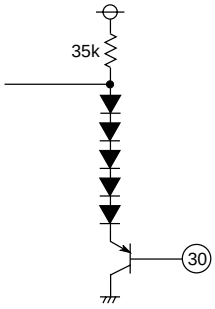
DESCRIPTION OF PIN

Pin No.	Name	DC voltage (V)	Peripheral circuit of pins	Description of function
1	OSD BLK IN	–		·Input pulses  ·Connected to GND if not used.
2 6 11	INPUT (R) INPUT (G) INPUT (R)	2.5		·Clamped to about 2.5V due to clamp pulses from pin 19. ·Input at low impedance.
3 8 12	V_{CC1} (R) V_{CC1} (G) V_{CC1} (B)	12	–	·Apply equivalent voltage to 3 channels.
4 9 13	OSD IN (R) OSD IN (G) OSD IN (B)	–		·Input pulses  ·Connected to GND if not used.
5 10 14 22 33	GND 1 (R) GND 1 (G) GND 1 (B) GND (5V) GND 2	GND	–	
7	INPUT (S on G)	When open≈2.5V		·SYNC ON GREEN input pin for sync separation. Sync is negative. input signal at Pin7, compare with the reference voltage of internal circuit in order to separate sync signal. ·When not used, set to OPEN.

DESCRIPTION OF PIN (cont.)

Pin No.	Name	DC voltage (V)	Peripheral circuit of pins	Description of function
15	ABL IN	When open 2.5V		·ABL (Automatic Beam Limitter) input pin. Recommended voltage range is 0 to 5V. When ABL function is not used, set to 5V.
16	NC	–	–	
17	Vcc (5V)	5	–	
18	S on G Sep OUT	–		·Sync signal output pin, Being of open collector output type.
19	Clamp Pulse IN	–		·Input pulses  ·Input at low impedance.
20	SCL	–		·SCL of I²C BUS (Serial clock line) VTH=2.3V
21	SDA	–		·SDA of I²C BUS (Serial data line) VTH=2.3V

DESCRIPTION OF PIN (cont.)

Pin No.	Name	DC voltage (V)	Peripheral circuit of pins	Description of function
23 24 25 26	D/A OUT	–		·D/A output pin. Output voltage range is 0 to 5V, Max output current is 0.4mA.
27	Retrace BLK IN	–		·Input pulses  ·Connected to GND if not used.
28 31 34	EXT Feed Back (B) EXT Feed Back (G) EXT Feed Back (R)	Variable		–
29 32 35	OUTPUT (B) OUTPUT (G) OUTPUT (R)	Variable		·A resistor is needed on the GND side. Set discretionally to maximum 15mA, depending on the required driving capacity.
36	V_{CC2}	12 Impressed		·Used to supply power to output emitter follower only.
30	Main Brightness	–		·It is recommended that the IC be used between pedestal voltage 2V and 3V.

APPLICATION METHOD FOR M52743SP

CLAMP PULSE INPUT

Clamp pulse width is recommended

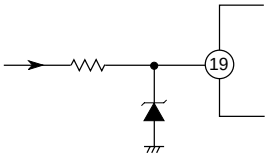
above 15kHz, 1.0µsec

above 30kHz, 0.5µsec

above 64kHz, 0.3µsec.

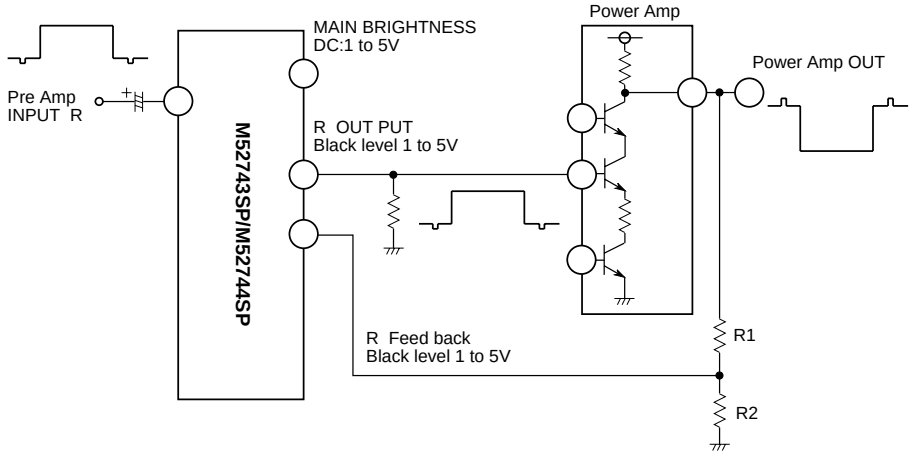
The clamp pulse circuit in ordinary set is a long round about way, and beside high voltage, sometimes connected to external terminal, it is very easy affected by large surge.

Therefore, the Fig. shown right is recommended.



EXT-FEED BACK

In case of application circuit example of lower figure, Set up R1, R2 which seems that the black level of the signal feedbacked from Power AMP is 1V, when the bottom of output signal is 1V.



EXT-FEED BACK APPLICATION CIRCUIT

NOTICE OF APPLICATION

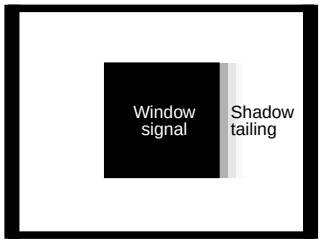
· Make the nearest distance between output pin and pull down resister.

· Recommended pedestal voltage of IC output signal is 2V.

TAILING

There is the case that a screen tailing like a figure by characteristic of the next stage amplifier connected to M52744SP.

That case recommends use of M52743SP.



SCREEN