ASYNCHRONOUS SRAM

32K x 8 SRAM

+5V SUPPLY, SINGLE CHIP ENABLE
TRADITIONAL PINOUT

FEATURES

- Fast access times: 8, 10, and 12ns
- Fast OE# access times: 5 and 6ns
- Single +5V ±10% power supply
- Fully static -- no clock or timing strobes necessary
- All inputs and outputs are TTL-compatible
- Three state outputs
- High-performance, low-power consumption, CMOS double-poly, double-metal process

OPTIONS — MARKING

- Timing
  - 8ns access — -8
  - 10ns access — -10
  - 12ns access — -12
- Packages
  - 28-pin SOJ (300 mil) — SJ
  - 28-pin TSOP — TS
- Power consumption
  - Standard — None
  - Low — L
- Temperature
  - Commercial — None — (0°C to 70°C)
  - Industrial — I — (-40°C to 85°C)

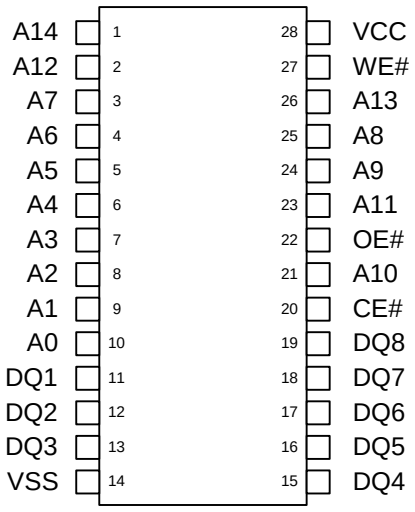
GENERAL DESCRIPTION

The GVT7232A8 is organized as a 32,768 x 8 SRAM using a four-transistor memory cell with a high performance, silicon gate, low-power CMOS process. Galvantech SRAMs are fabricated using double-layer polysilicon, double-layer metal technology.

Static design eliminates the need for external clocks or timing strobes. For increased system flexibility and eliminating bus contention problems, this device offers one chip enable (CE#) along with output enable (OE#) for this organization.

The chip is enabled when CE# is LOW. With chip being enabled, writing to this device is accomplished when write enable (WE#) is LOW and reading is accomplished when (OE#) go LOW with (WE#) remaining HIGH. The device offers a low power standby mode when chip is not selected. This allows system designers to meet low standby power requirements.

PIN ASSIGNMENT
28-Pin SOJ
28-Pin TSOP



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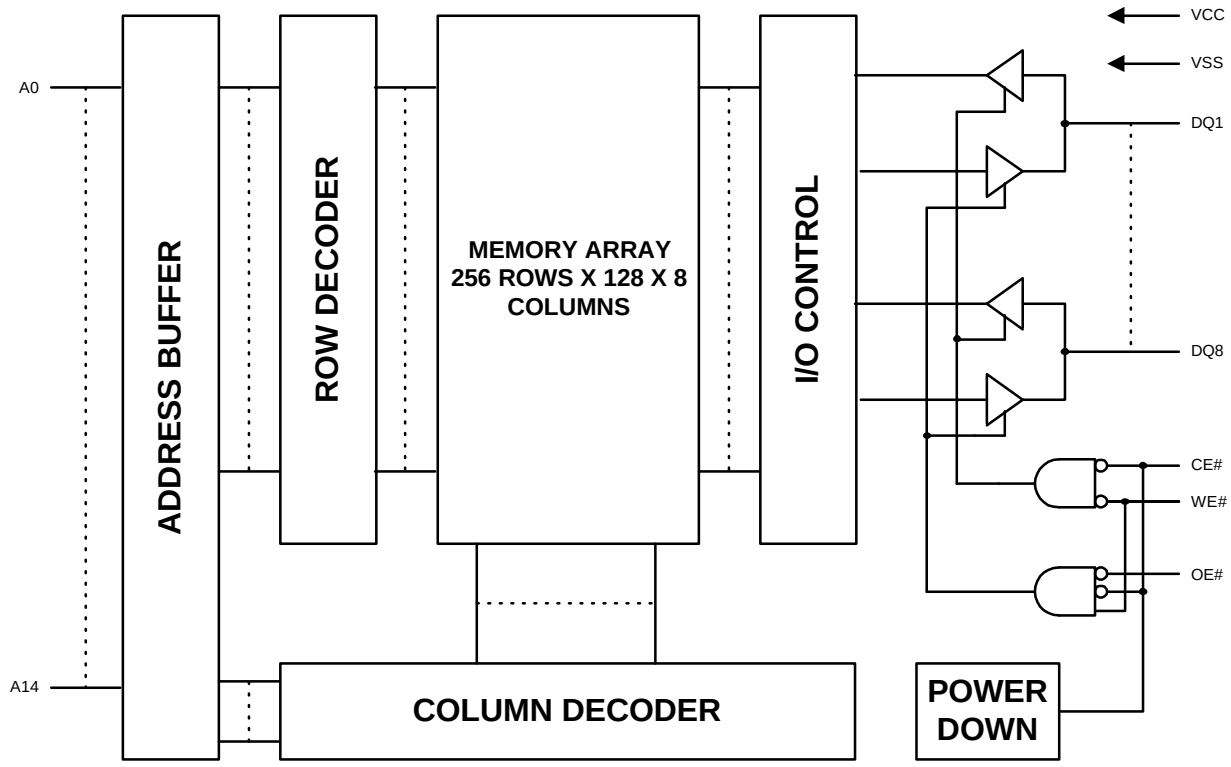
Rev. 2/98

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	CE#	WE#	OE#	DQ	POWER
READ	L	H	L	Q	ACTIVE
WRITE	L	L	X	D	ACTIVE
OUTPUT DISABLE	L	H	H	HIGH-Z	ACTIVE
STANDBY	H	X	X	HIGH-Z	STANDBY

PIN DESCRIPTIONS

Pin Numbers	SYMBOL	TYPE	DESCRIPTION
10, 9, 8, 7, 6, 5, 4, 3, 25, 24, 21, 23, 2, 26, 1	A0-A14	Input	Addresses Inputs: These inputs determine which cell is addressed.
27	WE#	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. WE# is LOW for a WRITE cycle and HIGH for a READ cycle.
20	CE#	Input	Chip Enable: This input is used to enable the device. When CE# is LOW, the chip is selected. When either CE# is HIGH, the chip is disabled and automatically goes into standby power mode.
22	OE#	Input	Output Enable: This active LOW input enables the output drivers.
11, 12, 13, 15, 16, 17, 18, 19	DQ1-DQ8	Input/ Output	SRAM Data I/O: Data inputs and data outputs
28	VCC	Supply	Power Supply: 5V ±10%
14	VSS	Supply	Ground

ABSOLUTE MAXIMUM RATINGS*

Voltage on VCC Supply Relative to VSS.....-0.5V to +7.0V
V_{IN} .....-0.5V to VCC+0.5V
Storage Temperature (plastic) .....-55°C to +125°
Junction Temperature .....+125°
Power Dissipation 1.2W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(All Temperature Ranges; VCC = 5V ±10% unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) voltage		V_{IH}	2.2	VCC+1	V	1, 2
Input Low (Logic 0) Voltage		V_{II}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ VCC	IL_I	-5	5	uA	
Output Leakage Current	Output(s) disabled, 0V ≤ V_{OUT} ≤ VCC	IL_O	-5	5	uA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		VCC	4.5	5.5	V	1

DESCRIPTION	CONDITIONS	SYM	TYP	POWER	-8*	-10	-12	UNITS	NOTES
Power Supply Current: Operating	Device selected; CE# ≤ V_{IL}; VCC =MAX; f=f_{MAX}; outputs open	Icc	60	standard	170	145	125	mA	3, 14
				low	160	135	115		
TTL Standby	CE# ≥V_{IH}; VCC = MAX; f=f_{MAX}	I_{SB1}	20	standard	45	41	37	mA	14
				low	40	36	32		
CMOS Standby	CE# ≥VCC -0.2; VCC = MAX; all other inputs ≤ VSS +0.2 or ≥VCC -0.2; all inputs static; f= 0	I_{SB2}	0.75	standard	5	5	5	mA	14
				low	5	5	5		

*NOTE: VCC = 5V ± 5% for this speed grade.

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz VCC = 5V	C_I	6	pF	4
Input/Output Capacitance (DQ)		$C_{I/O}$	8	pF	4

AC ELECTRICAL CHARACTERISTICS

(Note 5) (All Temperature Ranges; VCC = 5V ±10%)

DESCRIPTION		- 8*		- 10		- 12			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle									
READ cycle time	^tRC	8		10		12		ns	
Address access time	^tAA		8		10		12	ns	
Chip Enable access time	^tACE		8		10		12	ns	
Output hold from address change	^tOH	2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		3		ns	4, 7
Chip disable to output in High-Z	^tHZCE		5		5		6	ns	4, 6, 7
Output Enable access time	^tAOE		5		5		6	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		ns	
Output Enable to output in High-Z	^tHZOE		5		5		6	ns	4, 6
Chip Enable to power-up time	^tPU	0		0		0		ns	4
Chip disable to power-down time	^tPD		8		10		12	ns	4
WRITE Cycle									
WRITE cycle time	^tWC	8		10		12		ns	
Chip Enable to end of write	^tCW	6		7		8		ns	
Address valid to end of write, with OE# HIGH	^tAW	6		7		8		ns	
Address setup time	^tAS	0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		ns	
WRITE pulse width	$^tWP2$	8		10		10		ns	
WRITE pulse width, with OE# HIGH	$^tWP1$	6		7		8		ns	
Data setup time	^tDS	5		5		6		ns	
Data hold time	^tDH	0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		3		ns	4, 7
Write Enable to output in High-Z	^tHZWE		5		5		6	ns	4, 6, 7

*NOTE: VCC = 5V ± 5% for this speed grade.

AC TEST CONDITIONS

Input pulse levels	0V to 3.0V
Input rise and fall times	1.5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

OUTPUT LOADS

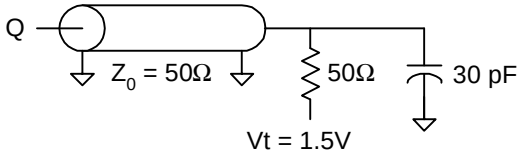


Fig. 1 OUTPUT LOAD EQUIVALENT

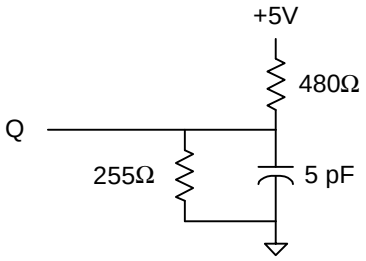
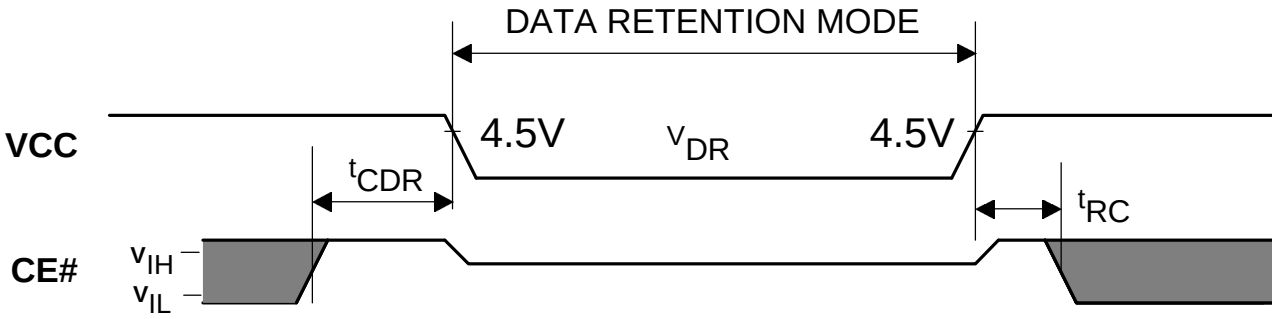


Fig. 2 OUTPUT LOAD EQUIVALENT

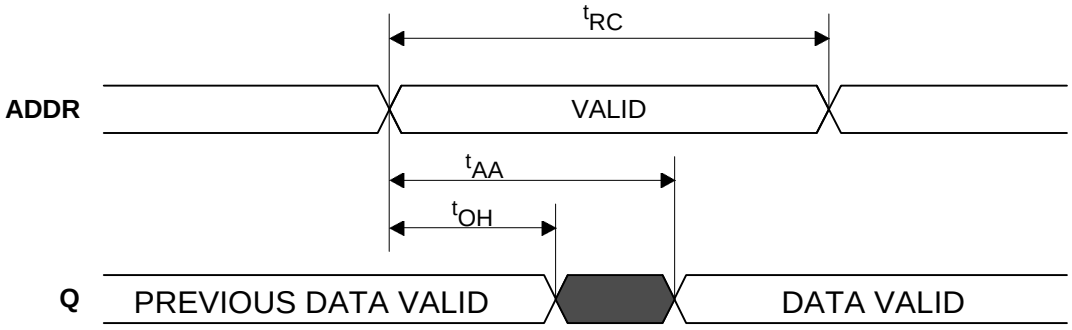
NOTES

1. All voltages referenced to VSS (GND).
2. Overshoot: $V_{IH} \leq +7.0V$ for $t \leq {}^tRC/2$.
   Undershoot: $V_{IL} \leq -2.0V$ for $t \leq {}^tRC/2$
3. I_{cc} is given with no output current. I_{cc} increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with C_L=5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$ and ${}^tHZWE$ is less than ${}^tLZWE$.
8. WE# is HIGH for READ cycle.
9. Device is continuously selected. Chip enable and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. t_{RC} = Read Cycle Time.
12. Chip Enable and Write Enable can initiate and terminate a WRITE cycle.
13. Capacitance derating applies to capacitance different from the load capacitance shown in Fig. 1.
14. Typical values are measured at 5V, 25°C and 20ns cycle time.

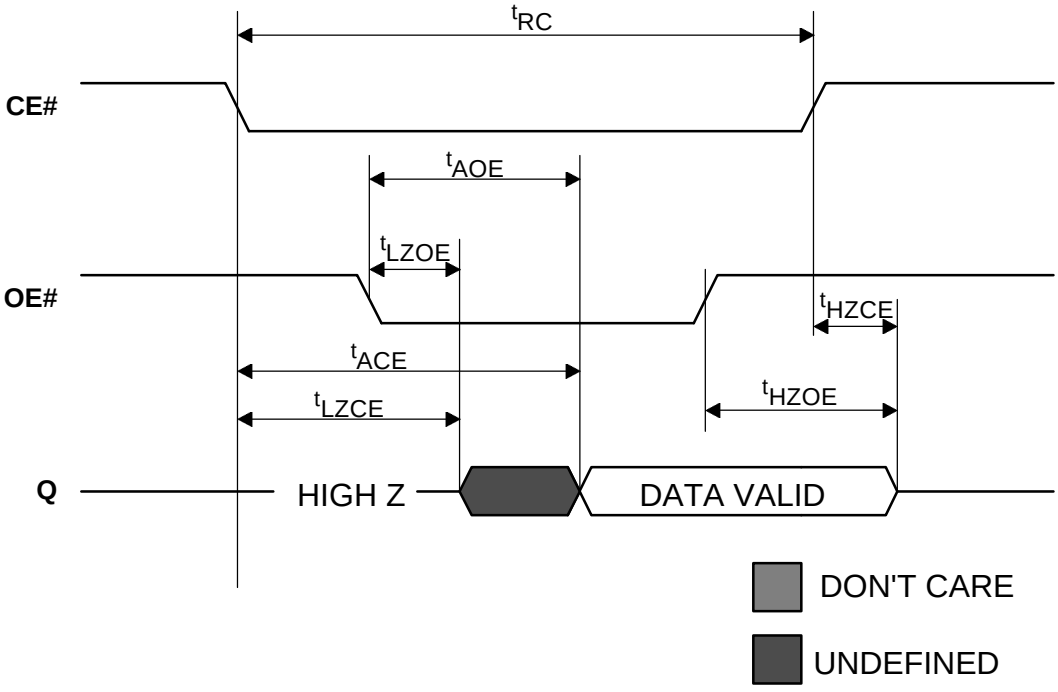
LOW VCC DATA RETENTION WAVEFORM



READ CYCLE NO. 1(8, 9)

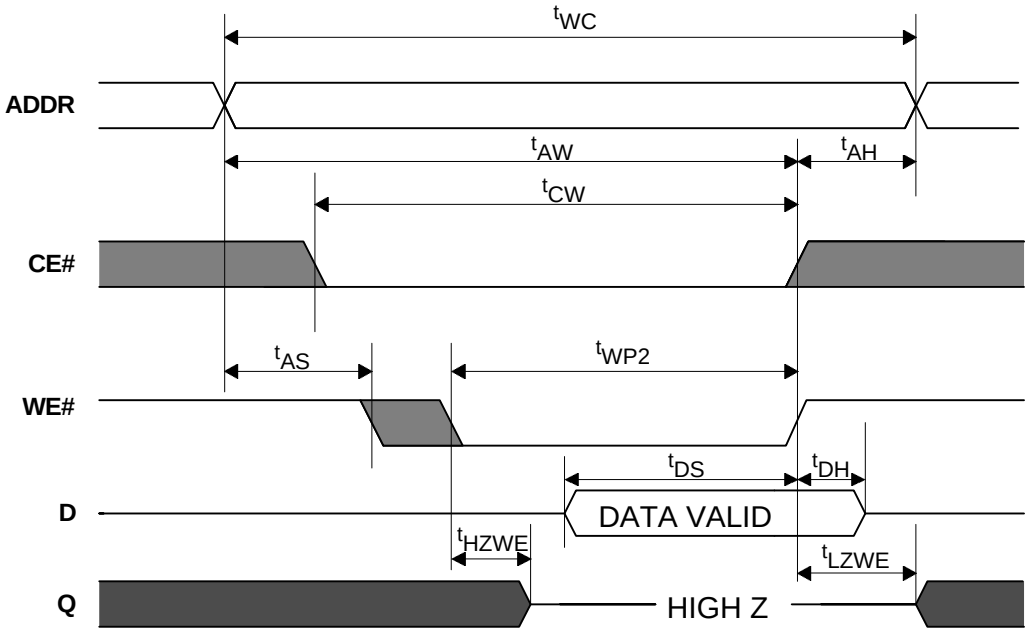


READ CYCLE NO. 2(7, 8, 10, 12)



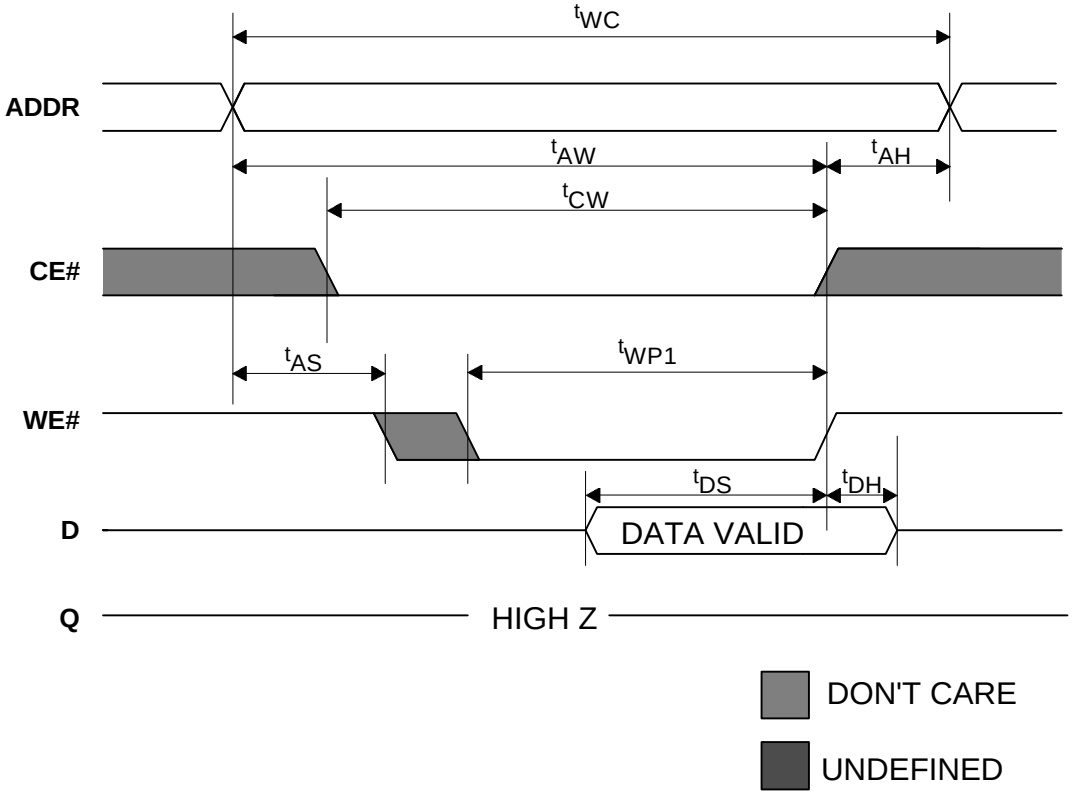
WRITE CYCLE NO. 1(7, 12, 13)

(Write Enable Controlled with Output Enable OE# active LOW))

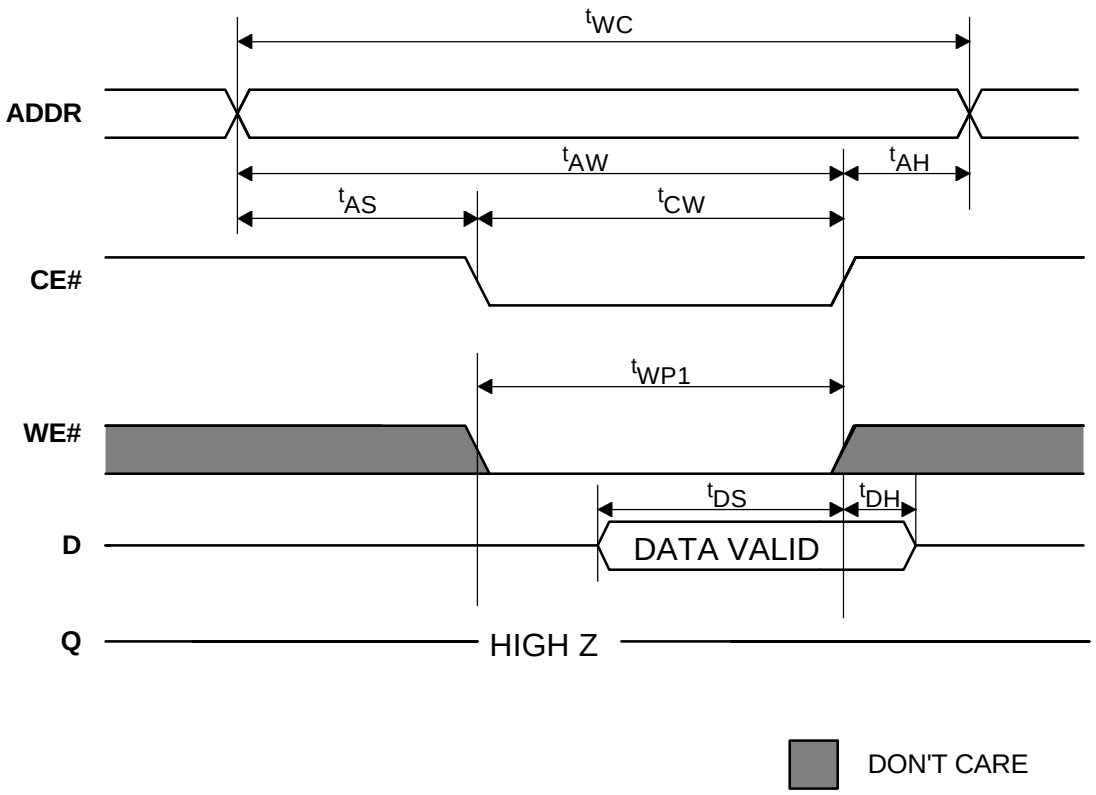


WRITE CYCLE NO. 2(12, 13)

(Write Enable Controlled with Output Enable OE# inactive HIGH)

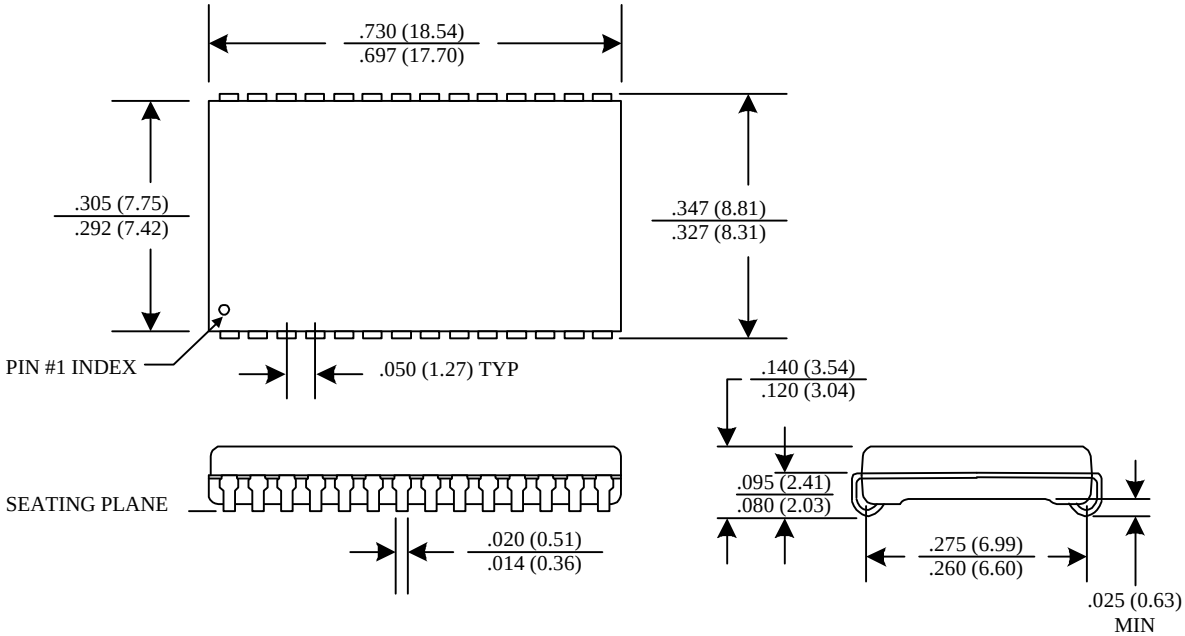


WRITE CYCLE NO. 3(12, 13)
(Chip Enable Controlled)



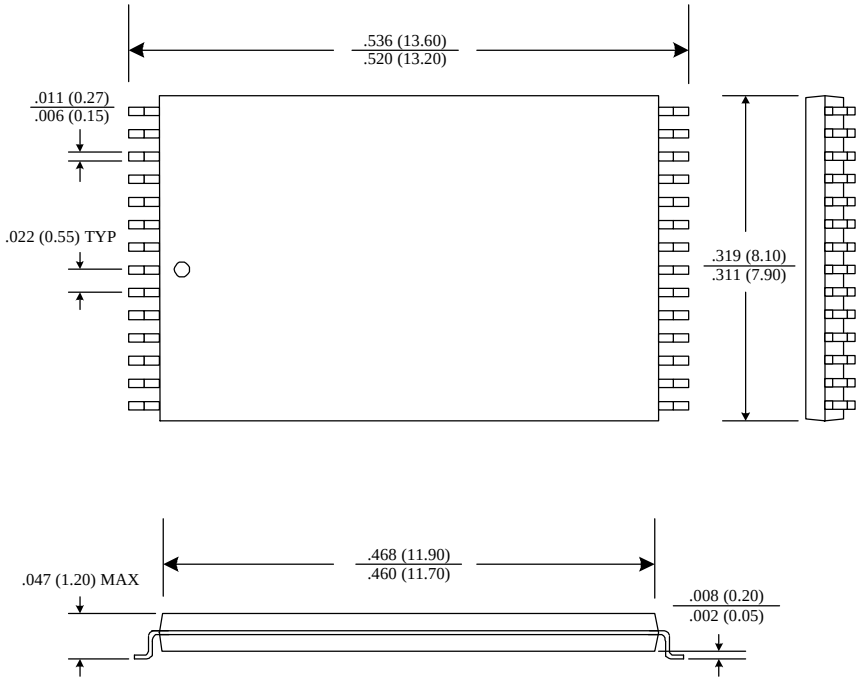
Package Dimensions

28-pin 300 Mil Plastic SOJ (SJ)



Note: All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical, min where noted.

28-pin Plastic TSOP (TS)



Note: All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical, max where noted.

Ordering Information

GVT 7232A8 XX - XX X X