ASYNCHRONOUS SRAM

128K x 24 SRAM

+3.3V SUPPLY, THREE MEGABIT THREE CHIP ENABLES

FEATURES

- Fast access times: 9, 10, 12 and 15ns
- Fast OE# access times: 4, 5, 6 and 7ns
- Single +3.3V±0.3V power supply
- Fully static -- no clock or timing strobes necessary
- All inputs and outputs are TTL-compatible
- Three state outputs
- Easy memory expansion with CE#, CE1#, CE2 and OE# options
- Automatic chip deselect power down
- High-performance, low-power consumption, CMOS, double-metal process
- Low profile 100 pin TQFP and 119 bump, 14mm x 22mm PBGA (Ball Grid Array) packages
- Multiple Ground and VCC pins for maximum noise immunity

OPTIONS	MARKING	
• Timing		
9ns access	-9	
10ns access	-10	
12ns access	-12	
15ns access	-15	
• Packages		
100-pin TQFP	T	
119-lead BGA	B	
• Temperature		
Commercial	None	(0°C to 70°C)
Industrial	I	(-40°C to 85°C)

GENERAL DESCRIPTION

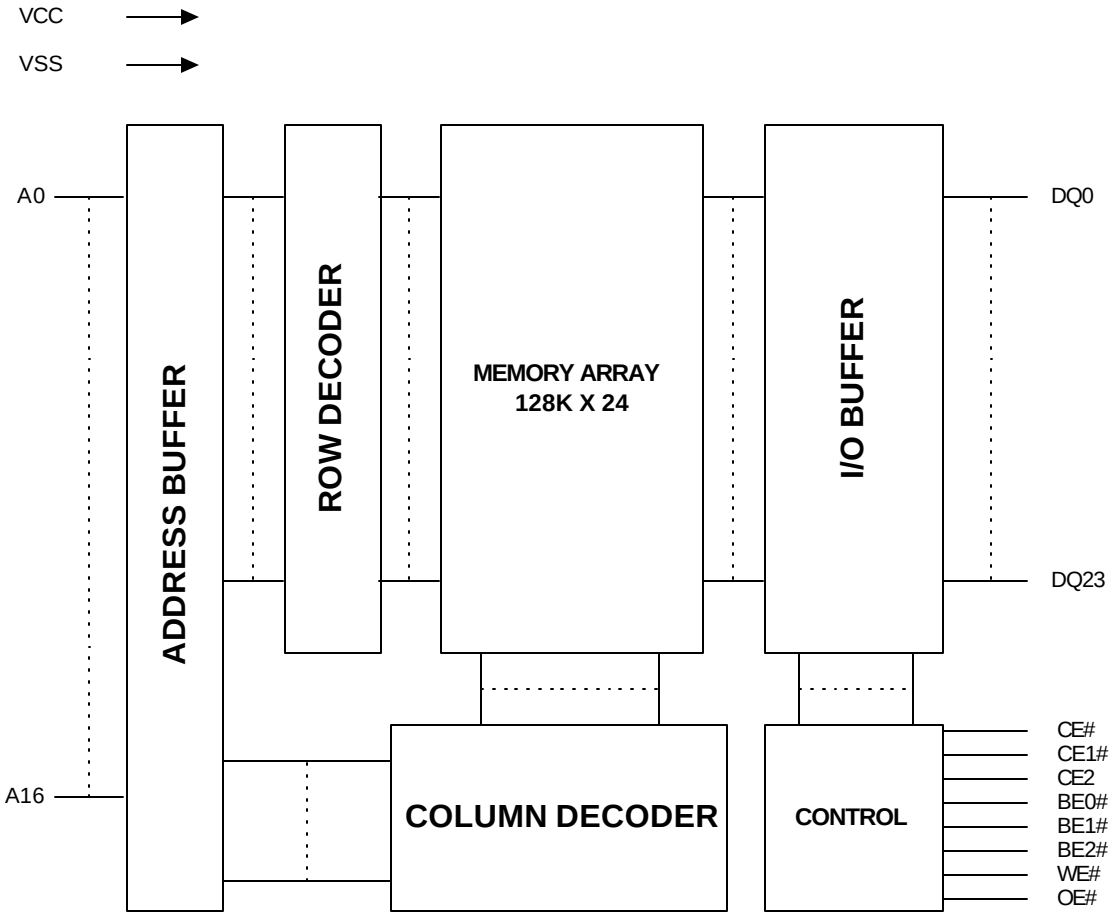
The GVT73128A24 and GVT73128S24 are organized as a 131,072 x 24 SRAM using a four-transistor memory cell with a high performance, silicon gate, low-power CMOS process. Galvantech SRAMs are fabricated using triple-layer polysilicon, double-layer metal technology.

This device offers multiple power and ground pins for improved performance and noise immunity. For increased system flexibility and eliminating bus contention problems, this device offers multiple chip enables (CE#, CE1# and CE2), and output enable (OE#) with this organization. For GVT73128S24 device in 100-pin TQFP package, separate byte enables (BE0#, BE1#, and BE2#) are also available to control individual bytes.

Writing to the device is accomplished by bringing Chip Enables (CE# and CE1#) and Write Enable (WE#) inputs LOW and CE2 HIGH. Reading from the device is accomplished by bringing Chip Enables (CE# and CE1#) LOW and bringing CE2 and Write Enable (WE#) inputs HIGH, along with Output Enable (OE#) being asserted LOW.

The device offers a low power standby mode when chip is not selected. This allows system designers to meet low standby power requirements.

FUNCTIONAL BLOCK DIAGRAM

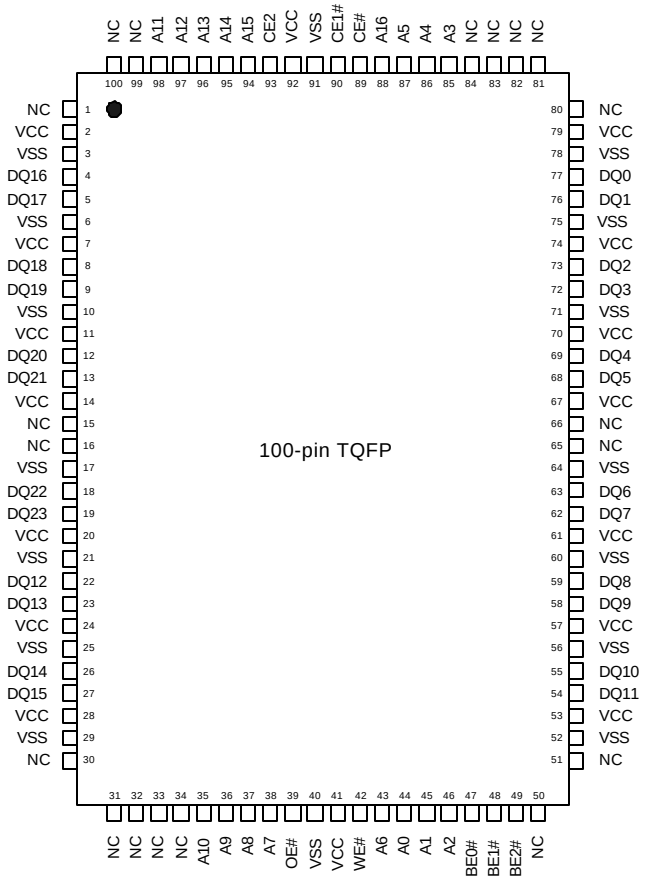


Note: BE0#, BE1# and BE2# are available for GVT73128S24 only.

128Kx24, 119-Bump PBGA (Top View)

	1	2	3	4	5	6	7
A	NC	A11	A14	A15	A16	A4	NC
B	NC	A12	A13	CE#	A5	A3	NC
C	DQ16	NC	CE2	NC	CE1#	NC	DQ0
D	DQ17	VCC	VSS	VSS	VSS	VCC	DQ1
E	DQ18	VSS	VCC	VSS	VCC	VSS	DQ2
F	DQ19	VCC	VSS	VSS	VSS	VCC	DQ3
G	DQ20	VSS	VCC	VSS	VCC	VSS	DQ4
H	DQ21	VCC	VSS	VSS	VSS	VCC	DQ5
J	VCC	VSS	VCC	VSS	VCC	VSS	VCC
K	DQ22	VCC	VSS	VSS	VSS	VCC	DQ6
L	DQ23	VSS	VCC	VSS	VCC	VSS	DQ7
M	DQ12	VCC	VSS	VSS	VSS	VCC	DQ8
N	DQ13	VSS	VCC	VSS	VCC	VSS	DQ9
P	DQ14	VCC	VSS	VSS	VSS	VCC	DQ10
R	DQ15	NC	NC	NC	NC	NC	DQ11
T	NC	A10	A8	WE#	A0	A1	NC
U	NC	A9	A7	OE#	A6	A2	NC

128Kx24, 100-PIN TQFP (Top View)



Note: BE0#, BE1# and BE2# are available for GVT73128S24 in 100-pin TQFP package only. For GVT73128A24 in 100-pin TQFP package, pin# 47, 48 and 49 are NC.

PIN DESCRIPTIONS

TQFP PINS GVT73128A24	TQFP PINS GVT73128S24	BGA PINS	SYMBOL	TYPE	DESCRIPTION
44, 45, 46, 85, 86, 87, 43, 38, 37, 36, 35, 98, 97, 96, 95, 94, 88	44, 45, 46, 85, 86, 87, 43, 38, 37, 36, 35, 98, 97, 96, 95, 94, 88	5T, 6T, 6U, 6B, 6A, 5B, 5U, 3U, 3T, 2U, 2T, 2A, 2B, 3B, 3A, 4A, 5A	A0-A16	Input	Address Inputs: These inputs determine which cell is addressed.
42	42	4T	WE#	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. WE# is LOW for a WRITE cycle and HIGH for a READ cycle.
89, 90, 93	89, 90, 93	4B, 5C, 3C	CE#, CE1#, CE2	Input	Chip Enable: These inputs are used to enable the device. When CE# and CE1# are LOW and CE2 is HIGH, the chip is selected. When CE# or CE1# are HIGH or CE2 is LOW, the chip is disabled and automatically goes into standby power mode.
-	47, 48,49	-	BE0#, BE1#, BE2#	Input	Byte Enable: These active LOW inputs are available for GVT73128A24 in 100-pin TQFP package only. These active LOW inputs allow individual bytes to be written or read. When BE0# is LOW, the data is written to or read from the lower byte (DQ0-DQ7). When BE1# is LOW, the data is written to or read from the middle byte (DQ8-DQ15). When BE2# is LOW, the data is written to or read from the higher byte (DQ16-DQ23).
39	39	4U	OE#	Input	Output Enable: This active LOW input enables the output drivers.
77, 76, 73, 72, 69, 68, 63, 62, 59, 58, 55, 54, 22, 23, 26, 27, 4, 5, 8, 9, 12, 13, 18, 19	77, 76, 73, 72, 69, 68, 63, 62, 59, 58, 55, 54, 22, 23, 26, 27, 4, 5, 8, 9, 12, 13, 18, 19	7C, 7D, 7E, 7F, 7G, 7H, 7K, 7L, 7M, 7N, 7P, 7R, 8M, 8N, 8P, 8R, 8C, 8D, 8E, 8F, 8G, 8H, 8K, 8L	DQ0-DQ23	Input/Output	SRAM Data I/O: Data inputs and data outputs.
2, 7, 11, 14, 20, 24, 28, 41, 53, 57, 61, 67, 70, 74, 79, 92	2, 7, 11, 14, 20, 24, 28, 41, 53, 57, 61, 67, 70, 74, 79, 92	1J, 2D, 2F, 2H, 2K, 2M, 2P, 3E, 3G, 3J, 3L, 3N 5E, 5G, 5J, 5L, 5N, 6D, 6F, 6H, 6K, 6M, 6P, 7J	VCC	Supply	Power Supply: 3.3V $\pm$ 0.3V
3, 6, 10, 17, 21, 25, 29, 40, 52, 56, 60, 64, 71, 75, 78, 91	3, 6, 10, 17, 21, 25, 29, 40, 52, 56, 60, 64, 71, 75, 78, 91	2E, 2G, 2J, 2L, 2N, 3D, 3F, 3H, 3K, 3M, 3P, 4D, 4E, 4F, 4G, 4H, 4J, 4K, 4L, 4M, 4N, 4P, 5D, 5F, 5H, 5K, 5M, 5P, 6E, 6G, 6J, 6L, 6N	VSS	Ground	Ground
1, 15, 16, 30, 31, 32, 33, 34, 47, 48, 49, 50, 51, 65, 66, 80, 81, 82, 83, 84, 99, 100	1, 15, 16, 30, 31, 32, 33, 34, 50, 51, 65, 66, 80, 81, 82, 83, 84, 99, 100	1A, 1B, 1T, 1U, 2C, 2R, 3R, 4C, 4R, 5R, 6C, 6R, 7A, 7B, 7T, 7U	NC	-	No Connect: These signals are not internally connected. User can connect them to VCC, VSS, or any signal lines or simply leave them floating.

TRUTH TABLE

MODE	CE#	CE1#	CE2	WE#	OE#	BE0#	BE1#	BE2#	DQ0-DQ7	DQ8-DQ15	DQ16-DQ23	POWER
STANDBY	H	X	X	X	X	X	X	X	HIGH-Z	HIGH-Z	HIGH-Z	STANDBY
STANDBY	X	H	X	X	X	X	X	X	HIGH-Z	HIGH-Z	HIGH-Z	STANDBY
STANDBY	X	X	L	X	X	X	X	X	HIGH-Z	HIGH-Z	HIGH-Z	STANDBY
BYTE 0 READ (DQ0-DQ7)	L	L	H	H	L	L	H	H	Q	HIGH-Z	HIGH-Z	ACTIVE
BYTE 1 READ (DQ8-DQ15)	L	L	H	H	L	H	L	H	HIGH-Z	Q	HIGH-Z	ACTIVE
BYTE 2 READ (DQ16-DQ23)	L	L	H	H	L	H	H	L	HIGH-Z	HIGH-Z	Q	ACTIVE
WORD READ (DQa-DQd)	L	L	H	H	L	L	L	L	Q	Q	Q	ACTIVE
WORD WRITE (DQa-DQd)	L	L	H	L	X	L	L	L	D	D	D	ACTIVE
BYTE 0 WRITE (DQ0-DQ7)	L	L	H	L	X	L	H	H	D	HIGH-Z	HIGH-Z	ACTIVE
BYTE 1 WRITE (DQ8-DQ15)	L	L	H	L	X	H	L	H	HIGH-Z	D	HIGH-Z	ACTIVE
BYTE 2 WRITE (DQ16-DQ23)	L	L	H	L	X	H	H	L	HIGH-Z	HIGH-Z	D	ACTIVE
OUTPUT DISABLE	L	L	H	X	X	H	H	H	HIGH-Z	HIGH-Z	HIGH-Z	ACTIVE
	L	L	H	H	H	X	X	X	HIGH-Z	HIGH-Z	HIGH-Z	ACTIVE

Note: BE0#, BE1# and BE2# are available for GVT73128S24 in 100-pin TQFP package only.

ABSOLUTE MAXIMUM RATINGS*

Voltage on VCC Supply Relative to VSS.....-0.5V to +4.6V
V_{IN} .....-0.5V to VCC+1.0V
Storage Temperature (plastic) .....-65°C to +150°
Ambient Temperature .....-55°C to +125°
Junction Temperature ..... +125°
Power Dissipation 1.0W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(All Temperature Ranges; VCC = 3.3V ±0.3V unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	Data Inputs (DQx)	V_{IHD}	2.2	VCC+0.5	V	1, 2
	All Other Inputs	V_{IH}	2.2	4.6	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \leq V_{IN} \leq VCC$	IL_I	-5	5	uA	
Output Leakage Current	Output(s) disabled, $0V \leq V_{OUT} \leq VCC$	IL_O	-5	5	uA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		VCC	3.0	3.6	V	1

DESCRIPTION	CONDITIONS	SYM	TYP	-9	-10	-12	-15	UNITS	NOTES
Power Supply Current: Operating	Device selected; $CE\# \leq V_{IL}$; VCC =MAX; $f=f_{MAX}$; outputs open	Icc	80	165	150	130	110	mA	3, 14
TTL Standby	$CE\# \geq V_{IH}$; VCC = MAX; $f=f_{MAX}$	I_{SB1}	30	55	50	45	40	mA	14
CMOS Standby	CE1# ≥VCC -0.2; VCC = MAX; all other inputs ≤ VSS +0.2 or ≥VCC -0.2; all inputs static; f= 0	I_{SB2}	5	10	10	10	10	mA	14

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz VCC = 3.3V	C_I	6	pF	4
Input/Output Capacitance (DQ)		$C_{I/O}$	8	pF	4

AC ELECTRICAL CHARACTERISTICS

(Note 5) (All Temperature Ranges; VCC = 3.3V ±0.3V)

DESCRIPTION		- 9		- 10		- 12		- 15			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	^tRC	9		10		12		15		ns	
Address access time	^tAA		9		10		12		15	ns	
Chip Enable access time	^tACE		9		10		12		15	ns	
Output hold from address change	^tOH	3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	3		3		3		3		ns	4, 7
Chip disable to output in High-Z	^tHZCE		4		5		6		7	ns	4, 6, 7
Output Enable access time	^tAOE		4		5		6		7	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	
Output Enable to output in High-Z	^tHZOE		5		5		6		7	ns	4, 6
Byte Enable access time	^tABE		5		5		6		7	ns	
Byte Enable to output in Low-Z	^tLZBE	0		0		0		0		ns	4, 7
Byte disable to output in High-Z	^tHZBE		5		5		6		7	ns	4, 6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	4
Chip disable to power-down time	^tPD		9		10		12		15	ns	4
WRITE Cycle											
WRITE cycle time	^tWC	9		10		12		15		ns	
Chip Enable to end of write	^tCW	7		7		8		9		ns	
Address valid to end of write, with OE# HIGH	^tAW	7		7		8		9		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
WRITE pulse width	$^tWP2$	9		9		10		11		ns	
WRITE pulse width, with OE# HIGH	$^tWP1$	7		7		8		9		ns	
Data setup time	^tDS	5.5		6		6		7		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		3		4		5		ns	4, 7
Write Enable to output in High-Z	^tHZWE		5		5		6		7	ns	4, 6, 7
Byte Enable to end of write	^tBW	7		7		8		9		ns	

AC TEST CONDITIONS

Input pulse levels	0V to 3.0V
Input rise and fall times	1.5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

OUTPUT LOADS

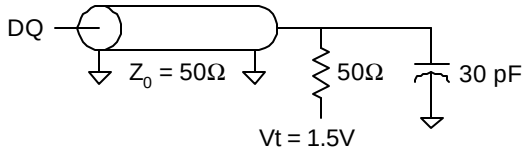


Fig. 1 OUTPUT LOAD EQUIVALENT

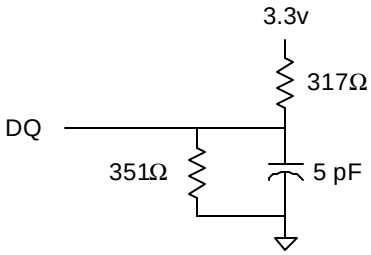
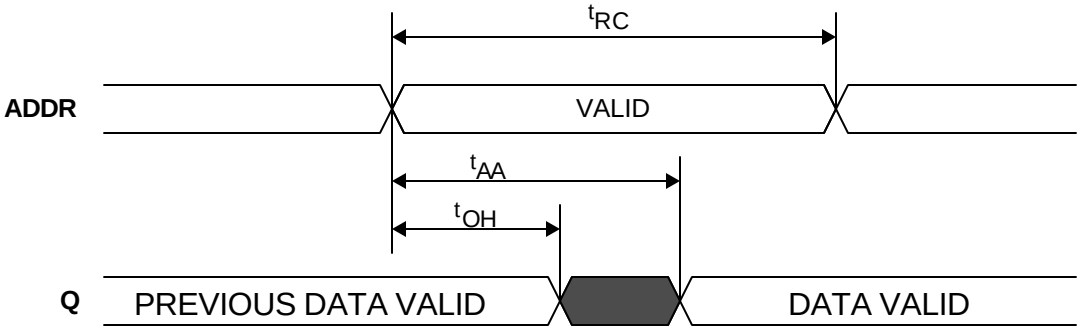


Fig. 2 OUTPUT LOAD EQUIVALENT

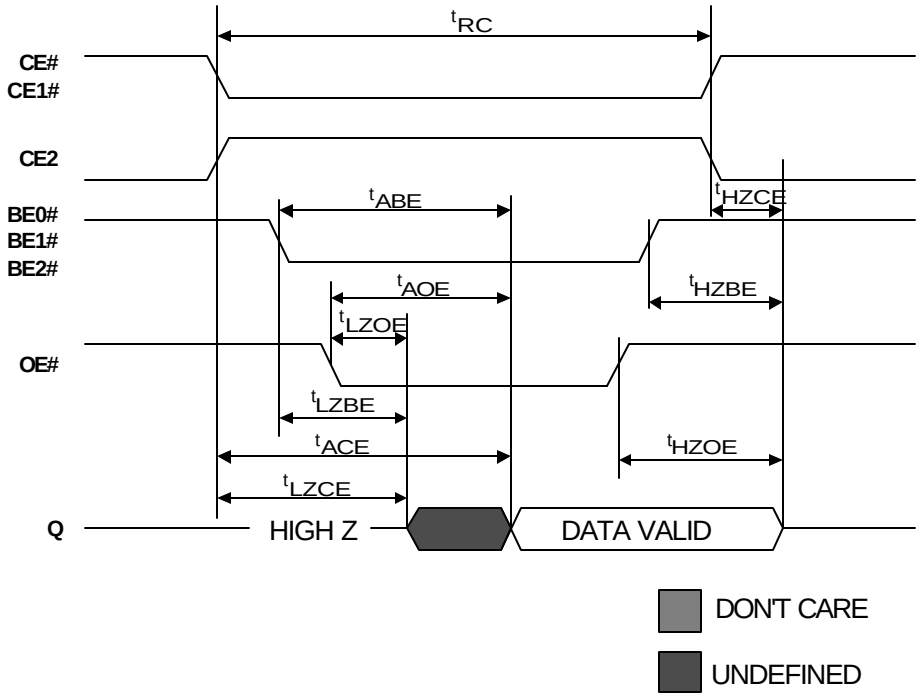
NOTES

1. All voltages referenced to VSS (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tRC/2$.
   Undershoot: $V_{IL} \leq -2.0V$ for $t \leq {}^tRC/2$
3. I_{cc} is given with no output current. I_{cc} increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with C_L=5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$ and ${}^tHZWE$ is less than ${}^tLZWE$.
8. WE# is HIGH for READ cycle.
9. Device is continuously selected. Chip enable and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. t_{RC} = Read Cycle Time.
12. Chip Enable and Write Enable can initiate and terminate a WRITE cycle.
13. Capacitance derating applies to capacitance different from the load capacitance shown in Fig. 1.
14. Typical values are measured at 3.3V, 25°C and 15ns cycle time.

READ CYCLE NO. 1(8, 9)



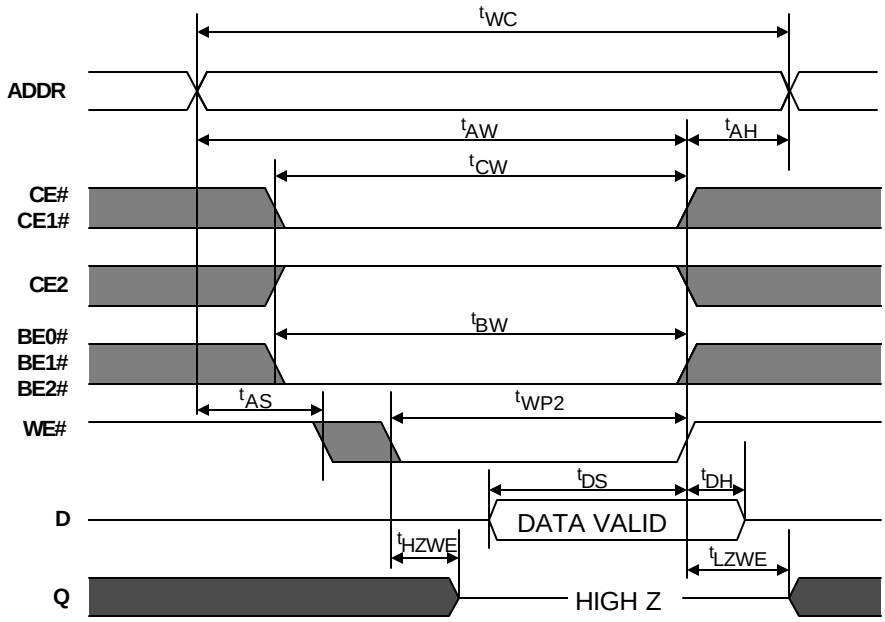
READ CYCLE NO. 2(7, 8, 10, 12)



Note: BE0#, BE1# and BE2# are available for GVT73128S24 only.

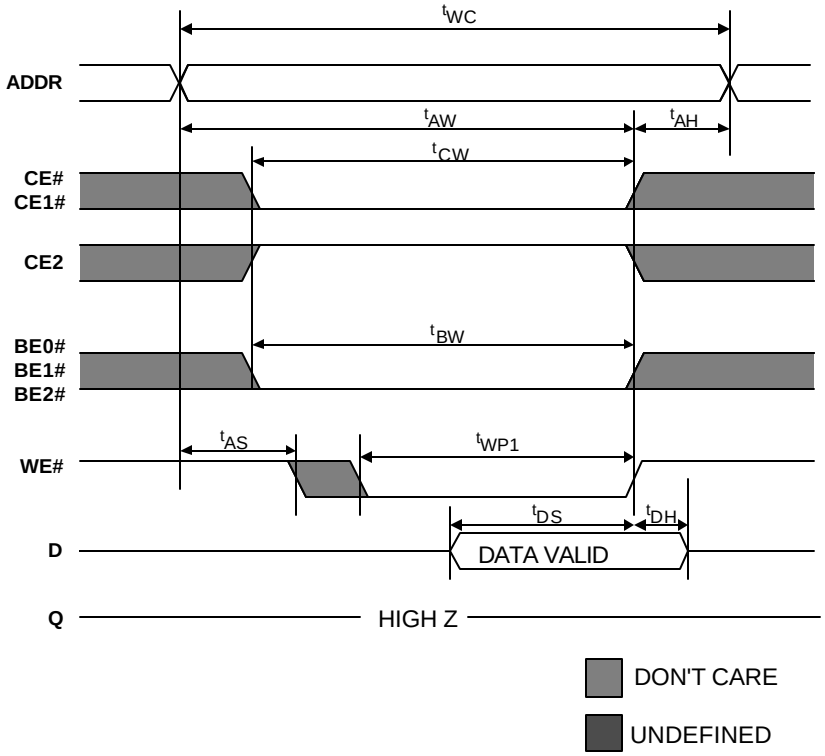
WRITE CYCLE NO. 1[7, 12, 13]

(Write Enable Controlled with Output Enable OE# active LOW))



WRITE CYCLE NO. 2[12, 13]

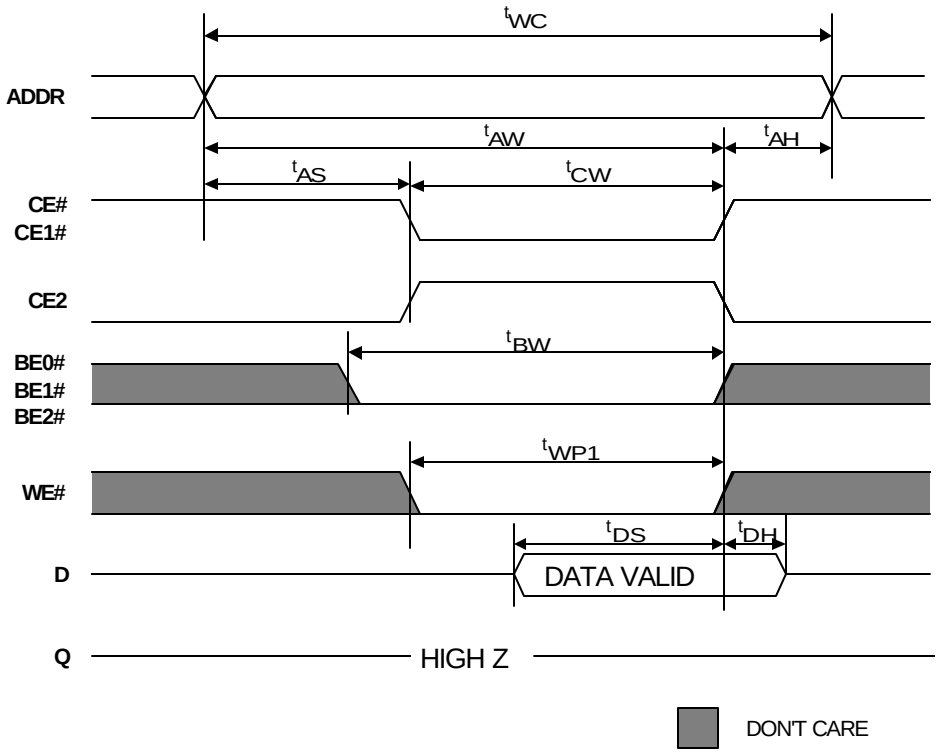
(Write Enable Controlled with Output Enable OE# inactive HIGH)



Note: BE0#, BE1# and BE2# are available for GVT73128S24 only.

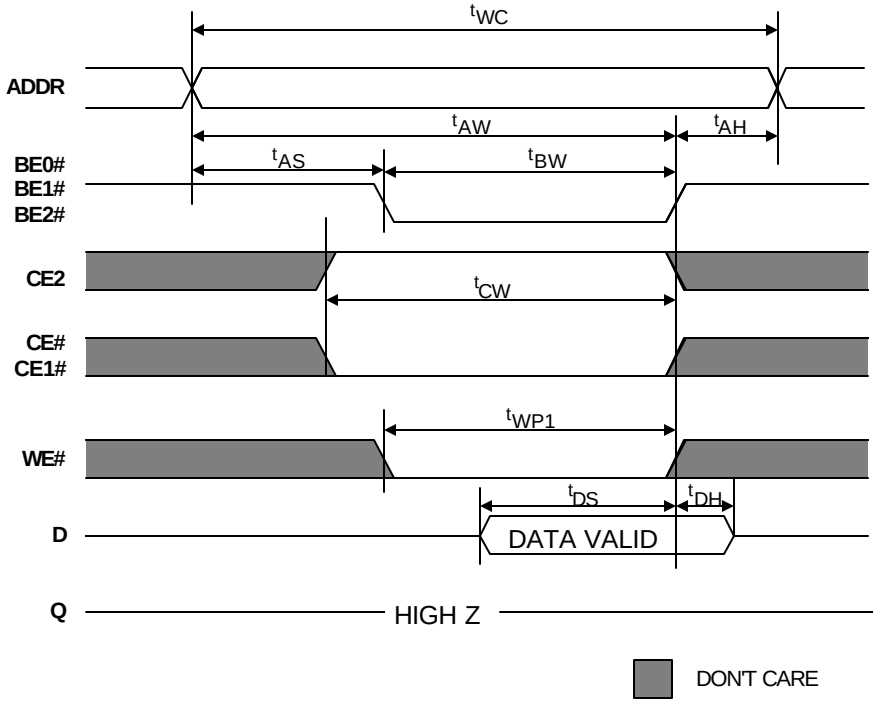
WRITE CYCLE NO. 3[12, 13]

(Chip Enable Controlled)



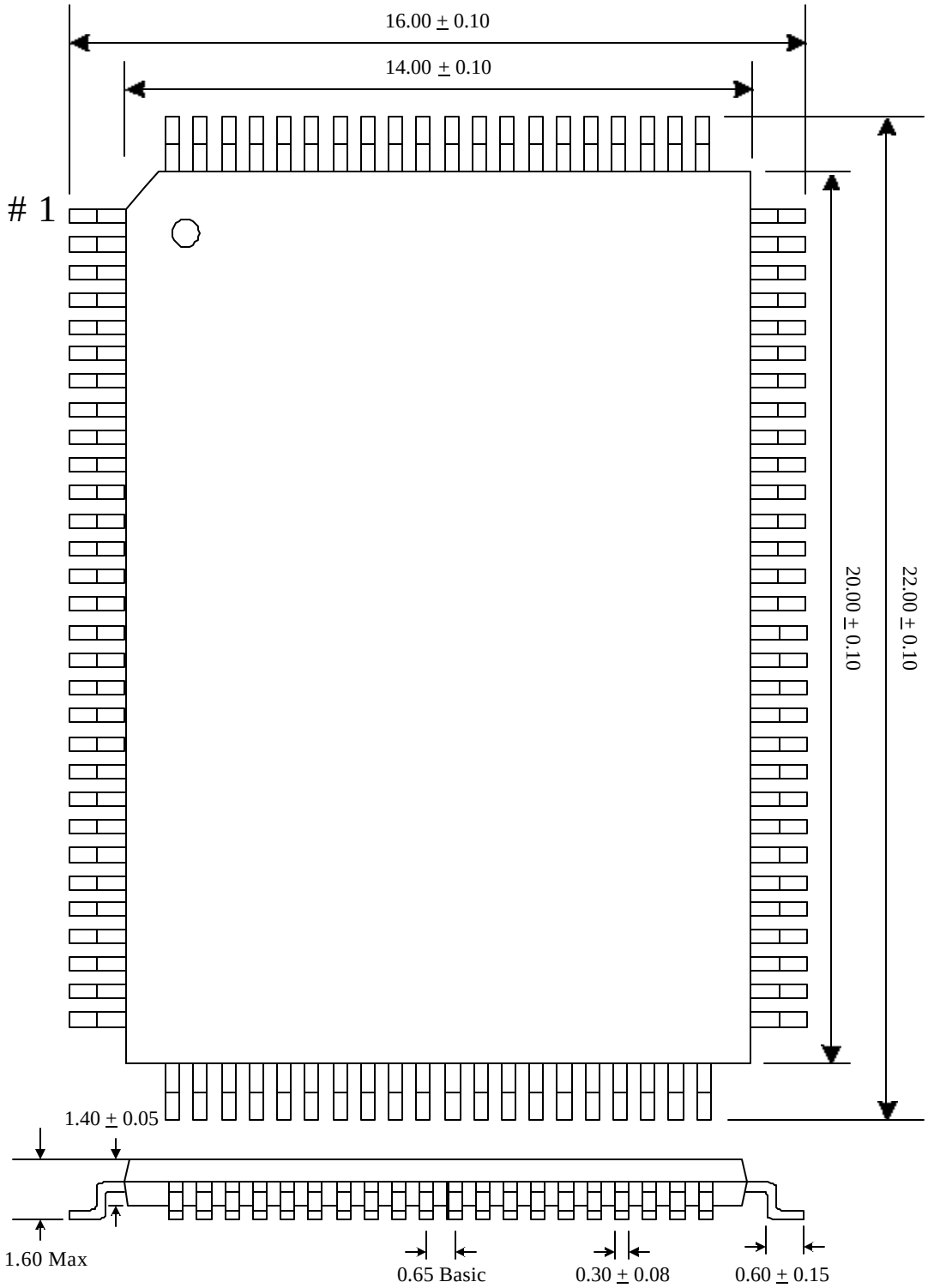
WRITE CYCLE NO. 4[12, 13]

(Byte Enable Controlled)



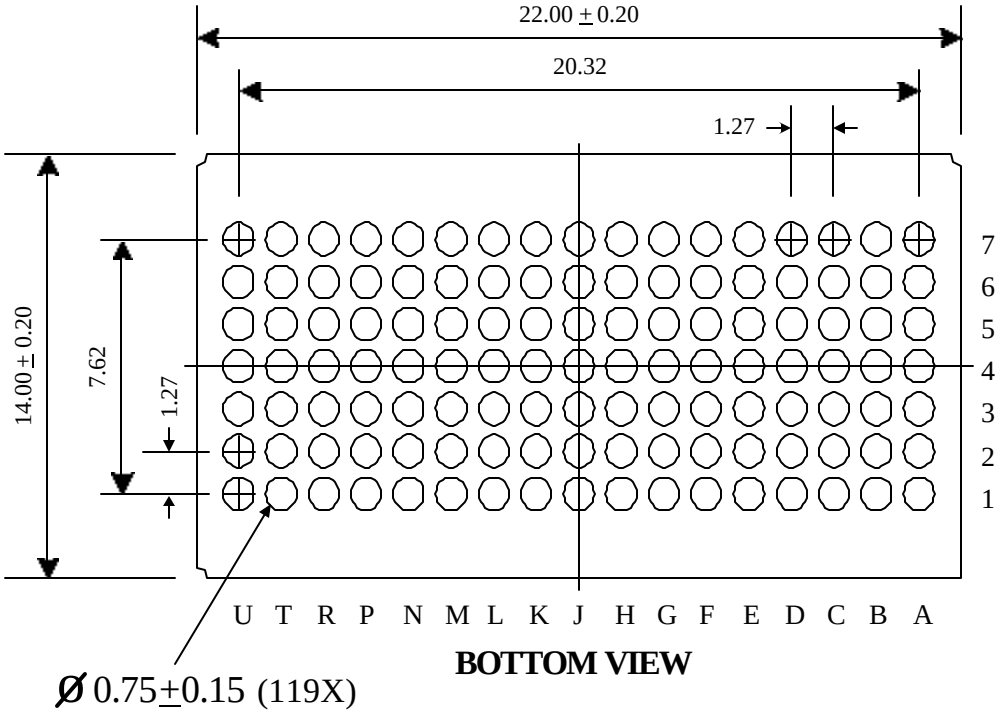
Note: BE0#, BE1# and BE2# are available for GVT73128S24 only.

100 Pin TQFP Package Dimensions

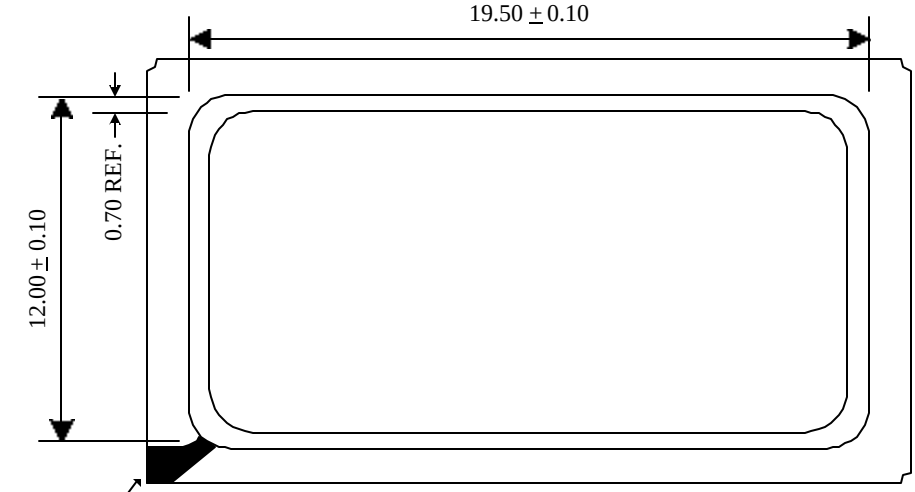


Note: All dimensions in Millimeters

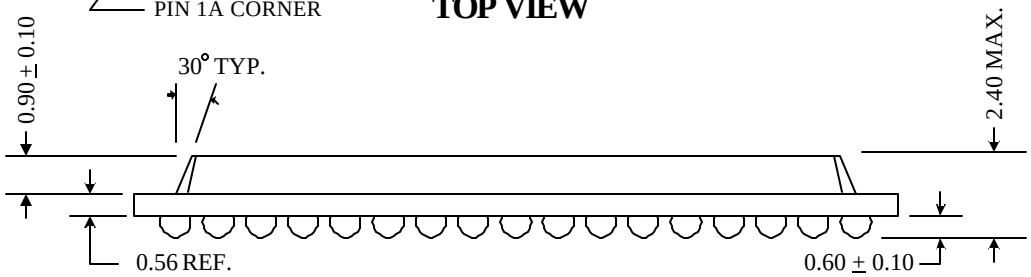
7 x 17 (119-lead) BGA Dimensions



BOTTOM VIEW



TOP VIEW



SIDE VIEW

Note: All dimensions in Millimeters

Ordering Information for 128K x 24