SYNCHRONOUS BURST SRAM PIPELINED OUTPUT

256K x 18 SRAM

+3.3V SUPPLY, FULLY REGISTERED INPUTS AND OUTPUTS, BURST COUNTER

FEATURES

- Fast access times: 3.5, 3.8, and 4.0ns
- Fast clock speed: 166, 150, 133, and 117MHz
- Provide high performance 3-1-1-1 access rate
- Fast OE# access times: 3.5ns and 3.8ns
- Optimal for depth expansion (one cycle chip deselect to eliminate bus contention)
- 3.3V -5% and +10% core power supply
- 2.5V or 3.3V I/O supply
- 5V tolerant inputs except I/O's
- Clamp diodes to VSSQ at all inputs and outputs
- Common data inputs and data outputs
- BYTE WRITE ENABLE and GLOBAL WRITE control
- Three chip enables for depth expansion and address pipeline
- Address, data and control registers
- Internally self-timed WRITE CYCLE
- Burst control pins (interleaved or linear burst sequence)
- Automatic power-down for portable applications
- Low profile 119 lead, 14mm x 22mm BGA (Ball Grid Array) and 100 pin TQFP packages

OPTIONS — MARKING

- Timing

3.5ns access/6.0ns cycle	-3
3.8ns access/6.7ns cycle	-4
4.0ns access/7.5ns cycle	-5
4.0ns access/8.5ns cycle	-6

- Packages

119-lead BGA	B
100-pin TQFP	T

GENERAL DESCRIPTION

The Galvantech Synchronous Burst SRAM family employs high-speed, low power CMOS designs using advanced triple-layer polysilicon, double-layer metal technology. Each memory cell consists of four transistors and two high valued resistors.

The GVT71256D18 SRAM integrates 262,144x18 SRAM cells with advanced synchronous peripheral circuitry and a 2-bit counter for internal burst operation. All synchronous inputs are gated by registers controlled by a positive-edge-triggered clock input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining chip enable (CE#), depth-expansion chip enables (CE2# and CE2), burst control inputs (ADSC#, ADSP#, and ADV#), write enables (WEL#, WEH#, and BWE#), and global write (GW#).

Asynchronous inputs include the output enable (OE#) and burst mode control (MODE). The data outputs (Q), enabled by OE#, are also asynchronous.

Addresses and chip enables are registered with either address status processor (ADSP#) or address status controller (ADSC#) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin (ADV#).

Address, data inputs, and write controls are registered on-chip to initiate self-timed WRITE cycle. WRITE cycles can be one to four bytes wide as controlled by the write control inputs. Individual byte write allows individual byte to be written. WEL# controls DQ1-DQ8 and DQP1. WEH# controls DQ9-DQ16 and DQP2. WEL#, and WEH# can be active only with BWE# being LOW. GW# being LOW causes all bytes to be written. WRITE pass-through capability allows written data available at the output for the immediately next READ cycle. This device also incorporates pipelined enable circuit for easy depth expansion without penalizing system performance.

The GVT71256D18 operates from a +3.3V power supply. All inputs and outputs are LVTTL compatible. The device is ideally suited for 486, Pentium™, 680x0, and PowerPC™ systems and for systems that are benefited from a wide synchronous data bus.

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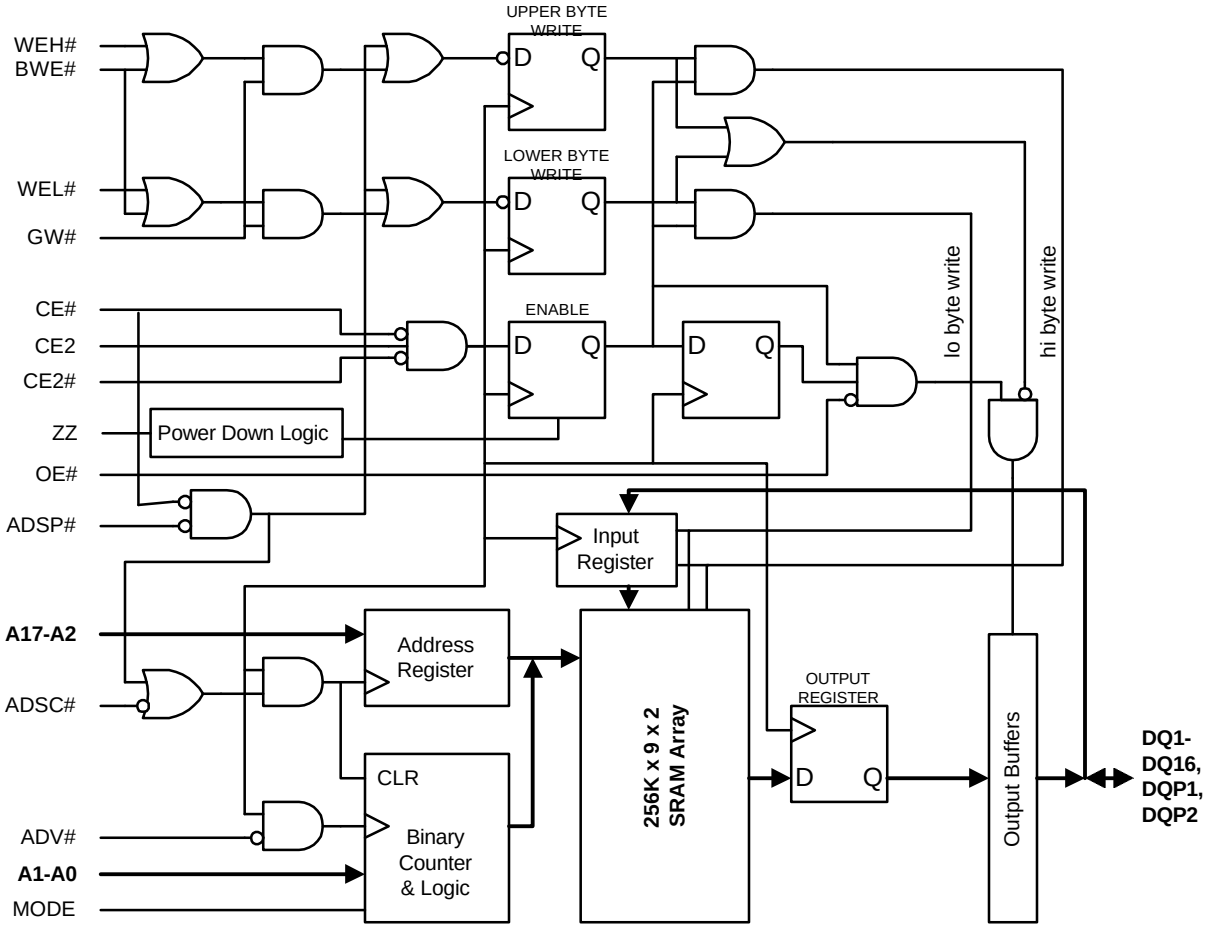
Rev. 11/98

FUNCTIONAL BLOCK DIAGRAM

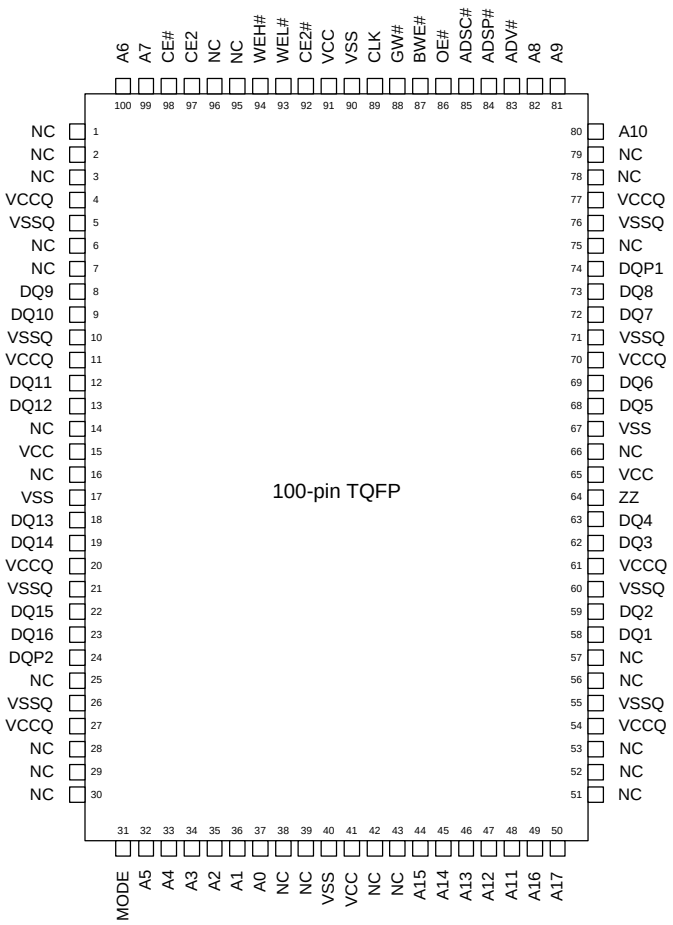


NOTE: The Functional Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

PIN ASSIGNMENT (Top View)

	1	2	3	4	5	6	7
A	VCCQ	A6	A4	ADSP#	A8	A16	VCCQ
B	NC	CE2	A3	ADSC#	A9	CE2#	NC
C	NC	A7	A2	VCC	A12	A15	NC
D	DQ9	NC	VSS	NC	VSS	DQP1	NC
E	NC	DQ10	VSS	CE#	VSS	NC	DQ8
F	VCCQ	NC	VSS	OE#	VSS	DQ7	VCCQ
G	NC	DQ11	WEH#	ADV#	VSS	NC	DQ6
H	DQ12	NC	VSS	GW#	VSS	DQ5	NC
J	VCCQ	VCC	NC	VCC	NC	VCC	VCCQ
K	NC	DQ13	VSS	CLK	VSS	NC	DQ4
L	DQ14	NC	VSS	NC	WEL#	DQ3	NC
M	VCCQ	DQ15	VSS	BWE#	VSS	NC	VCCQ
N	DQ16	NC	VSS	A1	VSS	DQ2	NC
P	NC	DQP2	VSS	A0	VSS	NC	DQ1
R	NC	A5	MODE	VCC	NC	A13	NC
T	NC	A10	A11	NC	A14	A17	ZZ
U	VCCQ	NC	NC	NC	NC	NC	VCCQ

TOP VIEW 119 LEAD BGA



PIN DESCRIPTIONS

BGA PINS	TQFP PINS	SYMBOL	TYPE	DESCRIPTION
4P, 4N, 2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 2R, 6R, 2T, 3T, 5T, 6T	37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 80, 48, 47, 46, 45, 44, 49, 50	A0-A17	Input-Synchronous	Addresses: These inputs are registered and must meet the setup and hold times around the rising edge of CLK. The burst counter generates internal addresses associated with A0 and A1, during burst cycle and wait cycle.
5L, 3G	93, 94	WEL#, WEH#	Input-Synchronous	Byte Write Enables: A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. WEL# controls DQ1-DQ8 and DQP1. WEH# controls DQ9-DQ16 and DQP2. Data I/O are high impedance if either of these inputs are LOW, conditioned by BWE# being LOW.
4M	87	BWE#	Input-Synchronous	Write Enable: This active LOW input gates byte write operations and must meet the setup and hold times around the rising edge of CLK.
4H	88	GW#	Input-Synchronous	Global Write: This active LOW input allows a full 18-bit WRITE to occur independent of the BWE# and WEn# lines and must meet the setup and hold times around the rising edge of CLK.
4K	89	CLK	Input-Synchronous	Clock: This signal registers the addresses, data, chip enables, write control and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
4E	98	CE#	Input-Synchronous	Chip Enable: This active LOW input is used to enable the device and to gate ADSP#.
6B	92	CE2#	Input-Synchronous	Chip Enable: This active LOW input is used to enable the device.

PIN DESCRIPTIONS (continued)

BGA PINS	TQFP PINS	SYMBOL	TYPE	DESCRIPTION
2B	97	CE2	input-Synchronous	Chip enable: This active HIGH input is used to enable the device.
4F	86	OE#	Input	Output Enable: This active LOW asynchronous input enables the data output drivers.
4G	83	ADV#	Input-Synchronous	Address Advance: This active LOW input is used to control the internal burst counter. A HIGH on this pin generates wait cycle (no address advance).
4A	84	ADSP#	Input-Synchronous	Address Status Processor: This active LOW input, along with CE# being LOW, causes a new external address to be registered and a READ cycle is initiated using the new address.
4B	85	ADSC#	Input-Synchronous	Address Status Controller: This active LOW input causes device to be de-selected or selected along with new external address to be registered. A READ or WRITE cycle is initiated depending upon write control inputs.
3R	31	MODE	Input-Static	Mode: This input selects the burst sequence. A LOW on this pin selects LINEAR BURST. A NC or HIGH on this pin selects INTERLEAVED BURST.
7T	64	ZZ	Input-Asynchro-nous	Snooze: This active HIGH input puts the device in low power consumption standby mode. For normal operation, this input has to be either LOW or NC (No Connect).
6D, 7E, 6F, 7G, 6H, 7K, 6L, 6N, 1D, 2E, 2G, 1H, 2K, 1L, 2M, 1N	58, 59, 62, 63, 68, 69, 72, 73, 8, 9, 12, 13, 18, 19, 22, 23	DQ1-DQ16	Input/ Output	Data Inputs/Outputs: Low Byte is DQ1-DQ8. High Byte is DQ9-DQ16. Input data must meet setup and hold times around the rising edge of CLK.
2P, 7P	74, 24	DQP1, DQP2	Input/ Output	Parity Inputs/Outputs: DQP1 is parity bit for DQ1-DQ8 and DQP2 is parity bit for DQ9-DQ16.
4C, 2J, 4J, 6J, 4R	15, 41,65, 91	VCC	Supply	Power Supply: +3.3V -5% and +10%
3D, 5D, 3E, 5E, 3F, 5F, 5G, 3H, 5H, 3K, 5K, 3L, 3M, 5M, 3N, 5N, 3P, 5P	17, 40, 67, 90	VSS	Ground	Ground: GND.
1A, 7A, 1F, 7F, 1J, 7J, 1M, 7M, 1U, 7U	4, 11, 20, 27, 54, 61, 70, 77	VCCQ	I/O Supply	Output Buffer Supply: +2.5V or 3.3V
	5, 10, 21, 26, 55, 60, 71, 76	VSSQ	I/O Ground	Output Buffer Ground: GND
1B, 7B, 1C, 7C, 2D, 4D, 7D, 1E, 6E, 2F, 1G, 6G, 2H, 7H, 3J, 5J, 1K, 6K, 2L, 4L, 7L, 6M, 2N, 7N, 1P, 6P, 1R, 5R, 7R, 1T, 4T, 2U, 3U, 4U, 5U, 6U	1-3, 6, 7, 14, 16, 25, 28-30, 38, 39, 42, 43, 51-53, 56, 57, 66, 75, 78, 79, 80, 95, 96	NC	-	No Connect: These signals are not internally connected.

BURST ADDRESS TABLE (MODE = NC/VCC)

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
A...A00	A...A01	A...A10	A...A11
A...A01	A...A00	A...A11	A...A10
A...A10	A...A11	A...A00	A...A01
A...A11	A...A10	A...A01	A...A00

BURST ADDRESS TABLE (MODE = GND)

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
A...A00	A...A01	A...A10	A...A11
A...A01	A...A10	A...A11	A...A00
A...A10	A...A11	A...A00	A...A01
A...A11	A...A00	A...A01	A...A10

TRUTH TABLE

OPERATION	ADDRESS USED	CE#	CE2#	CE2	ADSP#	ADSC#	ADV#	WRITE#	OE#	CLK	DQ
Deselected Cycle, Power Down	None	H	X	X	X	L	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	X	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	H	X	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	X	L	H	L	X	X	X	L-H	High-Z
Deselected Cycle, Power Down	None	L	H	X	H	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	L	H	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	L-H	D

Note:
1. X means “don’t care.” H means logic HIGH. L means logic LOW. WRITE# = L means [BWE# + WEL#*WEH#]*GW# equals LOW. WRITE# = H means [BWE# + WEL#*WEH#]*GW# equals HIGH.
2. WEL# enables write to DQ1-DQ8 and DQP1. WEH# enables write to DQ9-DQ16 and DQP2.
3. All inputs except OE# must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. Suspending burst generates wait cycle.
5. For a write operation following a read operation, OE# must be HIGH before the input data required setup time plus High-Z time for OE# and staying HIGH throughout the input data hold time.
6. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
7. ADSP# LOW along with chip being selected always initiates a READ cycle at the L-H edge of CLK. A WRITE cycle can be performed by setting WRITE# LOW for the CLK L-H edge of the subsequent wait cycle. Refer to WRITE timing diagram for clarification.

PARTIAL TRUTH TABLE FOR READ/WRITE

FUNCTION	GW#	BWE#	WEH#	WEL#
READ	H	H	X	X
READ	H	L	H	H
WRITE one byte	H	L	L	H
WRITE all bytes	H	L	L	L
WRITE all bytes	L	X	X	X

ABSOLUTE MAXIMUM RATINGS*

Voltage on VCC Supply Relative to VSS.....-0.5V to +4.6V
V_{IN} .....-0.5V to VCC+0.5V
Storage Temperature (plastic) .....-55°C to +150°
Junction Temperature .....+150°
Power Dissipation 1.0W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(0°C ≤ T_a ≤ 70°C; VCC = 3.3V -5% and +10% unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) voltage	Data Inputs (DQxx)	V_{IHD}	2.0	VCC+0.3	V	1, 2
	All Other Inputs	V_{IH}	2.0	4.6	V	1, 2
Input Low (Logic 0) Voltage		V_{II}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ VCC	IL_I	-2	2	uA	
MODE and ZZ Input Leakage Current	0V ≤ V_{IN} ≤ VCC	IL_I	-30	30	uA	14
Output Leakage Current	Output(s) disabled, 0V ≤ V_{OUT} ≤ VCC	IL_O	-2	2	uA	
Output High Voltage	I_{OH} = -5.0mA	V_{OH}	2.4		V	1, 11
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1, 11
Supply Voltage		VCC	3.135	3.6	V	1
I/O Supply Voltage		VCCQ	3.135	VCC	V	1

DESCRIPTION	CONDITIONS	SYM	TYP	-3	-4	-5	-6	UNITS	NOTES
Power Supply Current: Operating	Device selected; all inputs ≤ V_{IL} or ≥ V_{IH}; cycle time ≥ ^tKC MIN; VCC =MAX; outputs open	Icc	150	425	400	375	350	mA	3, 12, 13
CMOS Standby	Device deselected; VCC = MAX; all inputs ≤ VSS +0.2 or ≥VCC -0.2; all inputs static; CLK frequency = 0	I_{SB2}	5	10	10	10	10	mA	12,13
TTL Standby	Device deselected; all inputs ≤ V_{IL} or ≥ V_{IH}; all inputs static; VCC = MAX; CLK frequency = 0	I_{SB3}	10	20	20	20	20	mA	12,13
Clock Running	Device deselected; all inputs ≤ V_{IL} or ≥ V_{IH}; VCC = MAX; CLK cycle time ≥ ^tKC MIN	I_{SB4}	40	90	80	70	60	mA	12,13

AC ELECTRICAL CHARACTERISTICS

(Note 5) ($0^oC \leq T_A \leq 70^oC$; VCC = 3.3V -5% and +10%)

DESCRIPTION		- 3 166MHz		- 4 150MHz		- 5 133MHz		- 6 117MHz			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Clock											
Clock cycle time	^tKC	6.0		6.7		7.5		8.5		ns	
Clock HIGH time	^tKH	2.4		2.6		2.8		3.4		ns	
Clock LOW time	^tKL	2.4		2.6		2.8		3.4		ns	
Output Times											
Clock to output valid	^tKQ		3.5		3.8		4.0		4.0	ns	
Clock to output invalid	^tKQX	1.5		1.5		1.5		1.5		ns	
Clock to output in Low-Z	^tKQLZ	0		0		0		0		ns	4, 6,7
Clock to output in High-Z	^tKQHZ	1.5	6.0	1.5	6.7	1.5	7.5	1.5	8.5	ns	4, 6,7
OE to output valid	^tOEQ		3.5		3.5		3.8		3.8	ns	9
OE to output in Low-Z	^tOELZ	0		0		0		0		ns	4, 6,7
OE to output in High-Z	^tOEHZ		3.5		3.5		3.8		3.8	ns	4, 6,7
Setup Times											
Address, Controls and Data In	^tS	1.5		1.5		1.5		2.0		ns	10
Hold Times											
Address, Controls and Data In	^tH	0.5		0.5		0.5		0.5		ns	10

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	$T_A = 25^oC$; f = 1 MHz VCC = 3.3V	C_I	4	5	pF	4
Input/Output Capacitance (DQ)		C_O	7	8	pF	4

THERMAL CONSIDERATION

DESCRIPTION	CONDITIONS	SYMBOL	TQFP TYP	UNITS	NOTES
Thermal Resistance - Junction to Ambient	Still air, soldered on 4.25 x 1.125 inch 4-layer PCB	Θ_{JA}	25	^{o}C/W	
Thermal Resistance - Junction to Case		Θ_{JC}	9	^{o}C/W	

TYPICAL OUTPUT BUFFER CHARACTERISTICS

OUTPUT HIGH VOLTAGE	PULL-UP CURRENT			OUTPUT LOW VOLTAGE	PULL-DOWN CURRENT	
VOH (V)	IOH(mA) Min	IOH(mA) Max		VOL (V)	IOL(mA) Min	IOL(mA) Max
-0.5	-38	-105		-0.5	0	0
0	-38	-105		0	0	0
0.8	-38	-105		0.4	10	20
1.25	-26	-83		0.8	20	40
1.5	-20	-70		1.25	31	63
2.3	0	-30		1.6	40	80
2.7	0	-10		2.8	40	80
2.9	0	0		3.2	40	80
3.4	0	0		3.4	40	80

AC TEST CONDITIONS

Input pulse levels	0V to 3V
Input slew rate	1.0V/ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

OUTPUT LOADS

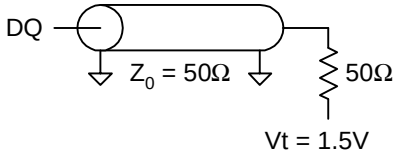


Fig. 1 OUTPUT LOAD EQUIVALENT

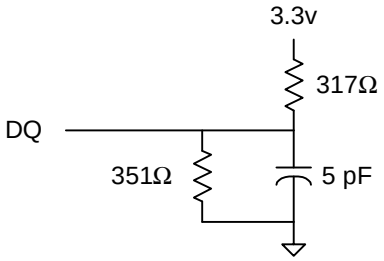
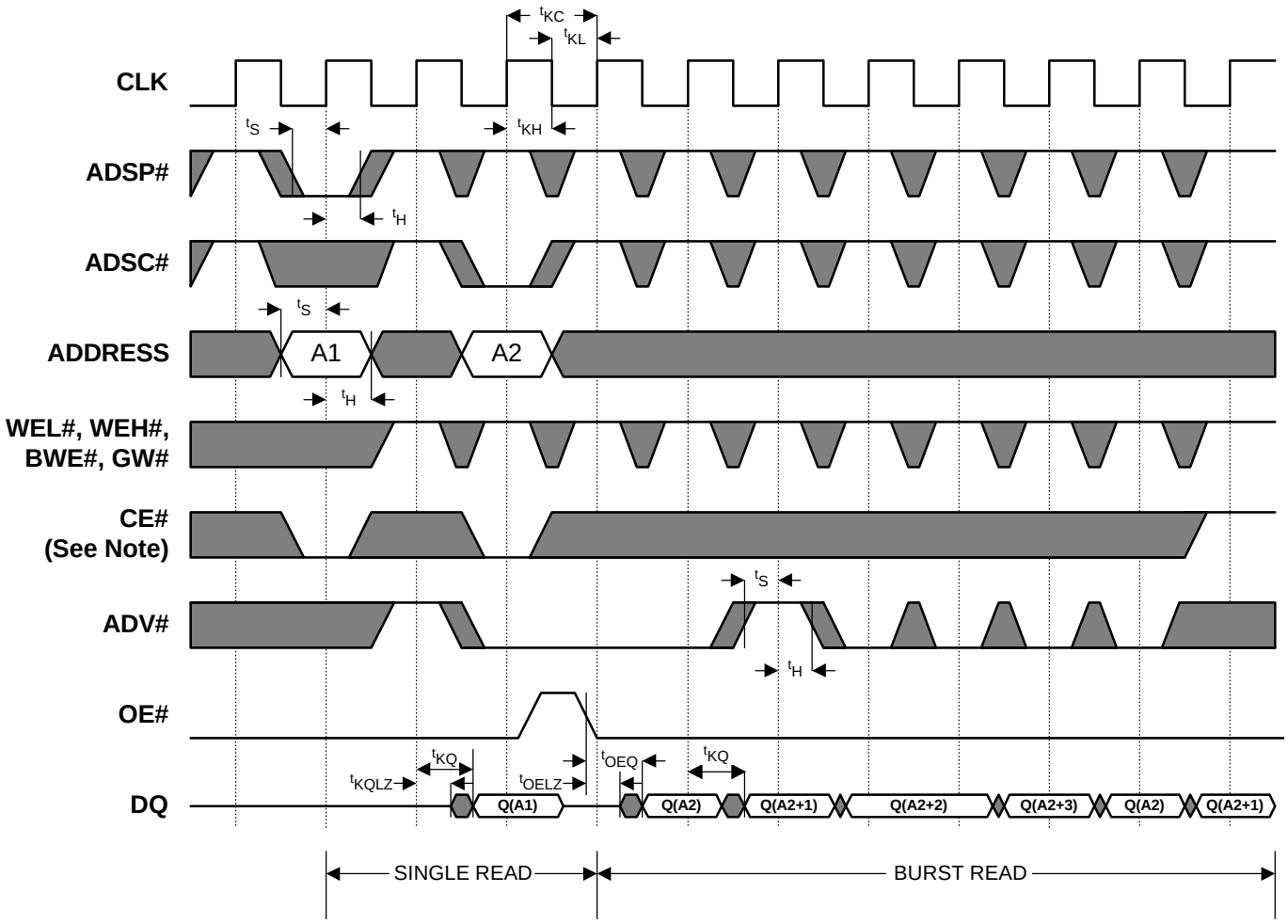


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

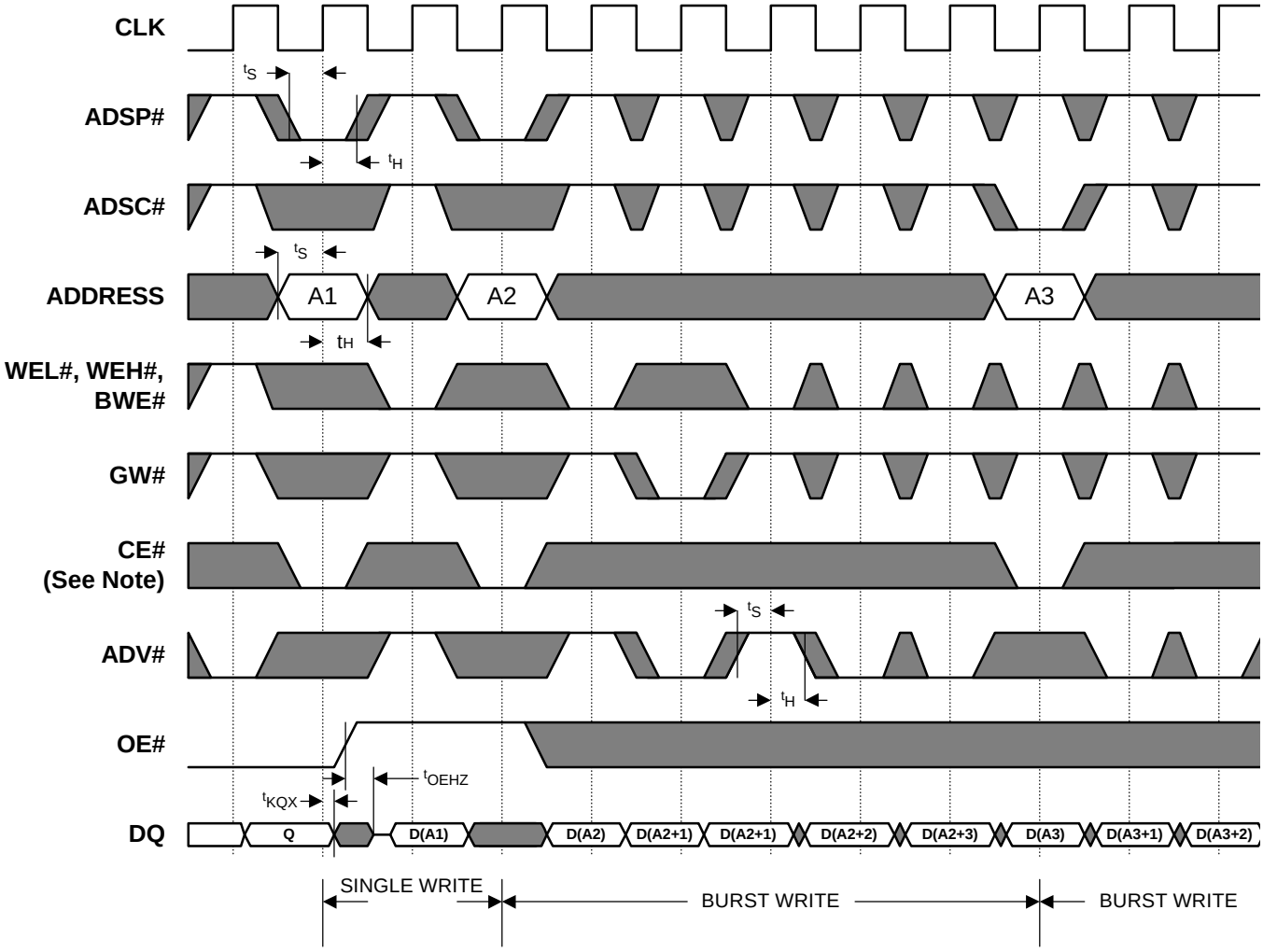
1. All voltages referenced to VSS (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tKC/2$.
   Undershoot: $V_{IL} \leq -2.0V$ for $t \leq {}^tKC/2$
3. I_{cc} is given with no output current. I_{cc} increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL=5pF as in Fig. 2.
7. At any given temperature and voltage condition, ${}^tKQHZ$ is less than ${}^tKQLZ$ and ${}^tOEHZ$ is less than ${}^tOELZ$.
8. A READ cycle is defined by byte write enables all HIGH or ADSP# LOW along with chip enables being active for the required setup and hold times. A WRITE cycle is defined by one byte or all byte WRITE per READ/WRITE TRUTH TABLE.
9. OE# is a “don’t care” when a byte write enable is sampled LOW.
10. This is a synchronous device. All synchronous inputs must meet specified setup and hold time, except for “don’t care” as defined in the truth table.
11. AC I/O curves are available upon request.
12. “Device Deselected” means the device is in POWER -DOWN mode as defined in the truth table. “Device Selected” means the device is active.
13. Typical values are measured at 3.3V, 25°C and 8.5ns cycle time.
14. MODE pin has an internal pull-up and ZZ pin has an internal pull-down. These two pins exhibit an input leakage current of ±30 µA.
15. Capacitance derating applies to capacitance different from the load capacitance shown in Fig. 1.

READ TIMING



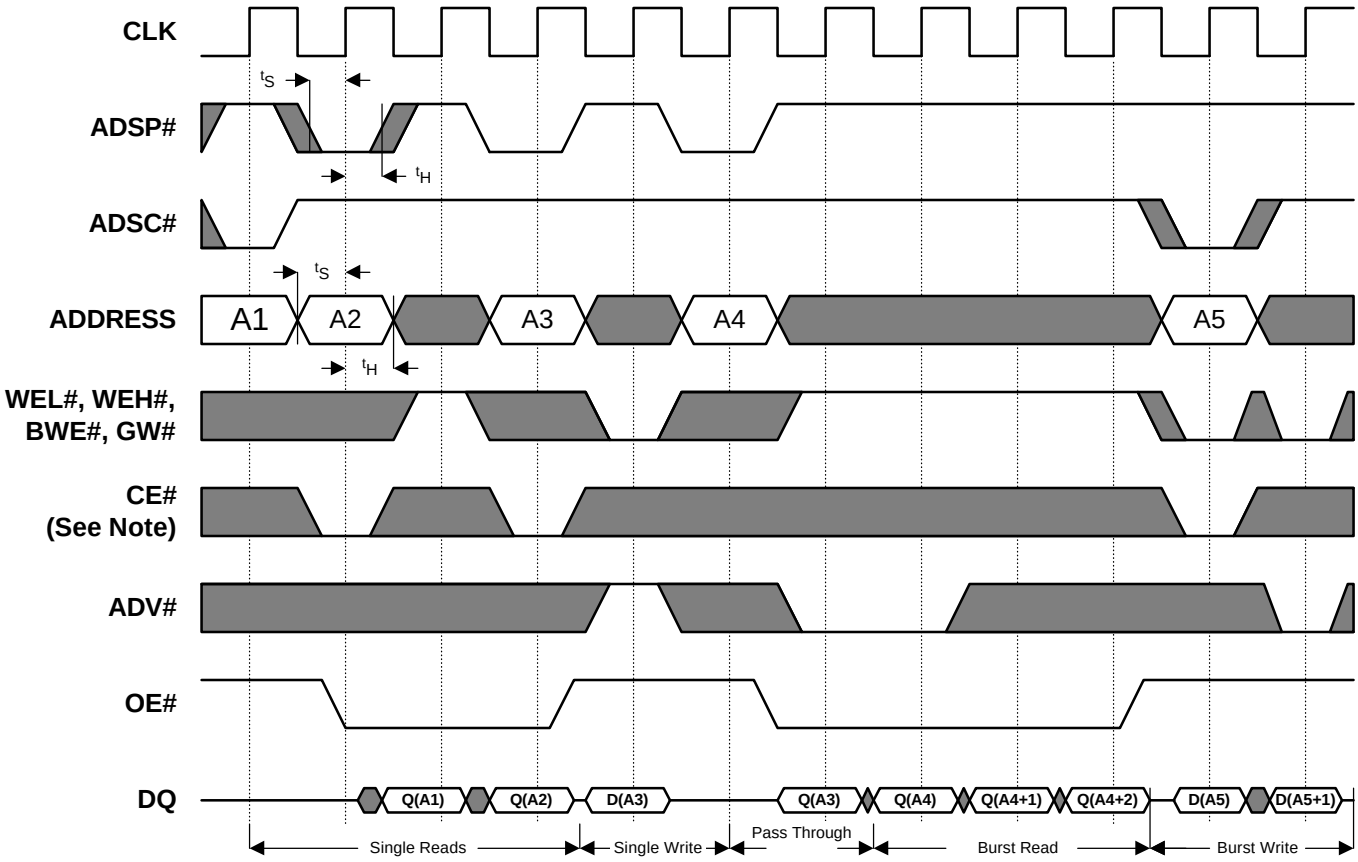
Note: CE# active in this timing diagram means that all chip enables CE#, CE2, and CE2# are active.

WRITE TIMING



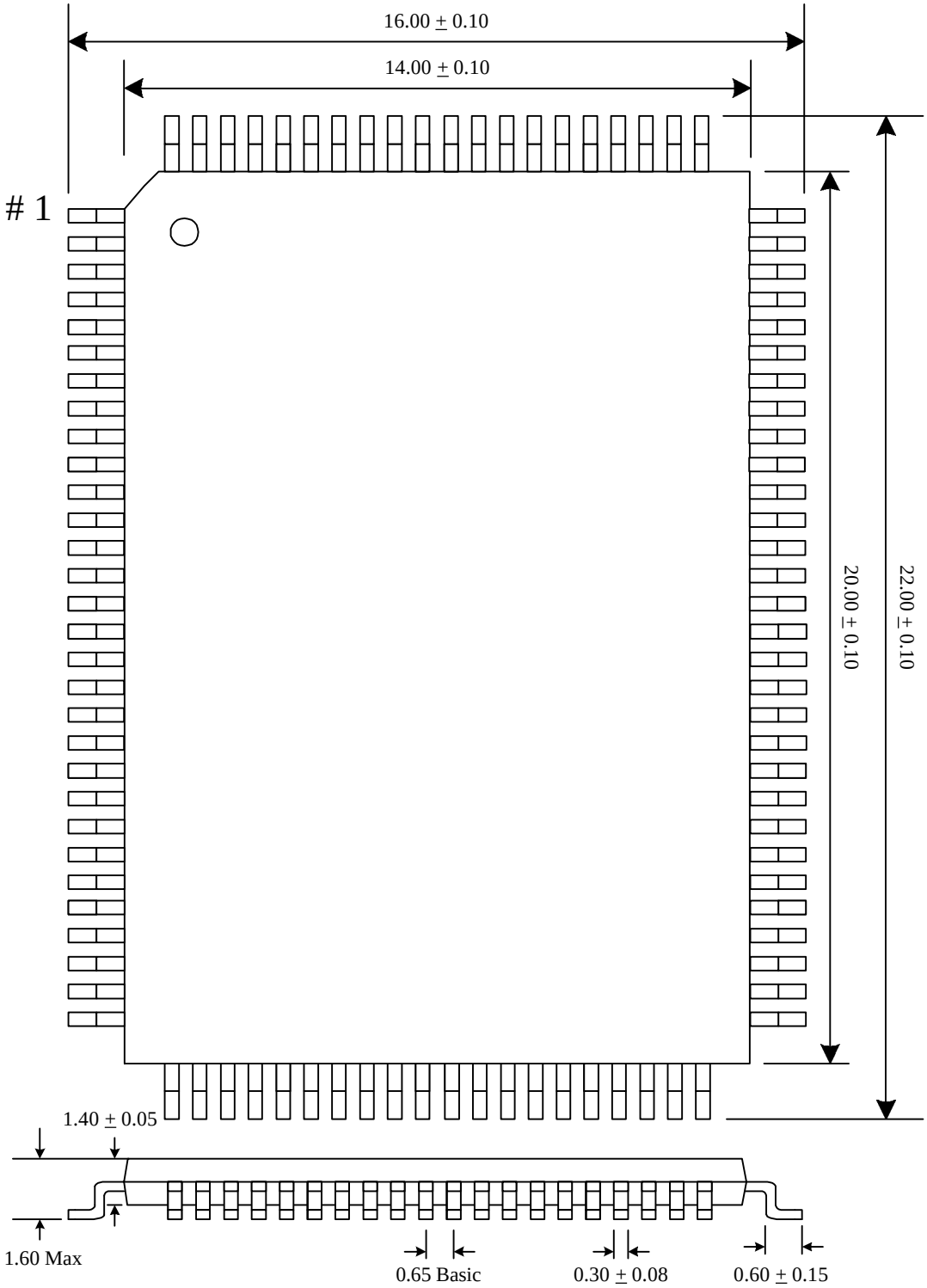
Note: CE# active in this timing diagram means that all chip enables CE#, CE2, and CE2# are active.

READ/WRITE TIMING



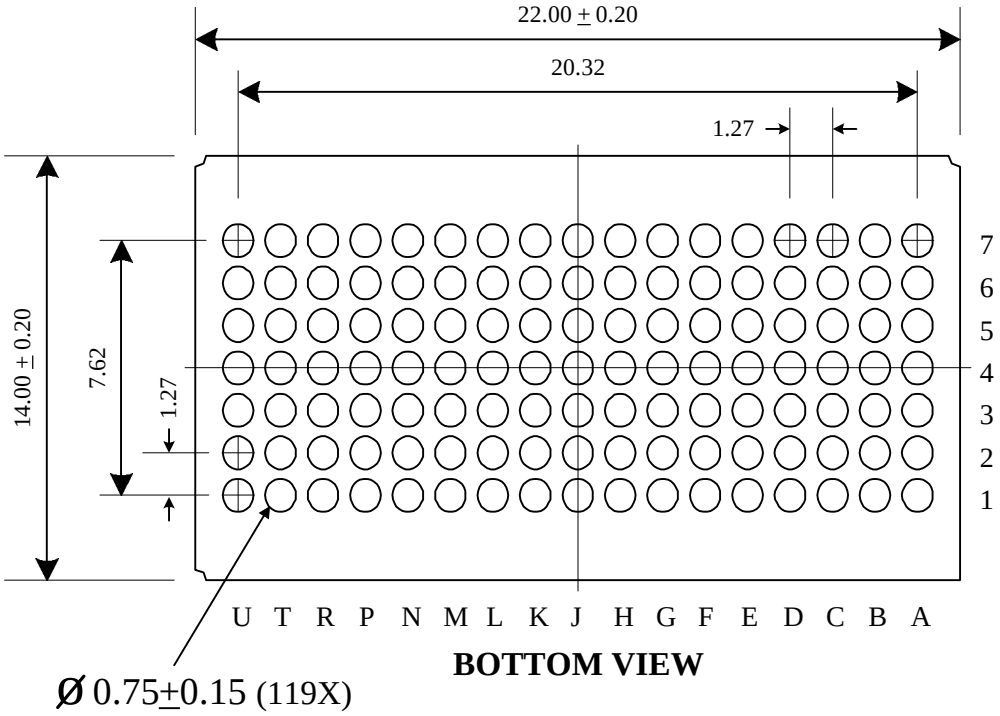
Note: CE# active in this timing diagram means that all chip enables CE#, CE2, and CE2# are active.

100 Pin TQFP Package Dimensions

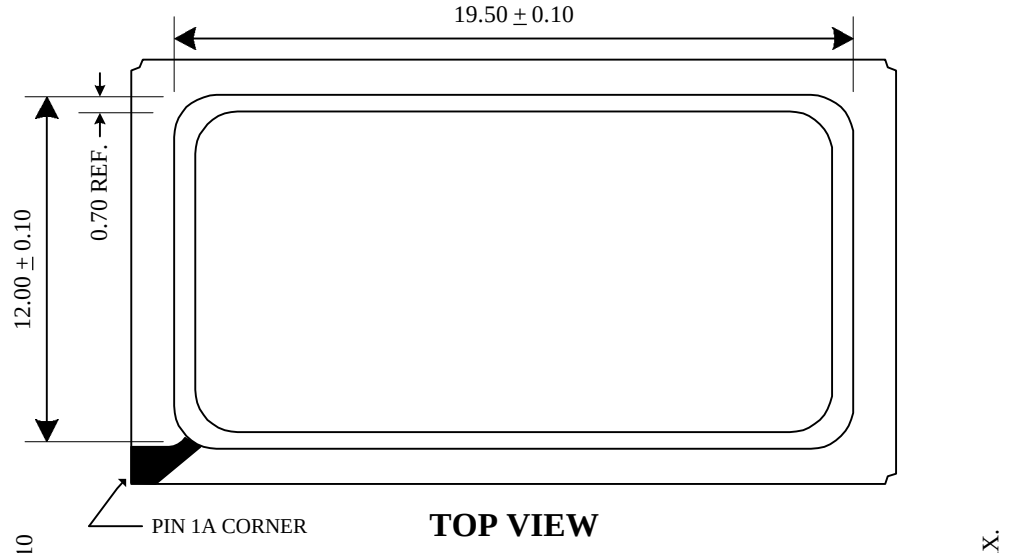


Note: All dimensions in Millimeters

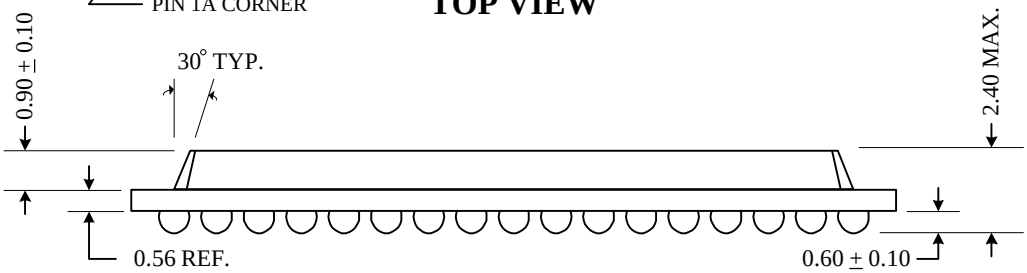
7 x 17 (119-lead) BGA Dimensions



BOTTOM VIEW



TOP VIEW



SIDE VIEW

Note: All dimensions in Millimeters

Ordering Information