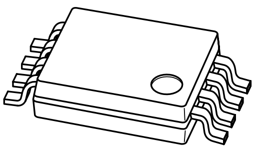


PMWD18UN

Dual N-channel µTrenchMOS ultra low level FET

Rev. 03 — 1 July 2005 Product data sheet

1. Product profile

1.1 General description

Dual common drain N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology.

1.2 Features

- Surface mounting package
- Very low threshold voltage
- Low profile
- Fast switching

1.3 Applications

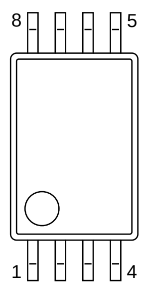
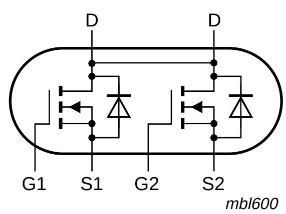
- Portable appliances
- Battery management
- Personal Computer Memory Card International Association (PCMCIA) cards
- Load switching

1.4 Quick reference data

- $V_{DS} \leq 30$ V
- $P_{tot} \leq 4.2$ W
- $I_D \leq 10.6$ A
- $R_{DSon} \leq 21.5$ mΩ

2. Pinning information

Table 1: Pinning

Pin	Description	Simplified outline	Symbol
1, 8	drain (D)	 SOT530-1 (TSSOP8)	
2, 3	source1 (S1)		
4	gate1 (G1)		
5	gate2 (G2)		
6, 7	source2 (S2)		

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3. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
PMWD18UN	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 4.4 mm	SOT530-1

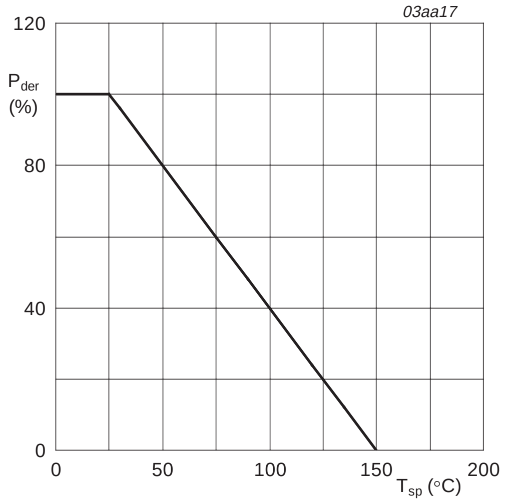
4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

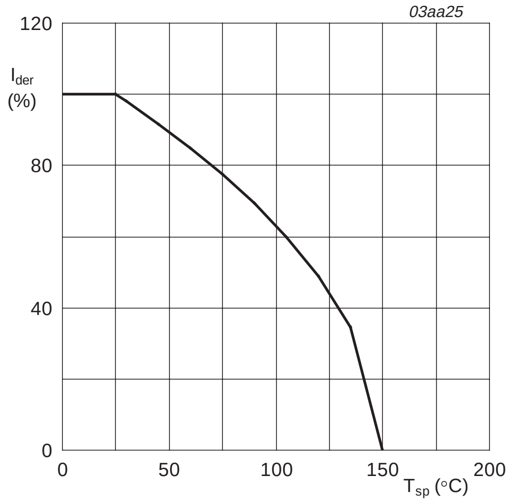
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 150 °C		-	30	V
V_{DGR}	drain-gate voltage (DC)	25 °C ≤ T_j ≤ 150 °C; R_{GS} = 20 kΩ		-	30	V
V_{GS}	gate-source voltage			-	±12	V
I_D	drain current	T_{sp} = 25 °C; V_{GS} = 4.5 V; see Figure 2 and 3	[1]	-	10.6	A
		T_{sp} = 100 °C; V_{GS} = 4.5 V; see Figure 2	[1]	-	6.8	A
I_{DM}	peak drain current	T_{sp} = 25 °C; pulsed; t_p ≤ 10 µs; see Figure 3	[1]	-	42.2	A
P_{tot}	total power dissipation	T_{sp} = 25 °C; see Figure 1	[1]	-	4.2	W
T_{stg}	storage temperature			–55	+150	°C
T_j	junction temperature			–55	+150	°C
Source-drain diode						
I_S	source current	T_{sp} = 25 °C	[1]	-	3.5	A
I_{SM}	peak source current	T_{sp} = 25 °C; pulsed; t_p ≤ 10 µs	[1]	-	14	A

[1] Single device conducting.



$$P_{der} = \frac{P_{tot}}{P_{tot(25\ ^{\circ}C)}} \times 100\ \%$$

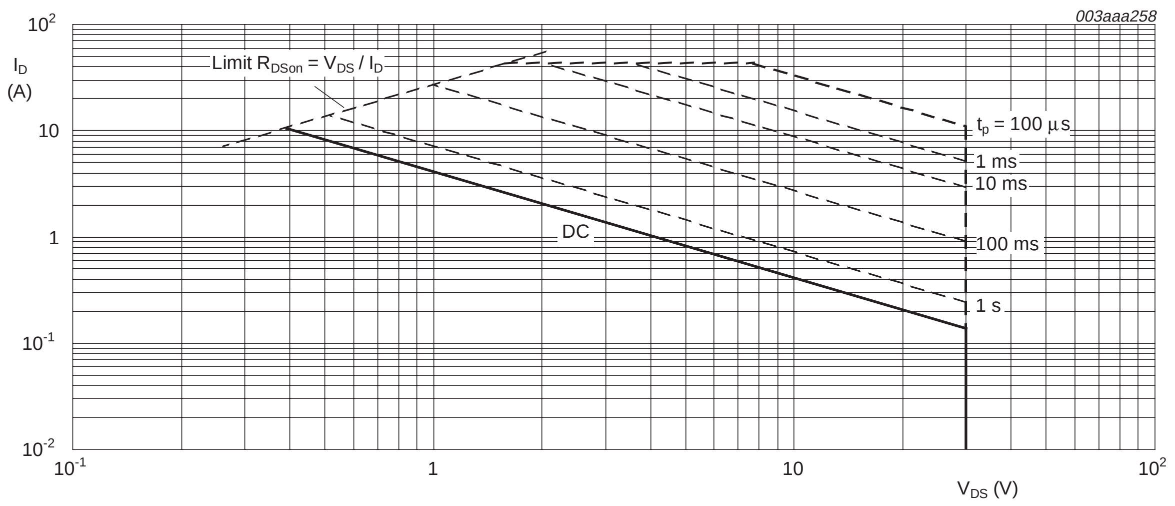
Fig 1. Normalized total power dissipation as a function of solder point temperature



$V_{GS} \geq 4.5$ V

$$I_{der} = \frac{I_D}{I_{D(25\ ^{\circ}C)}} \times 100\ \%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature



$T_{sp} = 25$ °C; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	see Figure 4	-	-	30	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	[1]	-	100	-	K/W

[1] Mounted on a printed-circuit board; minimum footprint; vertical in still air.

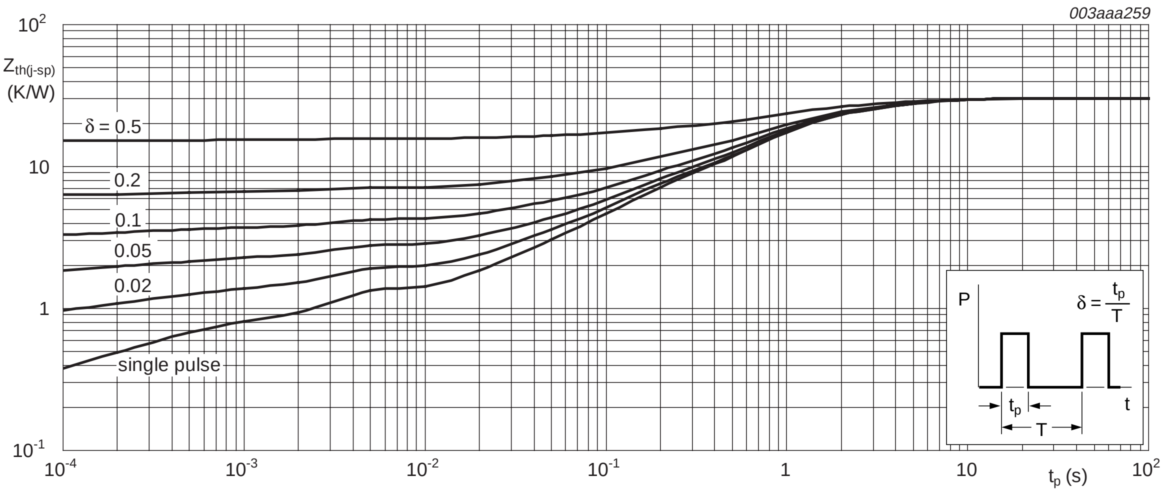


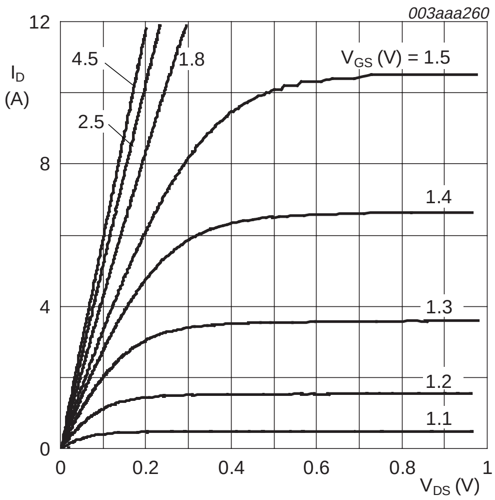
Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

6. Characteristics

Table 5: Characteristics

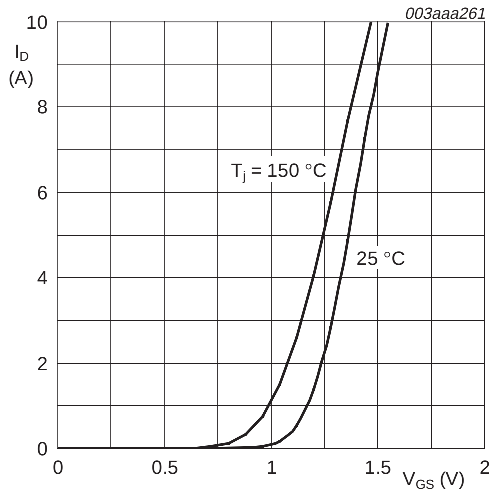
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V				
		T_j = 25 °C	30	-	-	V
		T_j = –55 °C	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; see Figure 9 and 10	0.45	0.7	-	V
I_{DSS}	drain leakage current	V_{DS} = 30 V; V_{GS} = 0 V				
		T_j = 25 °C	-	-	1	µA
		T_j = 150 °C	-	-	100	µA
I_{GSS}	gate leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	-	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 5 A; see Figure 7 and 8				
		T_j = 25 °C	-	18	21.5	mΩ
		T_j = 150 °C	-	31	37	mΩ
		V_{GS} = 1.8 V; I_D = 4.5 A; see Figure 7 and 8	-	24	35	mΩ
		V_{GS} = 2.5 V; I_D = 5 A; see Figure 7 and 8	-	20	23.5	mΩ
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 4 A; V_{DS} = 16 V; V_{GS} = 4.5 V; see Figure 13	-	24.7	-	nC
Q_{GS}	gate-source charge		-	2.2	-	nC
Q_{GD}	gate-drain charge		-	6.4	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 16 V; f = 1 MHz; see Figure 11	-	1526	-	pF
C_{oss}	output capacitance		-	210	-	pF
C_{rss}	reverse transfer capacitance		-	160	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 10 V; R_L = 10 Ω; V_{GS} = 4.5 V; R_G = 6 Ω	-	15	-	ns
t_r	rise time		-	21	-	ns
$t_{d(off)}$	turn-off delay time		-	57	-	ns
t_f	fall time		-	26	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 5 A; V_{GS} = 0 V; see Figure 12	-	0.87	1.2	V
t_{rr}	reverse recovery time	I_S = 5 A; dI_S/dt = –100 A/µs; V_{GS} = 0 V; V_R = 30 V	-	55	-	ns
Q_r	recovered charge		-	21	-	nC



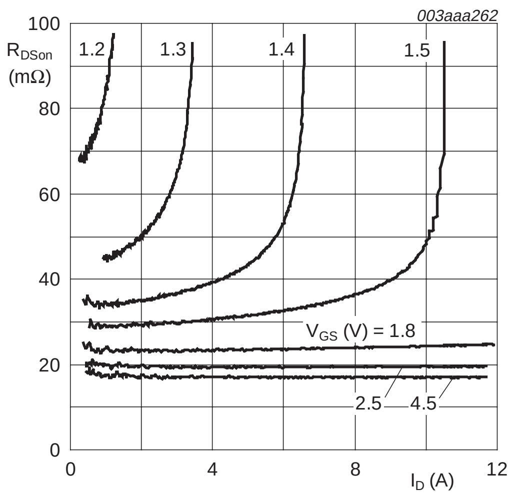
T_j = 25 °C

Fig 5. **Output characteristics: drain current as a function of drain-source voltage; typical values**



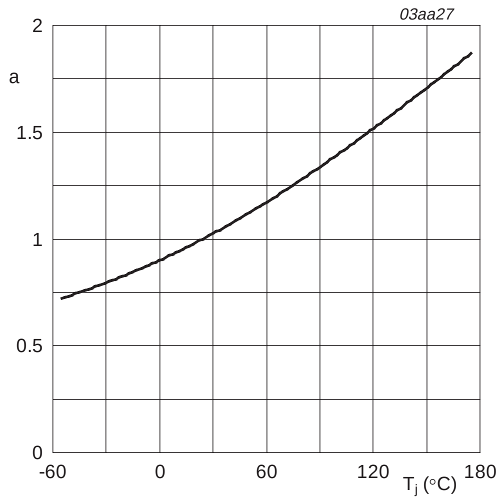
T_j = 25 °C and 150 °C; $V_{DS} > I_D \times R_{DSon}$

Fig 6. **Transfer characteristics: drain current as a function of gate-source voltage; typical values**



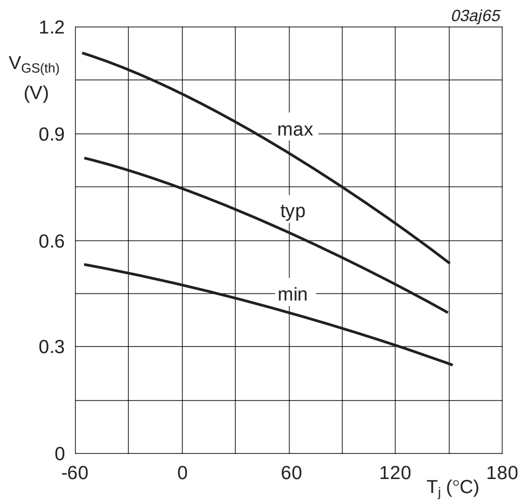
T_j = 25 °C

Fig 7. **Drain-source on-state resistance as a function of drain current; typical values**



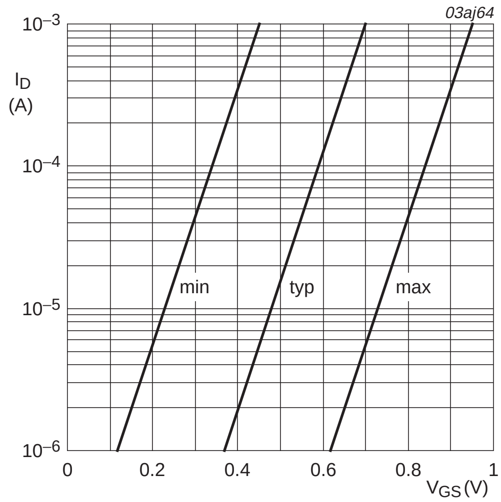
$$a = \frac{R_{DSon}}{R_{DSon(25\,^{\circ}C)}}$$

Fig 8. **Normalized drain-source on-state resistance factor as a function of junction temperature**



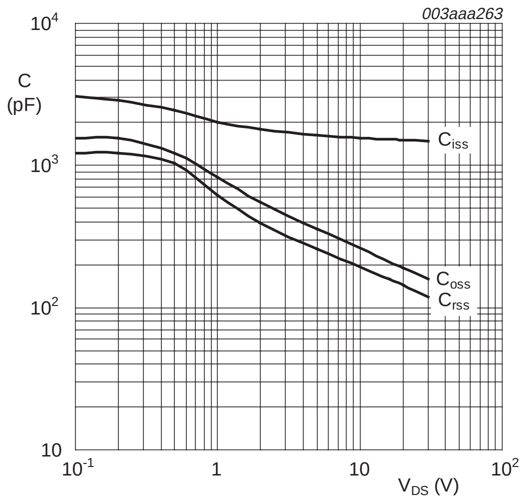
I_D = 1 mA; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



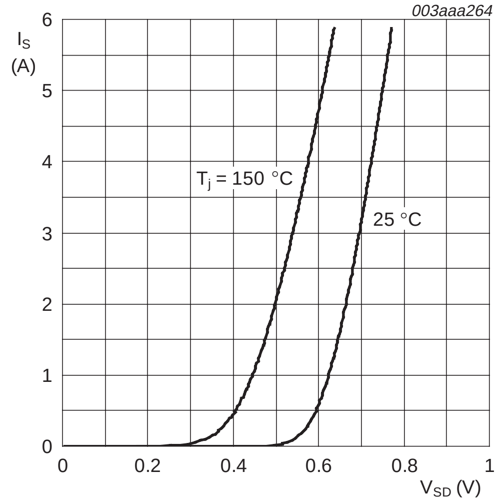
T_j = 25 °C; V_{DS} = 5 V

Fig 10. Sub-threshold drain current as a function of gate-source voltage



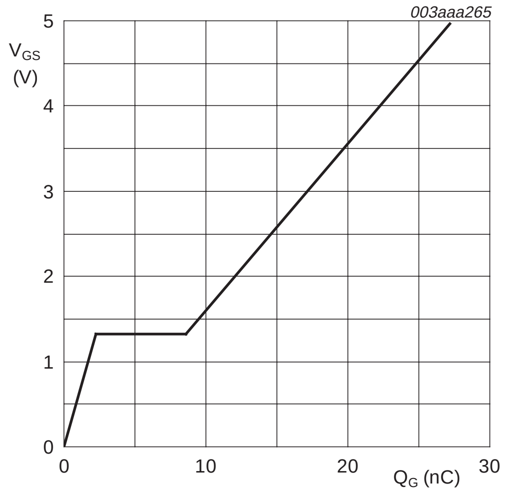
V_{GS} = 0 V; f = 1 MHz

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



T_j = 25 °C and 150 °C; V_{GS} = 0 V

Fig 12. Source current as a function of source-drain voltage; typical values

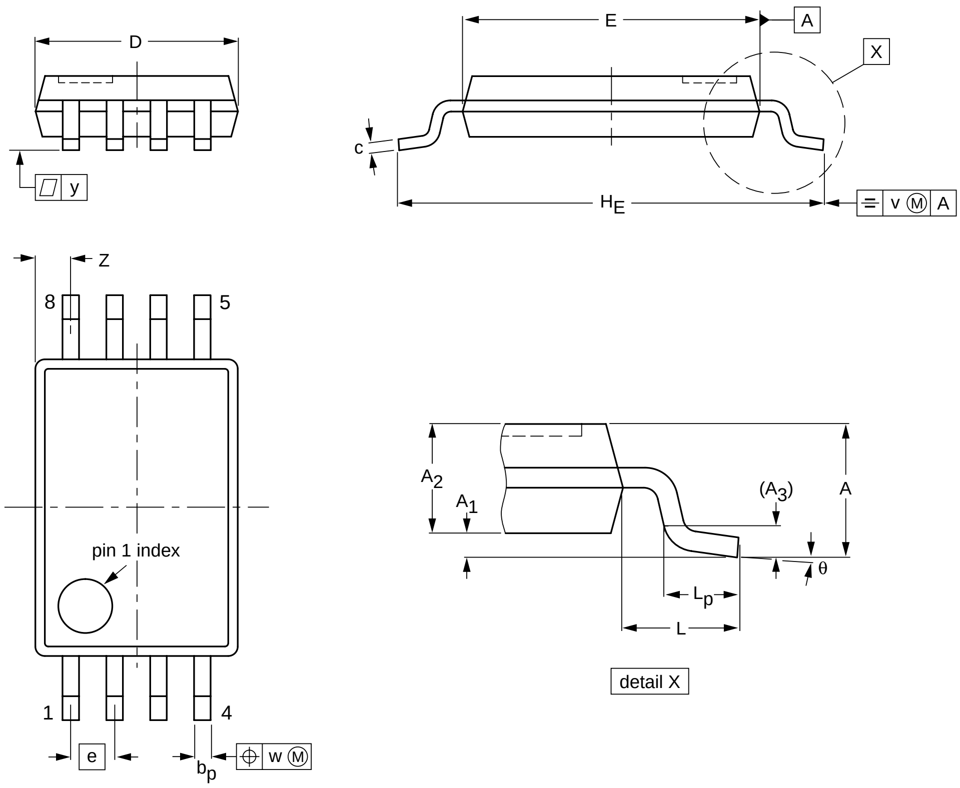


I_D = 4 A; V_{DD} = 16 V

Fig 13. Gate-source voltage as a function of gate charge; typical values

7. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 4.4 mm **SOT530-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	v	w	y	Z(1)	θ
mm	1.1	0.15 0.05	0.95 0.85	0.25	0.30 0.19	0.20 0.13	3.1 2.9	4.5 4.3	0.65	6.5 6.3	0.94	0.7 0.5	0.1	0.1	0.1	0.70 0.35	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

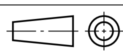
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT530-1		MO-153				~~00-02-24~~ 03-02-18

Fig 14. Package outline SOT530-1 (TSSOP8)

8. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PMWD18UN_3	20050701	Product data sheet	-	9397 750 14719	PMWD18UN-02
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • Section 1.4 “Quick reference data”: I_D and P_{tot} data revised. • Table 3 “Limiting values”: I_D, I_{DM}, P_{tot}, I_S and I_{SM} data revised. • Section 4 “Limiting values”: Figure 3 revised. • Table 4 “Thermal characteristics”: $R_{th(j-sp)}$ revised. • Section 5 “Thermal characteristics”: Figure 4 revised. • Section 6 “Characteristics”: Figure 5, 7 and 12 revised.				
PMWD18UN-02	20040223	Product data	-	9397 750 12706	PMWD18UN-01
PMWD18UN-01	20030204	Product data	-	9397 750 10832	-

9. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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14. Contents

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