

# M5296FP

**+5V CONSTANT-VOLTAGE POWER SUPPLY  
INCORPORATED WATCHDOG TIMER IC**

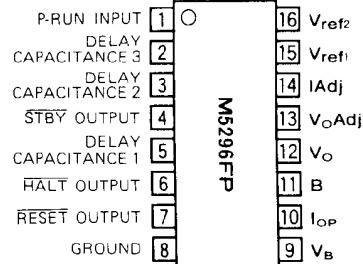
## DESCRIPTION

The M5296FP is a watchdog timer semiconductor integrated circuits which incorporates a 5V constant-voltage power supply.

To check for system failure and assure safe system operations, the M5296FP has three sequential outputs ( $\overline{\text{HALT}}$ ,  $\overline{\text{STBY}}$ , and  $\overline{\text{RESET}}$ ) and a watchdog timer output which intermittently generates a reset pulse when pulse width or cycle abnormalities are found in the clock signal from the microcomputer. (The watchdog output terminal is shared by the watchdog timer output and sequential output  $\overline{\text{RESET}}$ .)

Further, each output retains the Low reset feature at supply voltages down to 0.8V, thereby preventing system malfunctioning upon power ON.

## PIN CONFIGURATION (TOP VIEW)



Outline 16P2N-A

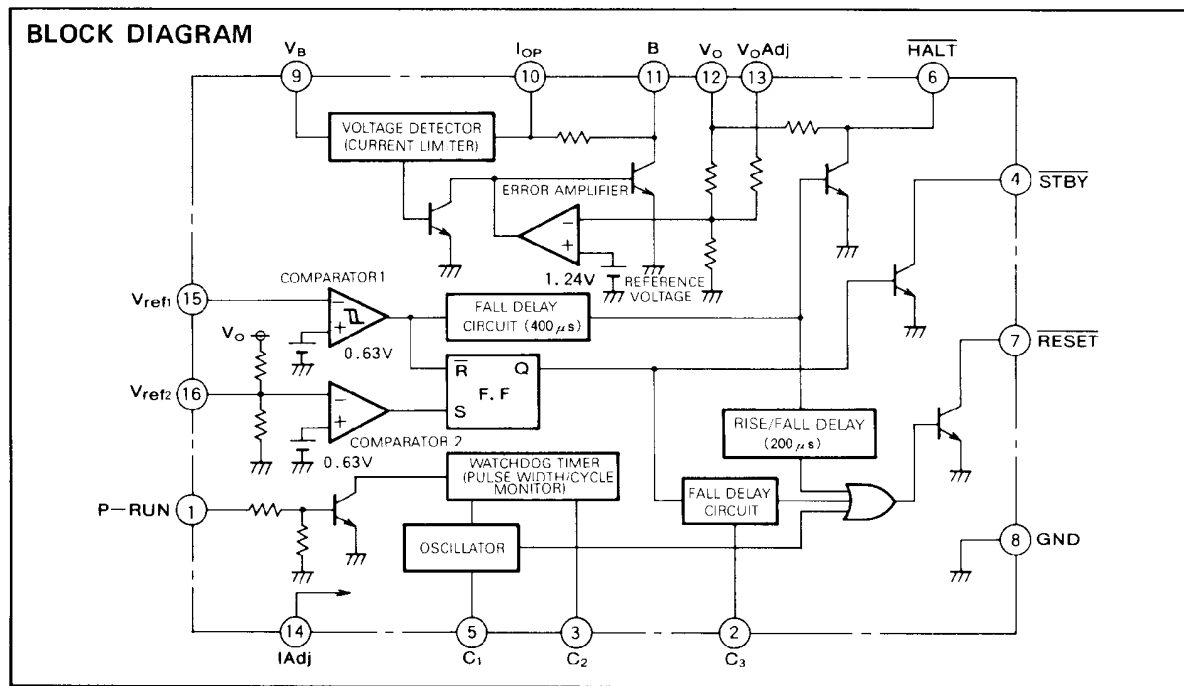
## FEATURES

- Watchdog timer (clock pulse width and cycle are monitored at the same time).
- Power ON reset timer.
- Three outputs ( $\overline{\text{HALT}}$  output for holding,  $\overline{\text{RESET}}$  output for reset, and  $\overline{\text{STBY}}$  output for return).
- Output voltage (can be fine-tuned with an external resistor)  
..... 5V  $\pm$  0.25V
- Wide supply voltage range ..... 6V~40V
- The delay time can be set using an external capacitor (the setting can be varied from about 1msec to 1sec).
- Built-in overcurrent protection circuit (which can be set up with an external resistor).

## APPLICATION

Home and industrial microcomputer systems.

## BLOCK DIAGRAM



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**ABSOLUTE MAXIMUM RATINGS** (Ta = 25°C unless otherwise noted)

Symbol	Parameter	Test conditions	Rating	Unit
V <sub>B</sub>	Supply voltage		40	V
V <sub>HALT</sub>	HALT output breakdown voltage		V <sub>O</sub>	V
V <sub>STBY</sub>	STBY output breakdown voltage		16	V
V <sub>RESET</sub>	RESET output breakdown voltage		16	V
I <sub>HALT</sub>	HALT output current		10	mA
I <sub>STBY</sub>	STBY output current		10	mA
I <sub>RESET</sub>	RESET output current		10	mA
P <sub>d</sub>	Internal power consumption		550	mW
K <sub>θ</sub>	Thermal derating	Ta ≥ 25°C	-5.5	mW/°C
T <sub>opr</sub>	Operating ambient temperature		-20 ~ +75	°C
T <sub>stg</sub>	Storage temperature		-55 ~ +125	°C

**ELECTRICAL CHARACTERISTICS** (V<sub>B</sub> = 12V, I<sub>O</sub> = 50mA, C<sub>1</sub> = 22μF, C<sub>O</sub> = 100μF, Ta = 25°C unless otherwise noted)

Symbol	Parameter	Test conditions	Rating			Unit	
			Terminal	Min	Typ		Max
I <sub>B</sub>	Bias current		⑨		9	20	mA
V <sub>O</sub>	Output voltage		⑫	4.75	5.0	5.25	V
V <sub>OM</sub>		V <sub>OAdj</sub> = 0V, V <sub>B</sub> = 6 ~ 40V	⑫			6.0	V
Reg-IN	Input stability	V <sub>B</sub> = 6 ~ 40V	⑫		0.1	0.2	%/V
Reg-L	Load stability	I <sub>O</sub> = 1 ~ 500mA	⑫		40	200	mV
V <sub>ref1</sub>	Reference voltage 1		⑮	0.56	0.63	0.68	V
V <sub>ref2</sub>	Reference voltage 2		⑯	0.56	0.63	0.68	V
ΔV <sub>TH1</sub>	Threshold voltage hysteresis width	*1 V <sub>TH1</sub> = 4.35V	⑫	20	50	100	mV
V <sub>TH2</sub>	Threshold voltage 2		⑫	2.6	3.0	3.4	V
V <sub>satH</sub>	HALT output saturation voltage	I <sub>HALT</sub> = 2mA	⑥		0.2	0.4	V
V <sub>satS</sub>	STBY output saturation voltage	I <sub>STBY</sub> = 5mA	④		0.2	0.4	V
V <sub>satR</sub>	RESET output saturation voltage	I <sub>RESET</sub> = 5mA	⑦		0.2	0.4	V
V <sub>HALT</sub>	HALT output H voltage		⑥	V <sub>O</sub> - 0.2	V <sub>O</sub> - 0.1	V <sub>O</sub>	V
I <sub>LS</sub>	STBY output leak current	V <sub>STBY</sub> = 5V	④			1	μA
I <sub>LR</sub>	RESET output leak current	V <sub>RESET</sub> = 5V	⑦			1	μA
I <sub>HALT</sub>	HALT output source current	*2	⑥	0.5	1.0	2.0	mA
I <sub>IN-P</sub>	P-RUN input current	V <sub>IN-P</sub> = 5V	①	130	200	300	μA
V <sub>IN-PH</sub>	P-RUN H input voltage		①	2.0			V
V <sub>IN-PL</sub>	P-RUN L input voltage		①			0.3	V
t <sub>1(RW)</sub>	Watchdog reset pulse width	C <sub>1</sub> = 0.15μF	⑦	35	50	70	ms
t <sub>2(RW)</sub>	Watchdog time	C <sub>1</sub> = 0.15μF, C <sub>2</sub> = 0.15μF	⑦	200	280	390	ms
t <sub>3(R)</sub>	RESET output delay time	C <sub>3</sub> = 0.068μF	⑦	55	80	115	ms
t <sub>4(H)</sub>	RESET output delay time		⑦	110	200	340	μs
t <sub>5(H)</sub>	HALT output delay time	*3	⑥	230	400	680	μs
t <sub>6(PW)</sub>	P-RUN input minimum pulse width		①	230	400	680	μs
V <sub>BMIN</sub>	V <sub>B</sub> minimum operating voltage	*4	⑨			2.0	V
V <sub>OMIN</sub>	V <sub>O</sub> minimum operating voltage	*5	⑫		0.8	1.0	V
V <sub>IP</sub>	Current limiter detection voltage	*6	⑨ ⑩	85	130	200	mV

- Note \*1: V<sub>TH1</sub> is the threshold voltage for V<sub>ref1</sub>. It is to be set up by an external resistor. The setup must be such that V<sub>TH1</sub> > V<sub>TH2</sub>.  
 \*2: A current that source when the HALT terminal is grounded in the HIGH HALT output mode (when V<sub>O</sub> is normal).  
 \*3: When Ta = -20 to +75°C, t<sub>5(H)</sub> > t<sub>4(H)</sub>.  
 \*4: The V<sub>B</sub> minimum operating voltage at which each function works.  
 \*5: The V<sub>O</sub> minimum operating voltage at which the HALT output, RESET output, and STBY output stay Low.  
 \*6: In the overcurrent operation state, the current limiter works when the external resistor (Rs) voltage (voltage developed between terminals ⑨ and ⑩) drops 130 mV (TYP) or more.

$$\text{Output peak current } I_{OP} = \frac{0.13}{R_S} \quad [\text{A}]$$

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**DEFINITION OF TERMS**

$t_{1(RW)}$  : Watchdog reset pulse width.  
 The width of an about 50% duty intermittent pulse that is generated from the  $\overline{RESET}$  terminal when the clock signal input to the P-RUN terminal has a low input level, an insufficient pulse width, an excessively long period, or other problem.

Cycle  $t = 2 \cdot t_{1(RW)}$

$t_{2(RW)}$  : Watchdog time.  
 The time for clock signal monitoring or the maximum clock cycle during which clock signal normality is detected.

$t_{3(R)}$  :  $\overline{RESET}$  output delay time.  
 The delay time from the instant the  $\overline{STBY}$  output is remove to the moment the  $\overline{RESET}$  output is remove.

$t_{4(R)}$  :  $\overline{RESET}$  output delay time.  
 The time interval between  $\overline{HALT}$  output fall/rise and  $\overline{RESET}$  output fall/rise in cases where the  $\overline{STBY}$  output is not generated (when  $V_O$  does not drop below  $V_{TH2}$ ).

$t_{5(H)}$  :  $\overline{HALT}$  output delay time.

The time interval between the instant  $V_O$  is restored to the  $V_{TH1} \pm \Delta V_{TH1}$  level and the instant the  $\overline{HALT}$  output is remove.

$t_{6(PW)}$  : P-RUN input minimum pulse width.

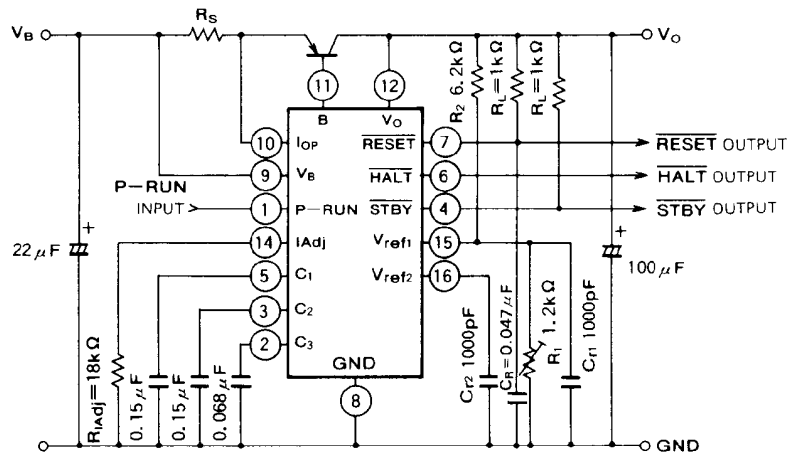
The minimum pulse width for clock signal normality detection.

$V_{IN-PH}$  : P-RUN H input voltage.

The minimum input voltage for P-RUN terminal input clock signal High level detection.

$V_{IN-PL}$  : The maximum input voltage for P-RUN terminal input clock signal Low level detection.

**APPLICATION CIRCUIT EXAMPLE**



- $C_1, C_0$  ... Necessary for oscillation prevention and input/output stabilization. Be sure that these devices are used near the IC pins.
- $R_S$  ... Required for current limiting setup. If the current limiting function is not to be exercised, short terminals ⑨ and ⑩.
- $R_{1Adj}$  ... Resistor for delay time ( $t_{1(RW)}$  to  $t_{6(PW)}$ ) setup constant current determination. A standard setting of  $18k\Omega$  should be employed.
- $R_1, R_2$  ... Resistor for threshold voltage  $V_{TH1}$  setup. For the setup procedure, see the later section entitled "PERIPHERAL CIRCUIT CONSTANT SETUP AND USAGE PRECAUTIONS."
- $C_1$  ... Necessary for watchdog reset pulse width setup.

- If the watchdog timer function is not to be used, ground terminal ⑤.
- $C_2$  ... Required for watchdog time setup. If the watchdog timer function is not to be used, ground terminal ③.
- $C_3$  ... Required for reset delay time setup for  $\overline{STBY}$  output generation ( $V_{TH2}$  detection). When terminal ② is open, the delay time for  $\overline{STBY}$  output is equal to that for  $\overline{HALT}$  output.  
 $t_{3(R)} = t_{4(R)}$
- $R_L$  ... As  $\overline{STBY}$  and  $\overline{RESET}$  are open-collector outputs, load resistor  $R_L$  is needed.
- $Cr_1, Cr_2$  ... Used when voltage detection terminals ⑮ and ⑯ are unstable due to power line noise or other factor.



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These devices are not needed when no such problems exist.

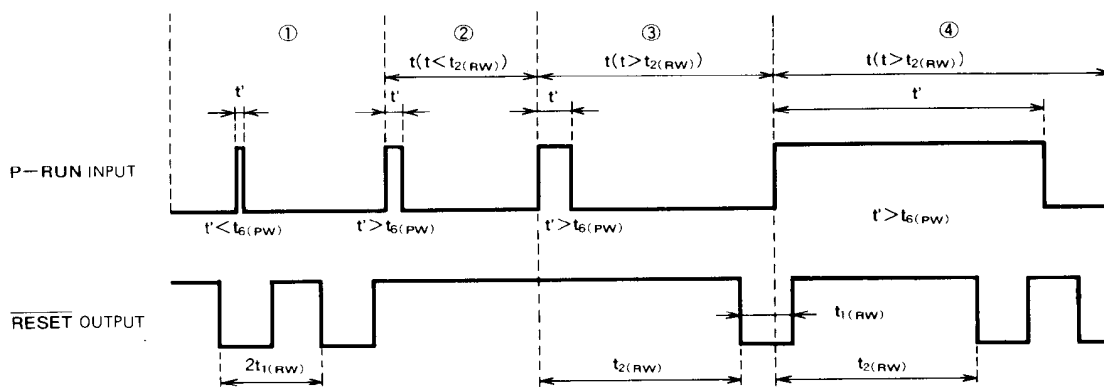
CR.....Necessary for  $\overline{\text{RESET}}$  output chattering prevention. The setup must be such that  $C_R \cdot R_L \geq 4.0 \times 10^{-5}$  (F $\cdot\Omega$ ).

**TIMING DIAGRAMS**

**1. Watchdog Timer**

When the clock signal input is not give to the P-RUN input terminal or the entered signal has pulse widths (less than

$t_{6(PW)}$ ) that are not to be detected as the clock signal, intermittent pulses (pulse width  $t_{1(RW)}$  having a duty ratio of about 50% are outputted from the  $\overline{\text{RESET}}$  terminal. When the entered clock signal has a pulse width of  $t_{6(PW)}$  or more, the  $\overline{\text{RESET}}$  intermittent operation stops and the signal goes High so that the watchdog timer (time setting:  $t_{2(RW)}$ ) actuates. If no clock signal having a pulse width of  $t_{6(PW)}$  or more is entered for a time period of  $t_{2(RW)}$  after clock signal input, the  $\overline{\text{RESET}}$  output starts an intermittent operation.

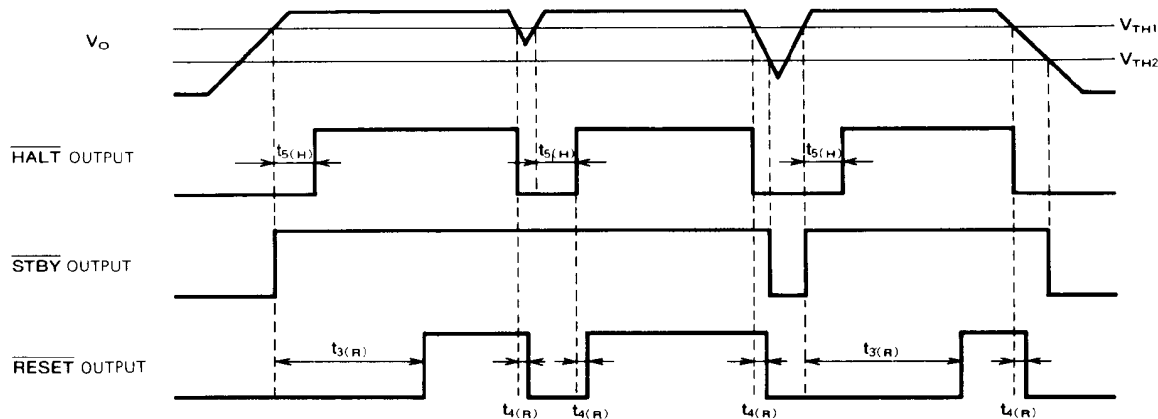


- (1) The clock signal input is give to the P-RUN input terminal. However, as the pulse width is smaller than  $t_{6(PW)}$ , the clock signal input is not detected as a signal so that  $\overline{\text{RESET}}$  generates intermittent pulsing.
- (2) As the signal input has a pulse width of  $t_{6(PW)}$  or more, the  $\overline{\text{RESET}}$  intermittent operation stops and the High output is generated. Further, as the clock signal cycle is not longer than the watchdog time  $t_{2(RW)}$ ,  $\overline{\text{RESET}}$  keeps its High output.
- (3)  $\overline{\text{RESET}}$  maintains its High output by performing the same operations as indicated in paragraph (2) above.

However, as the clock signal cycle is rendered longer than the watchdog time  $t_{2(RW)}$ ,  $\overline{\text{RESET}}$  starts an intermittent operation.

- (4) The  $\overline{\text{RESET}}$  intermittent operation starts  $t_{2(RW)}$  after clock signal input due to the same operations as indicated in paragraph (3) above. Even if the clock signal input is fed while the  $\overline{\text{RESET}}$  level is Low with intermittent operations performed,  $\overline{\text{RESET}}$  does not immediately go High so that the Low pulse width ( $t_{1(RW)}$ ) is assured.

**VOLTAGE MONITORING TIMING DIAGRAM (P-RUN INPUT NORMALITY)**



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**2. Voltage Monitoring Timing Diagram (P-RUN Input Normality)**

**HALT** output

When  $V_O$  drops below the threshold voltage  $V_{TH1}$ ,  $\overline{HALT}$  generates a Low level.  $\overline{HALT}$  is reset  $t_{5(H)}$  after  $V_O$  is restored to the  $V_{TH1} \pm \Delta V_{TH1}$  level.

**STBY** output

When  $V_O$  drops below the threshold voltage  $V_{TH2}$  ( $V_{TH2} < V_{TH1}$ ),  $\overline{STBY}$  generates a Low level. When  $V_O$  is restored to the  $V_{TH1}$  level,  $\overline{STBY}$  is reset.

**RESET** output

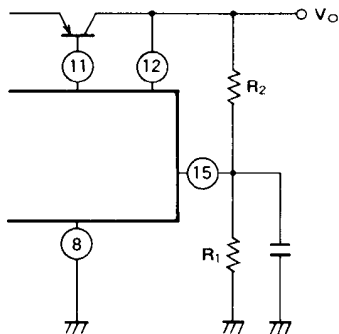
When the decreased  $V_O$  level is between  $V_{TH2}$  and  $V_{TH1}$  ( $V_{TH2} < V_O < V_{TH1}$ ),  $\overline{RESET}$  output generation takes place  $t_{4(R)}$  after  $\overline{HALT}$  fall/rise. When  $V_O$  is lower than  $V_{TH2}$ ,  $\overline{RESET}$  rise occurs  $t_{3(R)}$  after  $\overline{STBY}$  rise.

However,  $t_{3(R)} > t_{5(H)}$ .

**PERIPHERAL CIRCUIT CONSTANT SETUP AND USAGE PRECAUTIONS**

**1. Threshold Voltage Setup**

As indicated in the timing diagram on the preceding page, the M5296FP checks for output voltage decrease on the basis of two preset values (threshold voltages 1 and 2 [ $V_{TH1}$  and  $V_{TH2}$ ]).  $V_{TH1}$  can be set as desired with an external resistor (however,  $V_{TH1} > V_{TH2}$ ).  $V_{TH2}$  is set to 3.0V Typ by the built-in resistor; however, it is possible to raise it slightly using the  $V_{ref2}$  terminal.



In the above circuit,  $V_{TH1}$  is calculated as follows.

$$V_{TH1} = 0.63 \times \frac{R_1 + R_2}{R_1} \quad (\text{V})$$

For  $V_{TH1}$  detection purposes, hysteresis is provided to avoid operation instability which may be caused by noise ripple or other factor, and its value is as indicated below.

$$\Delta V_{TH1} \approx 7 \times \frac{R_1 + R_2}{R_1} \quad (\text{mV})$$

NOTE 1:  $V_{TH1}$  must be set up so that  $V_{TH1} > V_{TH2}$ .

NOTE 2: If malfunctioning occurs due to noise or other problem, connect an about 1000pF capacitor between terminals ⑮ and GND to assure stable operations.

**2. Delay Time Setup**

The M5296FP uses an external capacitor to set up three different delay times (watchdog reset pulse width  $t_{1(RW)}$ , watchdog time  $t_{2(RW)}$ , and  $\overline{RESET}$  output delay time  $t_{3(R)}$ ).

**(1)  $t_{1(RW)}$  Setup**

When the clock signal input to the P-RUN terminal is abnormal, intermittent pulsing having a duty ratio of about 50% is generated from the  $\overline{RESET}$  terminal.

The oscillation cycle  $2 \cdot t_{1(RW)}$  is to be set up using  $C_1$  as indicated below.

$$2 \cdot t_{1(RW)} = 6.72 \times 10^5 \times C_1 \quad (\text{s})$$

**(2)  $t_{2(RW)}$  Setup**

The watchdog time  $t_{2(RW)}$  is used for clock signal monitoring purposes. It denotes the clock signal cycle limit. If the clock signal cycle becomes longer than  $t_{2(RW)}$ , intermittent pulses preset by  $C_1$  are generated from the  $\overline{RESET}$  terminal. The value  $t_{2(RW)}$  is to be set up by  $C_2$ .

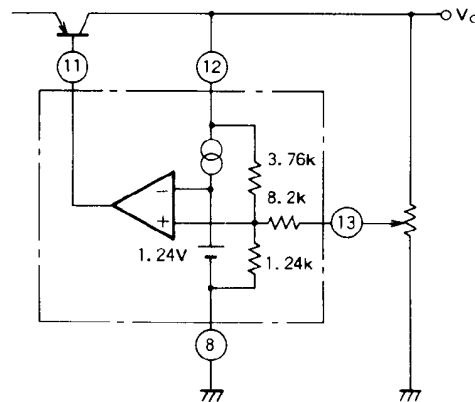
$$t_{2(RW)} = t_{1(RW)} + 1.53 \times 10^6 \times C_2 \quad (\text{s})$$

**(3)  $t_{3(R)}$  Setup**

The  $\overline{RESET}$  output delay time  $t_{3(R)}$  refers to the elapsed time from the instant the  $\overline{STBY}$  output is reset to the moment  $\overline{RESET}$  output is reset. It is to be set up by  $C_3$ .

$$t_{3(R)} = 1.18 \times 10^6 \times C_3 \quad (\text{s})$$

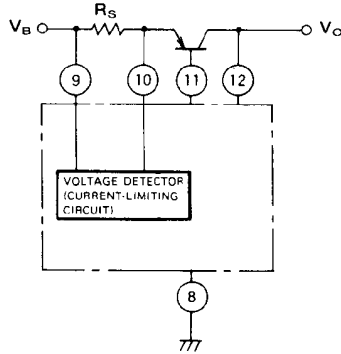
**3. Output Voltage  $V_O$  Adjustment**



As shown above, the  $V_{OAdj}$  terminal permits output voltage fine adjustment. However, as a  $8.2k\Omega$  resistor is series-connected to the  $V_{OAdj}$  terminal, the approximate adjustment range is from -20% to +10%.

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**4. Overcurrent Protection Setup  
( $I_O$  Peak Current Setup)**



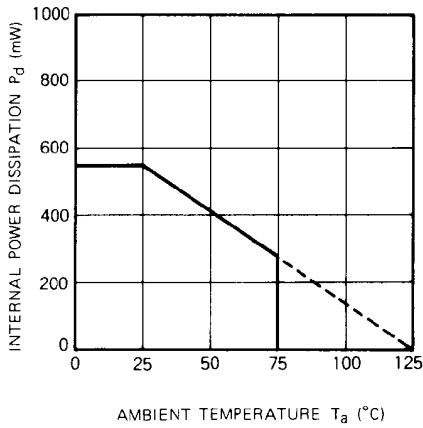
In the circuit shown at left, the load current flowing through the detection resistor  $R_S$  is detected as a voltage value (detection voltage: 130mV) for current limiting purposes.

$$I_{OP} \doteq \frac{130(\text{mV})}{R_S(\Omega)} (\text{mA})$$

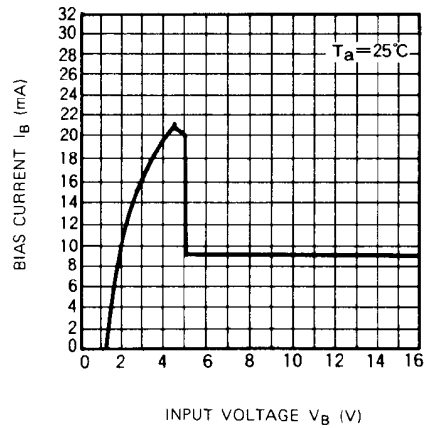
NOTE 3: The current flowing through  $R_S$  contains the IC bias current  $I_B$ . Therefore, the setup must be such that  $I_B < 130/R_S$  (mA).

**TYPICAL CHARACTERISTICS**

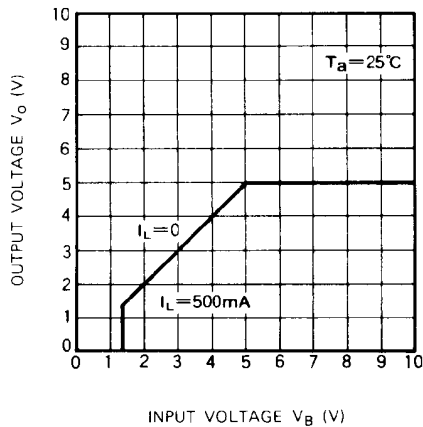
**THERMAL DERATING (MAXIMUM RATING)**



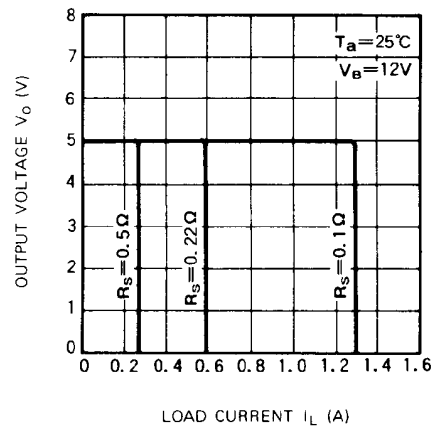
**BIAS CURRENT VS. INPUT VOLTAGE**



**OUTPUT VOLTAGE ( $V_O$ ) VS. INPUT VOLTAGE ( $V_B$ )**

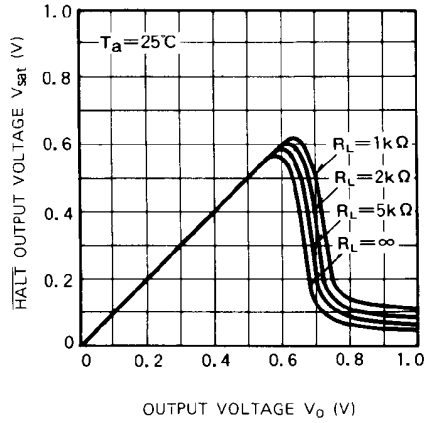


**OUTPUT VOLTAGE ( $V_O$ ) VS. LOAD CURRENT ( $I_L$ )**

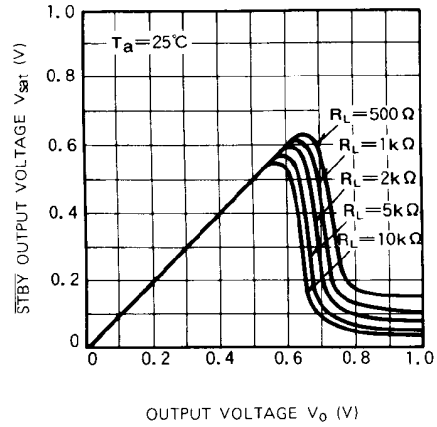


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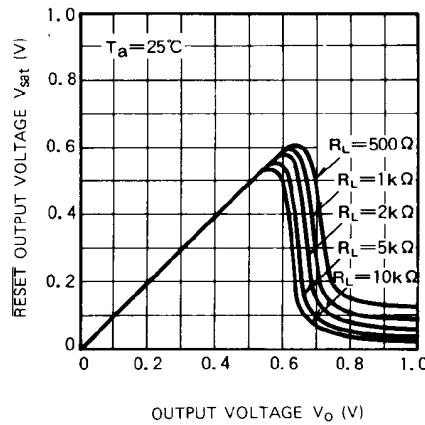
**CRITICAL OPERATION VOLTAGE CHARACTERISTICS**



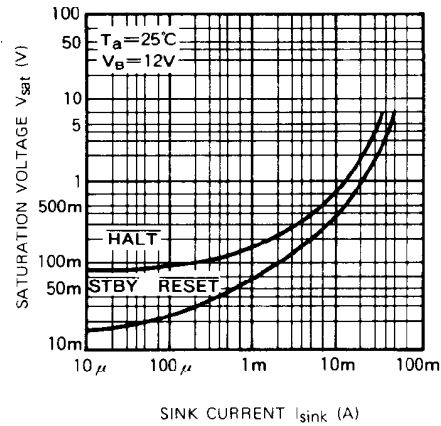
**CRITICAL OPERATION VOLTAGE CHARACTERISTICS**



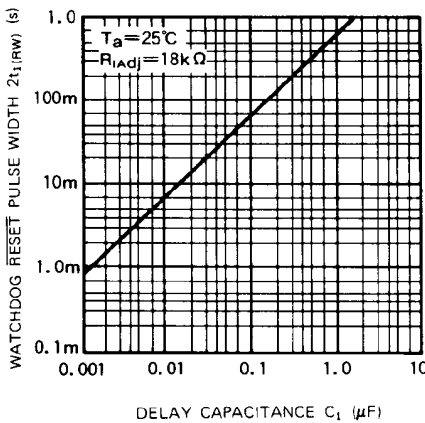
**CRITICAL OPERATION VOLTAGE CHARACTERISTICS**



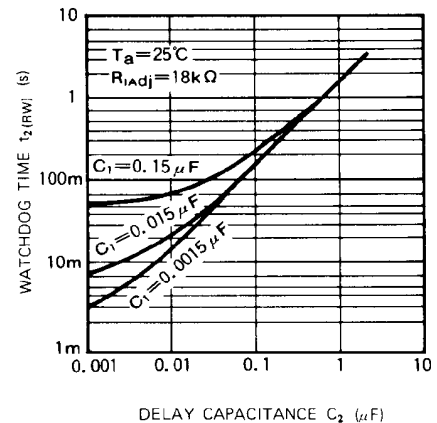
**SATURATION VOLTAGE VS. SINK CURRENT**



**WATCHDOG RESET PULSE WIDTH VS. DELAY CAPACITANCE**

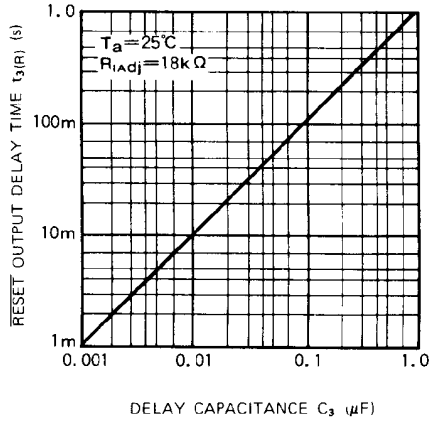


**WATCHDOG TIME VS. DELAY CAPACITANCE**

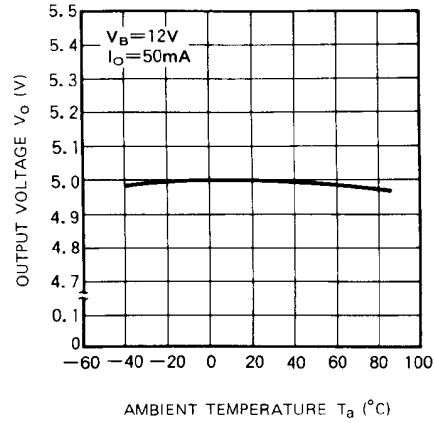


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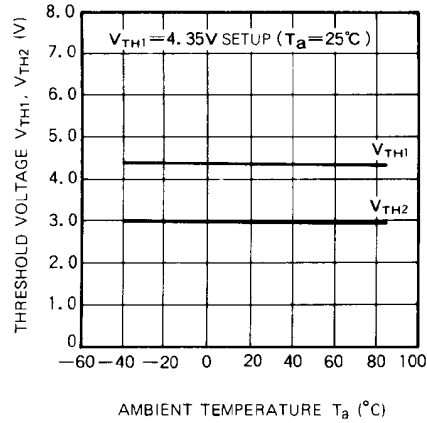
**RESET OUTPUT DELAY TIME VS. DELAY CAPACITANCE**



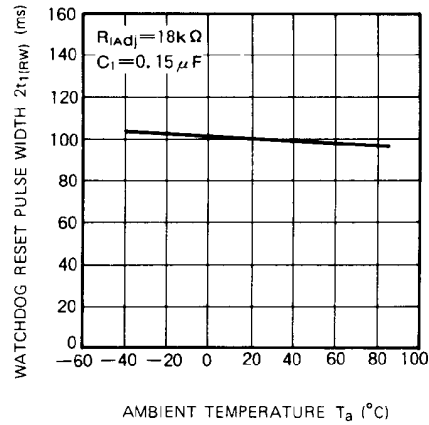
**OUTPUT VOLTAGE VS. AMBIENT TEMPERATURE**



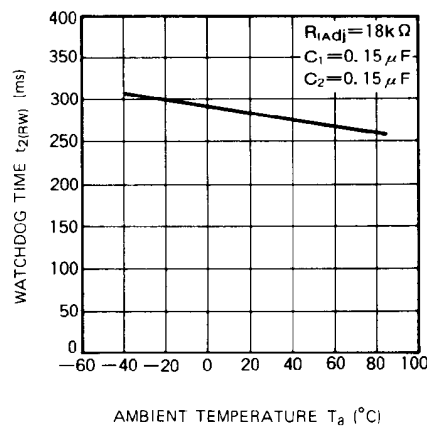
**THRESHOLD VOLTAGE VS. AMBIENT TEMPERATURE**



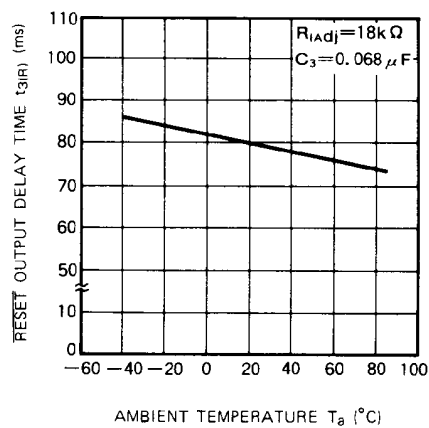
**WATCHDOG RESET PULSE WIDTH VS. AMBIENT TEMPERATURE**



**WATCHDOG TIME VS. AMBIENT TEMPERATURE**



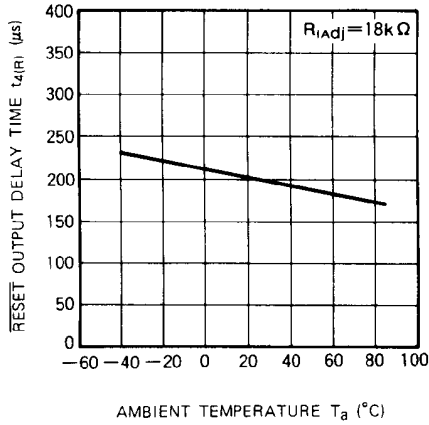
**RESET OUTPUT DELAY TIME VS. AMBIENT TEMPERATURE**



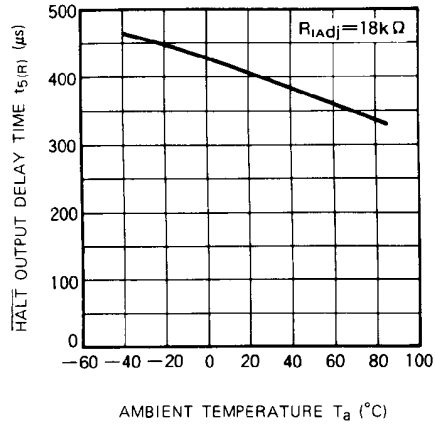


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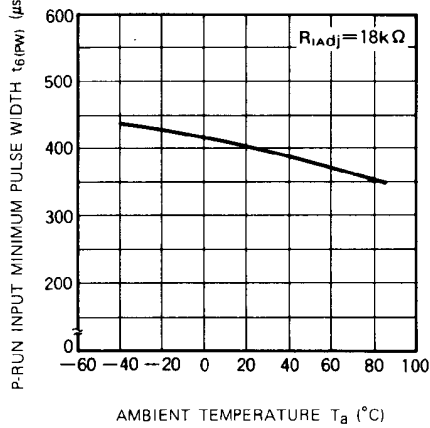
**RESET OUTPUT DELAY TIME VS. AMBIENT TEMPERATURE**



**HALT OUTPUT DELAY TIME VS. AMBIENT TEMPERATURE**



**P-RUN INPUT MINIMUM PULSE WIDTH VS. AMBIENT TEMPERATURE**



**BIAS CURRENT VS. AMBIENT TEMPERATURE**

