M5290P,FP

±5V TRACKING REGULATOR WITH RESET CIRCUIT

DESCRIPTION

M5290 is a semiconductor integrated circuit designed for voltage regulator which is dual tracking type (positive/negative output voltage) with system reset circuit.

Since the output voltage is fixed inside, User can omit the outside resistors, and this IC includes the system reset circuit for detecting the abnormal status of Power Supply. When Power Supply of system is in abnormal status, this IC sends the system reset output (Low) to the MPU/CPU, so User can make the system operate safely.

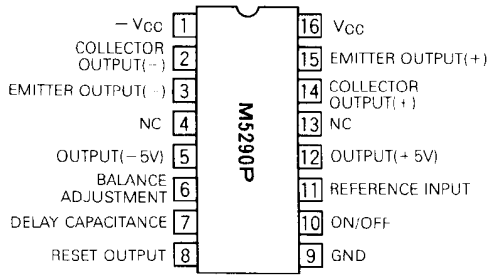
FEATURES

- High input voltage ..... $V_I = \pm 20V$
- Fixed output voltage ..... $V_O = \pm 5V$
- Internal system reset circuit (with hysteresis)
  detectable voltage 4.2V
  (deray time is variable by connecting capacity at 7pin (6pin for the FP))
- Current limiting circuit, thermal protection circuit
- Capable of ON/OFF control (10pin)
- Very Low input-output voltage differential operation by using transistor
- Variable output voltage (with external resistors connected between terminals ⑪ and GND and between positive output terminals).

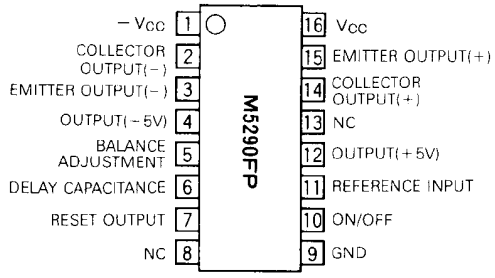
APPLICATION

Dual power supply for CD players and stereo set pre-/main-amplifiers

PIN CONFIGURATION (TOP VIEW)



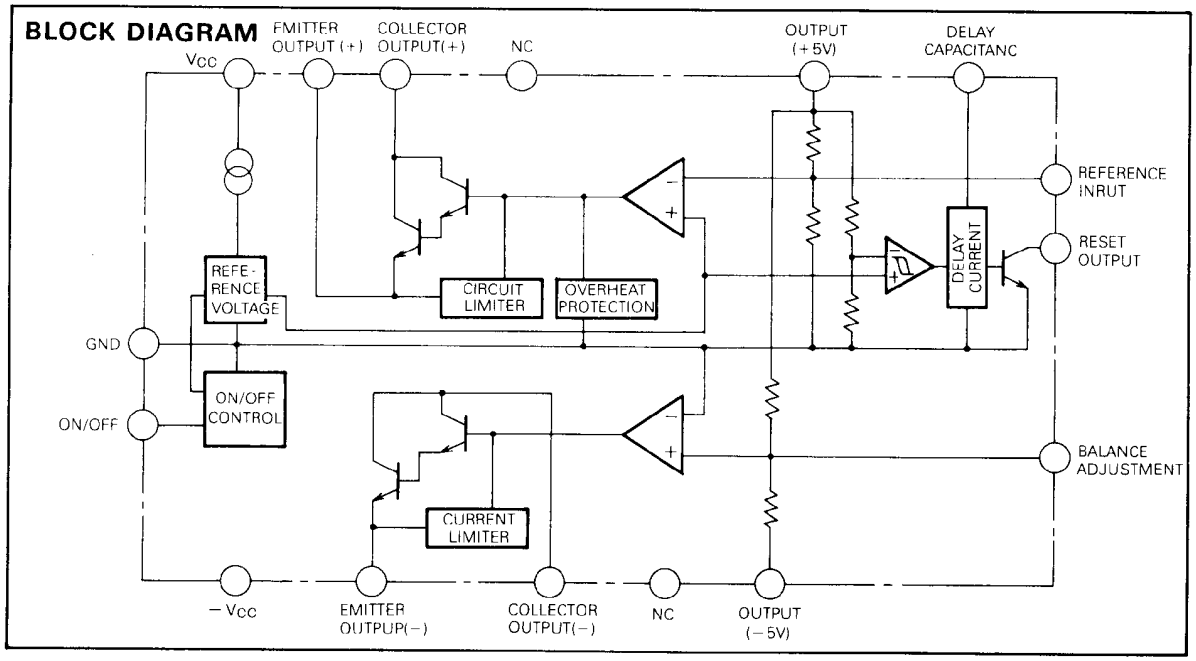
Outline 16P4



NC: NO CONNECTION

Outline 16P2S-A

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

±5V TRACKING REGULATOR WITH RESET CIRCUIT

ABUSOLUTE MAXIMUM RATINGS (Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		±20(40)	V
I_{LP}	Load current		±30	mA
V_{DIF}	Input/Output Voltage difference		±15(30)	V
Pd	Power dissipation		1.0(P)/0.55(FP)	W
K_θ	Thermal derating	Ta≧25℃	10.0(P)/5.5(FP)	mW/℃
Topr	Ambient temperature		−20 ~ +75	℃
Tstg	Storage temperature		−55 ~ +125	℃

ELECTRICAL CHARACTERISTICS (Ta = 25℃, V_{CC} = ±8V, I_L = ±10mA, unless otherwise noted)

Symbol	Rarameter	Test condition	Limits			Unit
			MIN	TYP	MAX	
I_{CC}	Circuit current		—	3.0	6.0	mA

REGULATOR PART

Symbol	Parameter	Test conditions	Limits			Unit
			MIN	TYP	MAX	
V_{IN}	Input voltage		$\pm V_O \pm 2$	—	±20	V
V_O	Output voltage		±4.75	±5.0	±5.25	V
V_{REF}	Reference input voltage		1.15	1.20	1.25	V
$\triangle V_O$	Dual voltage tracking		—	0.5	2	%
R.R	Ripple rejection	C_{REF} = 1μF, f = 120Hz	50	65	—	dB
REG-in	Input voltage rejection	V_I = ±8 ~ ±18V	—	0.05	0.2	%/V
REG-I_O	Loading voltage rejection	I_{LO} = 0 ~ 20mA	—	20	100	mV
V_{NO}	Output noise voltage	f = 20Hz ~ 100kHz	—	10	—	μVrms
$V_{O(off)}$	Output cut-off voltage	10pin GND	—	—	±0.1	V

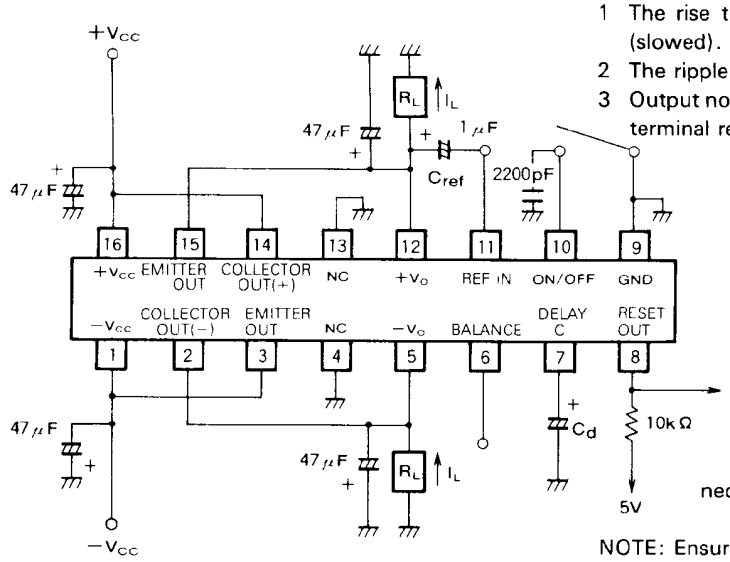
RESET PART

Symbol	Parameter	Test conditions	Limits			Unit
			MIN	TYP	MAX	
V_S	Detected voltage		3.95	4.2	4.45	V
$\triangle V_S$	Hysteresis voltage		50	100	300	mA
Tpd	Delay time	Cd = 0.1μF	3	7	14	mS
Vsat	Output saturation voltage	I_{sink} = 3mA	—	0.2	0.4	V

Note: The employed measurement circuit conforms to application circuit example (1).

APPLICATION EXAMPLE

1. Standard application example ($I_L = \pm 30mA$)



CREF

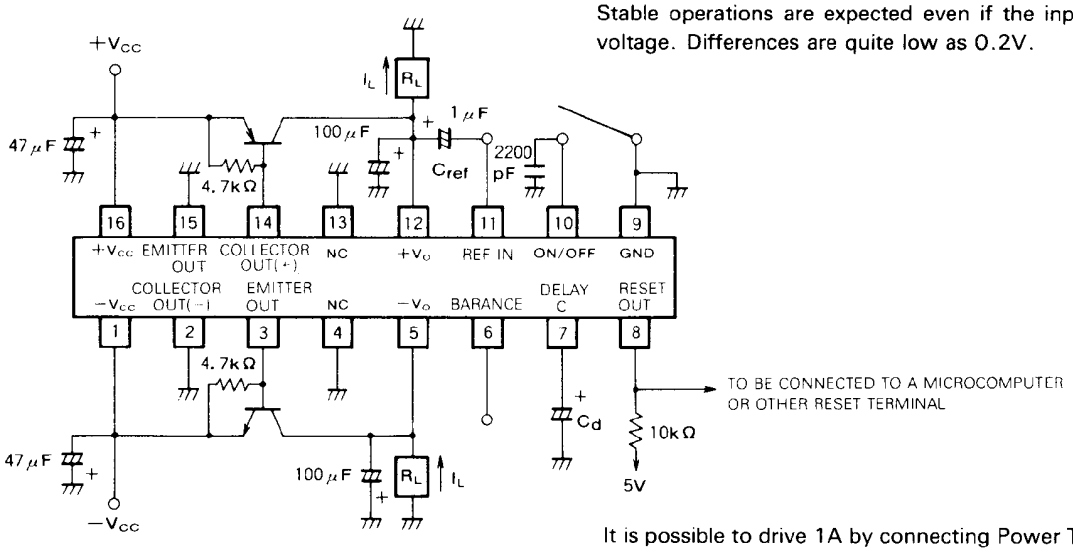
Connection of this capacitor gives the following characteristics.

1 The rise time of the output voltage can be adjusted (slowed).
2 The ripple rejection ratio is improved.
3 Output noise voltage is reduced down to 1/10 of three terminal regulator IC.

The output is cut off when 10pin is connected to the GND terminal.

NOTE: Ensure that the capacitance of the employed capacitor does not significantly vary with the temperature.

2. Very Low input-out voltage differential operation

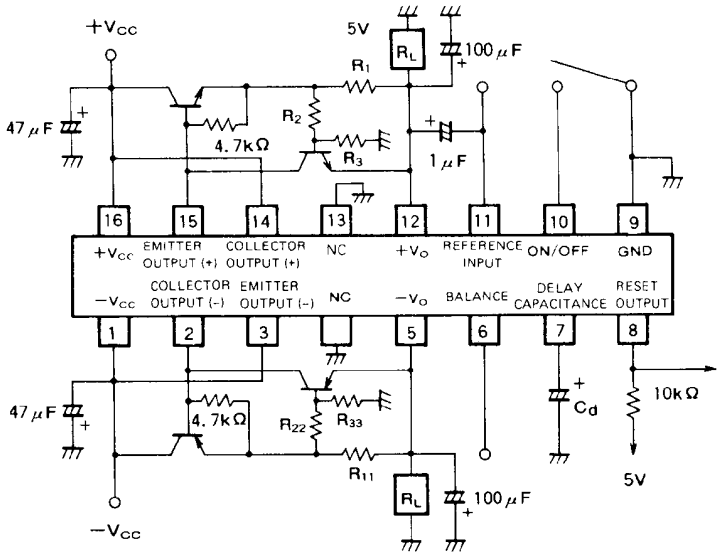


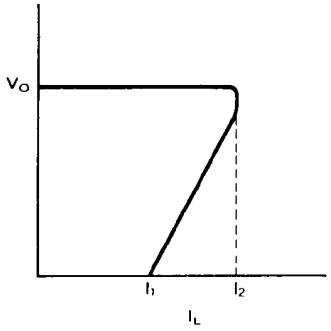
Stable operations are expected even if the input-output voltage. Differences are quite low as 0.2V.

It is possible to drive 1A by connecting Power Transistor. By shorting the 10pin to the GND, the output is shut down.

(3) Foldback Protection Circuit Application Example (M5290P Foldback System)

The input/output voltage differential V_{IO} should be adjusted to be high enough considering the voltage difference developed at R_1.





When two protective transistors are employed, the M5290P/FP can provide foldback characteristic for protection purposes. The I_1 and I_2 values are determined according to the external resistance.

$$I_1 \fallingdotseq \frac{R_2+R_3}{R_1 \cdot R_3} \times 0.65 \ (A)$$

$$I_2 \fallingdotseq I_1 + \frac{R_2}{R_1 \cdot R_3} \times 12 \ (A)$$

Cases where $I_{L(PEAK)} = I_2 \approx 500mA$ and $I_1 \approx 100mA$

$R_1 = R_{11} = 13\Omega$, $R_2 = R_{22} = 2k\Omega$, $R_3 = R_{33} = 2k\Omega$

The required input/output voltage differential is 8V or greater.