M5295AL/AP/AFP

Watchdog Timer

REJ03D0780-0200
Rev.2.00
Jun 15, 2007

Description

M5295A is a semiconductor integrated circuit which is designed for system reset to detect +5 V power supply.

This IC keeps the operation microcomputer watching. When the system is abnormal, it generates reset output until the system returns to normal states of the system.

It is possible to vary the two detective voltage by connecting the resistor, so it is suitable to high quality and high performance system.

Features

- Watchdog timer
- Power on reset timer
- Low circuit current: 0.8 mA (Typ, V_{CC} = 5 V)
- Wide supply voltage range: $V_{CC(max)}$ = 15 V

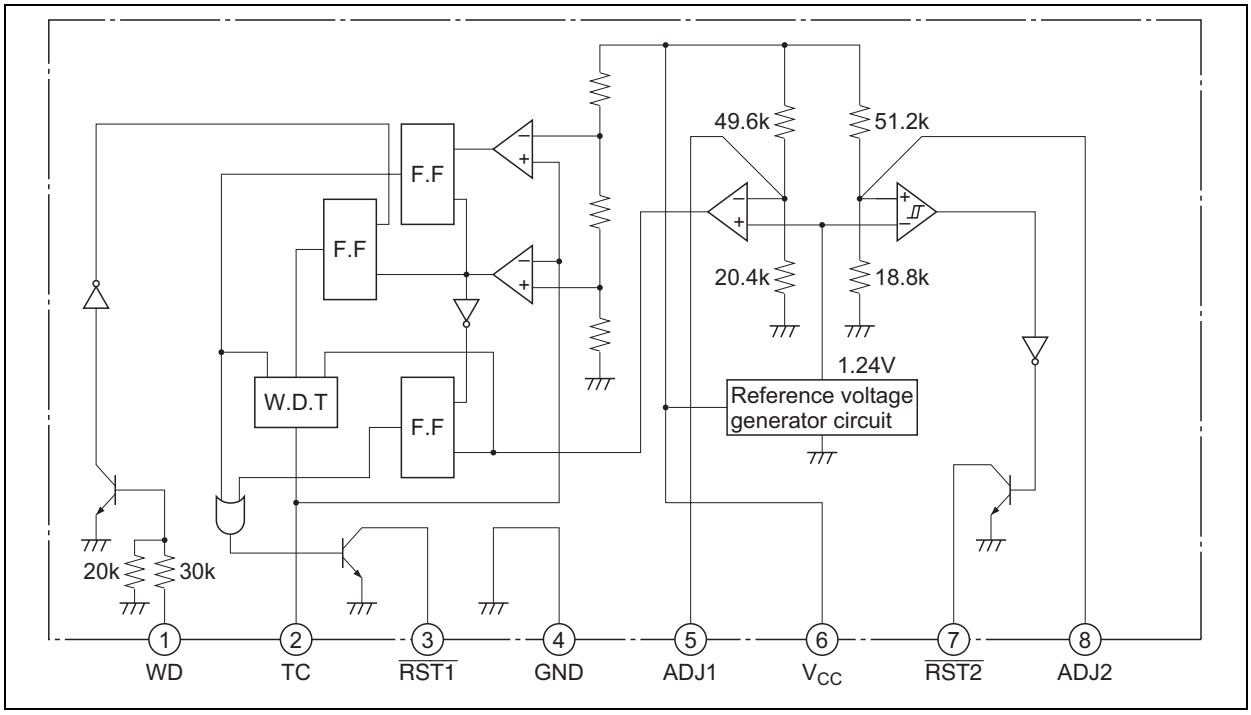
Application

- Microcomputer system

Recommended Operating Condition

- Supply voltage range: 4 V to 15 V
- Rated supply voltage: 5 V

Block Diagram



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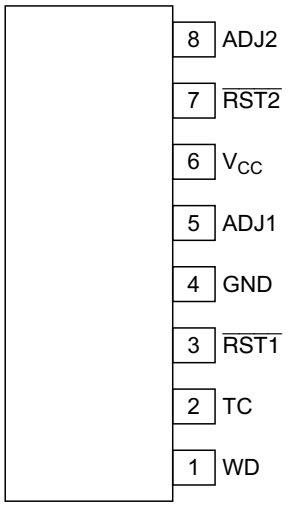
Pin Arrangement

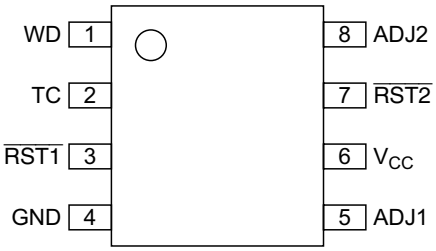
M5295AL



(Top view)

Outline: PRSS0008AA-A (8P5) [AL]

M5295AP
M5295AFP



(Top view)

Outline: PRDP0008AA-A (8P4) [AP]
PRSP0008DE-C [AFP] (recommend)
PRSP0008DA-A (8P2S-A) [AFP] (not recommend for new design)

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Absolute Maximum Ratings

(Ta = 25°C, unless otherwise noted)

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	15	V
Input voltage	V_{IN}	–10 to +10	V
Output voltage	V_{OUT}	15	V
Output current	I_{OUT}	10	mA
Power dissipation	Pd	800(AL)/625(AP)/440(AFP)	mW
Thermal derating	Kθ	8.0(AL)/6.25(AP)/4.4(AFP)	mW/°C
Operating temperature	Topr	–20 to +75	°C
Storage temperature	Tstg	–55 to +125	°C

Electrical Characteristics

(Ta = 25°C, unless otherwise noted)

DC Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	
						Pin	
WD input current	I_{IH}	0.06	0.15	0.25	mA	WD	V_{IN} = 5V
	I_{IL}	–0.05	–0.1	–0.15			V_{IN} = –5V
WD input voltage	V_{IH}	2	—	—	V	WD	
	V_{IL}	—	—	0.8			
TC output current	I_{OUT}	—	—	–1	µA	TC	V_{IN} = 1.5V
TC input current	I_{IN}	—	3.3	—	mA	TC	V_{OUT} = 4.2V
Threshold voltage of watchdog timer	$V_{TH3(H)}$	3.7	4	4.3	V	TC	
	$V_{TH3(L)}$	1.7	2	2.3			
Output voltage	V_{OL}	—	0.1	0.5	V	RST1	I_{OUT} = 1mA
Output leakage current	Ileak	—	—	5	µA	RST2	V_{OUT} = 15V
V_{CC} detective voltage (1)	V_{TH1}	4.05	4.25	4.45	V	V_{CC}	
V_{CC} detective voltage (2)	$V_{TH2(H)}$	4.5	4.7	4.9	V	V_{CC}	
	$V_{TH2(L)}$	4.45	4.6	4.75			
	ΔV_{TH2}	0.05	0.1	0.2			
ADJ1 voltage	V_5	1.17	1.46	1.75	V	ADJ1	
ADJ2 voltage	V_8	1.07	1.34	1.61	V	ADJ2	
$\overline{RST1}$ on voltage	RST1	—	—	0.5	V	RST1	V_{CC} = 1.2V, R_L = 4.7kΩ
$\overline{RST2}$ on voltage	RST2	—	—	0.5	V	RST2	V_{CC} = 1.2V, R_L = 4.7kΩ
Circuit current	I_{CC}	—	0.8	1.5	mA	V_{CC}	

DC Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	
						Pin	
Watchdog timer	T_{WD}	—	1.1·C·R_1	—	s	$\overline{RST1}$	
		0.5	1.1	1.7	ms		C = 0.1µF, R_1 = 10kΩ
Reset timer (1)	$t_{RST(1)}$	—	0.5·C·R_1	—	s	$\overline{RST1}$	
		0.2	0.5	1.1	ms		C = 0.1µF, R_1 = 10kΩ
Reset timer (2)	$t_{RST(2)}$	—	830·C	—	s	$\overline{RST1}$	R_1 = 10kΩ
		40	83	220	µs		C = 0.1µF, R_1 = 10kΩ
Input pulse watch	t_{WDIN}	3	—	—	µs	WD	
Transmittal delay time	t_{d1}	—	20	—	µs	$\overline{RST1}$	
	t_{d2}	—	10	—		$\overline{RST2}$	

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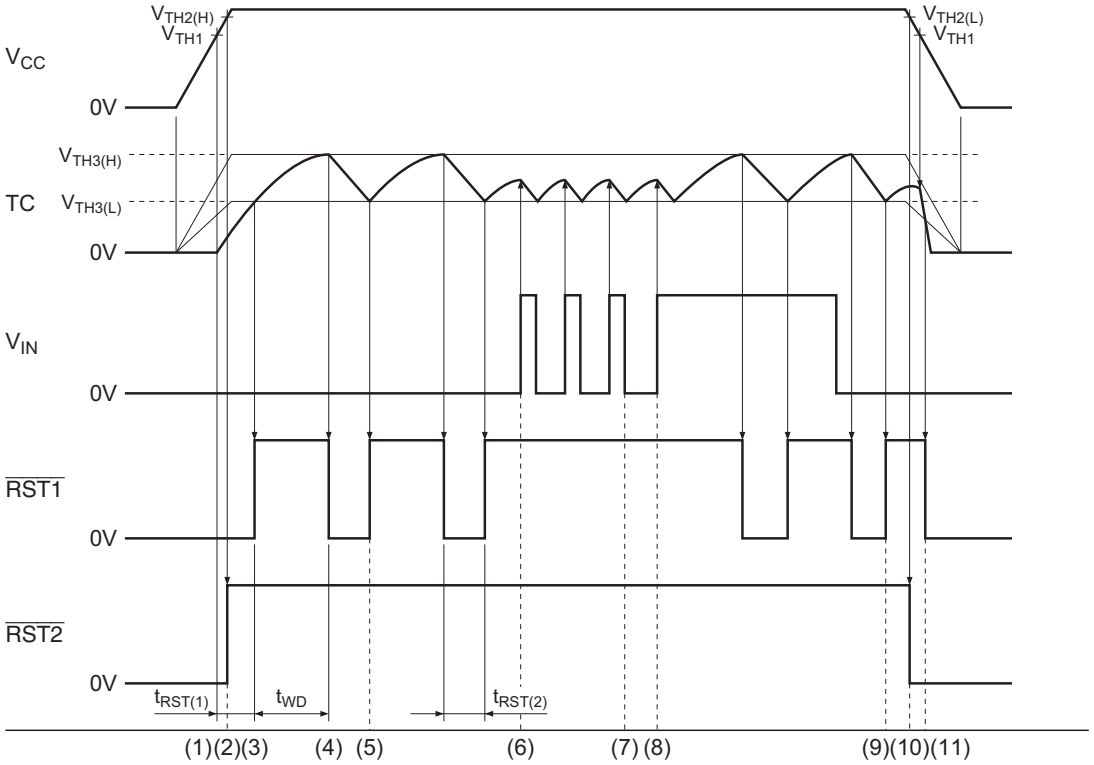
Operating Description



(1): The V_{CC} rises up to 0.8 V, then $\overline{RST1}$ and $\overline{RST2}$ generates low output, and rising up to 4.25 V, charge of C1 begins.

(2): The V_{CC} rises up to 4.7 V, then $\overline{RST2}$ generates high.

(3), (4): The voltage at TC pin is 2 V, then $\overline{RST2}$ generates high, when 4 V, C1 is discharged and $\overline{RST1}$ generates low.

(5): The voltage at TC pin falls to 2 V, then $\overline{RST1}$ generates high unless normal clock signal is entered to WD pin, $\overline{RST1}$ repeats this operation.

(6), (7): Before the voltage at TC pin reaches 4 V, if normal clock signal is entered to WD pin, low $\overline{RST1}$ is canceled.

(8), (9): In the case of entrance of abnormal signal input, as the waveform of TC pin repeats charge and discharge of $\overline{RST1}$ alternatively from 2 V to 4 V, the $\overline{RST1}$ repeats high and low output operation.

(10): The V_{CC} falls to 4.6 V, then $\overline{RST2}$ generates low, this detective voltage has a 100 mV hysteresis.

(11): When V_{CC} goes down to 4.25 V(V_{TH1}), the status of TC pin is switched to discharge. When the potentional at TC pin is detected being $V_{TH3(H)}$ or $V_{TH3(L)}$, the status of $\overline{RST1}$ becomes "low".

Terminology

$t_{RST(1)}$: Time required for TC pin potential to rise from 0 V $V_{TH3(L)}$ when V_{CC} is being applied.

t_{WD} : Time required for TC pin potential to rise from $V_{TH3(L)}$ to $V_{TH3(H)}$.

$t_{RST(2)}$: Time required for TC pin potential to go down from $V_{TH3(H)}$ to $V_{TH3(L)}$.

Figure 1 Operating Waveform

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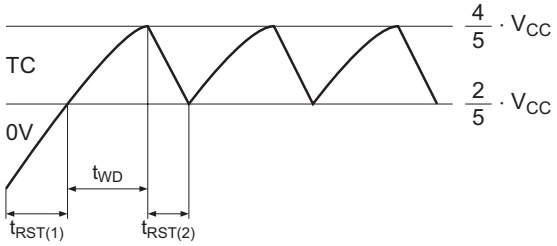
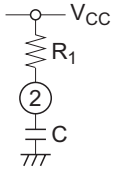
1. Pin(2) (TC pin) charge time and discharge time
   When input to WD pin is abnormal, TC pin output waveform is as shown below:



$t_{RST(1)} = 0.51 \cdot C \cdot R_1$

$t_{WD} = 1.1 \cdot C \cdot R_1$ (charge time)

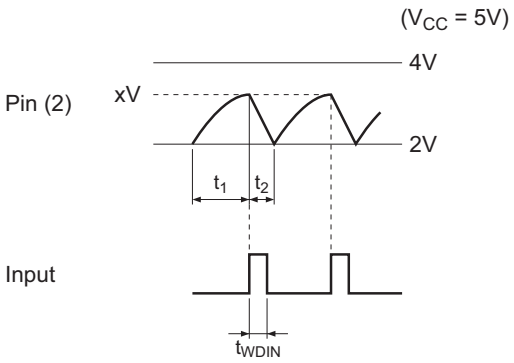
$$t_{RST(2)} = 1000 \cdot C \cdot \ell n \frac{4 \cdot \frac{R_1}{1000} - 1}{2 \cdot \frac{R_1}{1000} - 3}$$ (discharge time)



Resistance R_1: $10k\Omega \leq R_1 \leq 30k\Omega$
When R_1 is $10k\Omega$, $t_{RST(2)}$ is $830 \cdot C$

Figure 2

2. Pin (1) (WD pin) input frequency, input pulse width, charge time and discharge time
   When input to WD pin is normal, TC pin output waveform is as shown below:



$$t_1 = C \cdot R_1 \cdot \ell n \frac{3}{5 - x}$$ (charge time)

$$t_2 = 1000 \cdot C \cdot \ell n \frac{(\frac{R_1}{1000} + 1)\, x - 5}{2 \cdot \frac{R_1}{1000} - 3}$$ (discharge time)

Figure 3

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- Pin (1) (WD pin) input requirements
  (1) Connect capacitor between WD pin and voltage input. (refer to section 3)
  (2) Input cycle: t_{WD} or less (discharge should start before voltage at WD pin reaches 4 V.)

$$\frac{1}{1.1 \cdot C \cdot R_1} < f$$

  (3) Input pulse width t_{WDIN}: t_2 or less

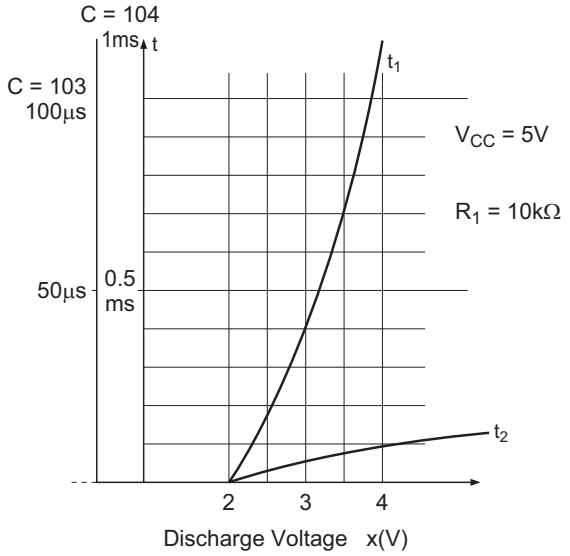
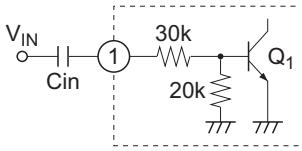


Figure 4

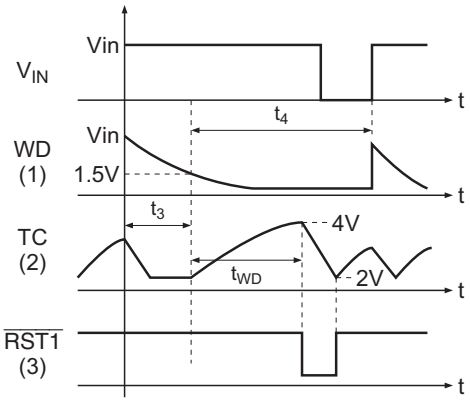
3. Relationship between input pulse width and input capacitance Cin
   When input to pin (1) is 1.5 V or more, TC pin discharges electricity. Determine pulse width and input capacitance Cin with reference to the diagram shown in figure 5.



Q_1 is off when voltage at pin (1) is 1.5V or less.

$$t_3 = Cin \cdot 5 \times 10^4 \cdot \ell n \frac{Vin}{1.5}$$

$\overline{RST1}$ is output when t_4 is longer than t_{WD}.



Cin: 10000pF, t_3 = 0.6ms
Cin: 1000pF, t_3 = 60µs
Cin: 100pF, t_3 = 6µs

When t_3 is too long, TC pin output waveform frequency changes as shown above. Set t_3 to be sufficiently long to turn on Q_1 [t_{WDIN}(3µs) or more] but not to exceed t_2 (discharge time).
(t_2: Discharge time during normal input)

Figure 5

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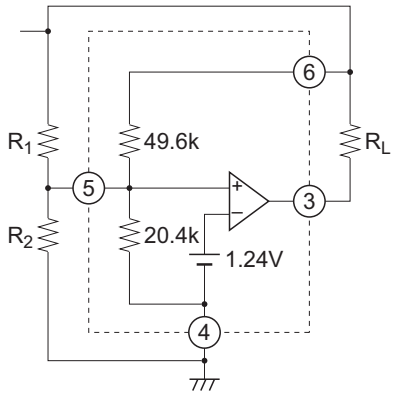
4. V_{CC} detection voltage adjustment

(1) Detection voltage 1 (V_{TH1}) adjustment



V_{TH1} (V)	R_1 (kΩ)	R_2 (kΩ)	Detection voltage calculation formula
13	10	0.92	$V_{TH1} = \frac{R_{01} + R_{02}}{R_{02}} \times 1.24$ (V) $(R_{01} = R_1 // 49.6k\Omega$ $R_{02} = R_2 // 20.4k\Omega)$
10	10	1.25	
7	10	1.96	
5	10	3.17	
4.25	—	—	
4	10.90	5	
3.5	8.59	5	

To adjust detection voltage 1, determine external resistance with the following equations.

(a) $V_{TH1} > 4.25V$ ($R_1 = 10k\Omega$)

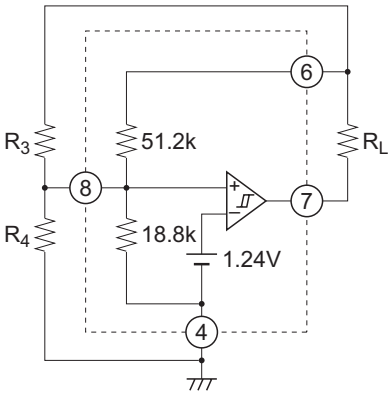
$$R_2 = \frac{1}{\frac{1}{R_0} - \frac{1}{20.4k}} \qquad (R_0 = \frac{8.322k \times 1.24}{V_{TH1} - 1.24})$$

(b) $V_{TH1} < 4.25V$ ($R_2 = 5k\Omega$)

$$R_1 = \frac{1}{\frac{1}{R_0} - \frac{1}{49.6k}} \qquad (R_0 = \frac{(V_{TH1} - 1.24)\ 4.016k}{1.24})$$

Figure 6 Detection Voltage 1 (V_{TH1}) Adjustment

(2) Detection voltage 2 ($V_{TH2(L)}$) adjustment



$V_{TH2(L)}$ (V)	R_3 (kΩ)	R_4 (kΩ)	ΔV_{TH2} (mV)	Detection voltage calculation formula
13	10	0.93	16.3	$V_{TH2(L)} = \frac{R_{03} + R_{04}}{R_{04}} \times 1.24$ (V) $(R_{03} = R_3 // 51.2k\Omega$ $R_{04} = R_4 // 18.8k\Omega)$ $\Delta V_{TH2} = \frac{R_{03}}{51.2k} \times 100$ (mV)
10	10	1.26	16.3	
7	10	1.99	16.3	
5	10	3.24	16.3	
4.6	—	—	100	
4	10.61	5	17.2	
3.5	8.38	5	14.1	

To adjust detection voltage 2, determine external resistance with the following equations.

(a) $V_{TH2(L)} > 4.6V$ ($R_3 = 10k\Omega$)

$$R_4 = \frac{1}{\frac{1}{R_0} - \frac{1}{18.8k}} \qquad (R_0 = \frac{8.37k \times 1.24}{V_{TH2(L)} - 1.24})$$

(b) $V_{TH2(L)} < 4.6V$ ($R_4 = 5k\Omega$)

$$R_3 = \frac{1}{\frac{1}{R_0} - \frac{1}{51.2k}} \qquad (R_0 = \frac{(V_{TH2(L)} - 1.24)\ 3.95k}{1.24})$$

Figure 7 Detection Voltage 2 ($V_{TH2(L)}$) Adjustment

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Application Example

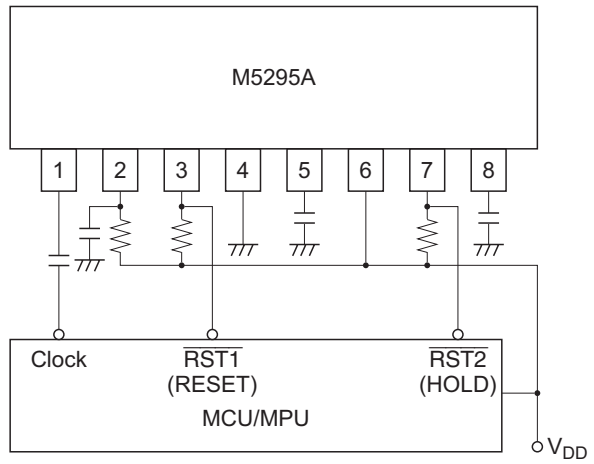
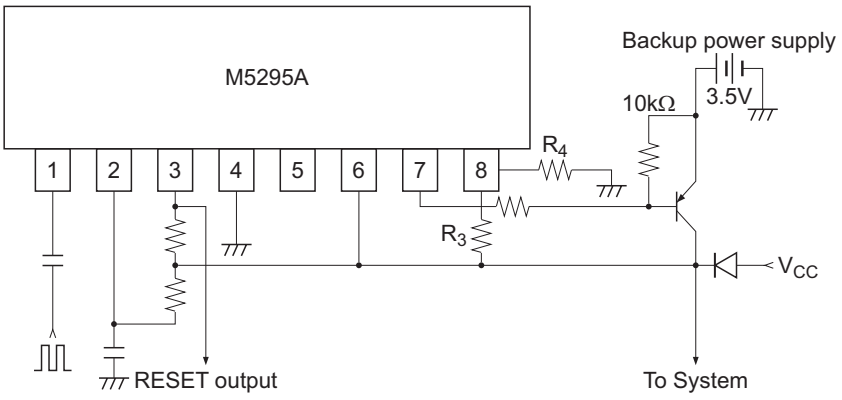


Figure 8 Application Example

Notice for Use

1. When malfunction occurs due to noise or order related trouble, connect capacitance of approximately 1000 pF between pin (5) and GND as well as pin (8) and GND to stabilize operation.
2. To adjust detection voltage, add resistance of 15 kΩ or less to both V_{CC} and GND via adjusting pins. (Set detection voltage to no less than 3 V.)
3. Set t_{WD} and $t_{RST(2)}$ as shown below:
   $110\ \mu s \leq t_{WD} \leq 1.1\ s$
   $8.3\ \mu s \leq t_{RST(2)} \leq 83\ ms$
   $10\ k\Omega \leq R_1 \leq 30\ k\Omega$
4. Input clock pulses to pin (1) via capacitor. To determine capacitance, refer to “Relationship between input pulse width and input capacitance Cin”.



Backup switching voltage $V_{TH2(L)}$ Switching voltage calculation formula

$$V_{TH2(L)} = \frac{R_{03} + R_{04}}{R_{04}} \times 1.24\ (V)$$

$$\begin{pmatrix} R_{03} = R_3 \,//\, 51.2k\Omega \\ R_{04} = R_4 \,//\, 18.8k\Omega \end{pmatrix}$$

Note: Set backup switching voltage to be more than or equal to backup supply voltage.

Figure 9 Example of Backup Circuit with M5295AL

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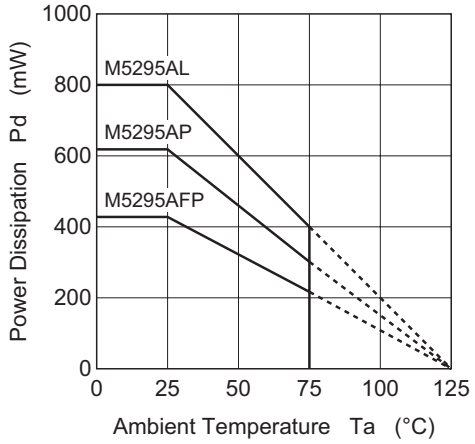
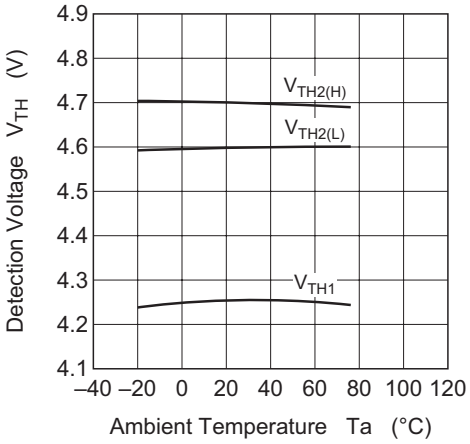
Typical Characteristics

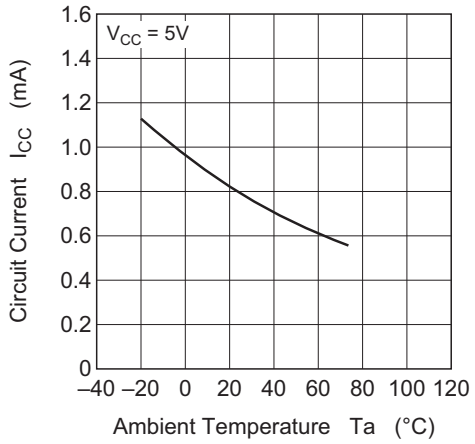
Thermal Derating
(Maximum Rating)



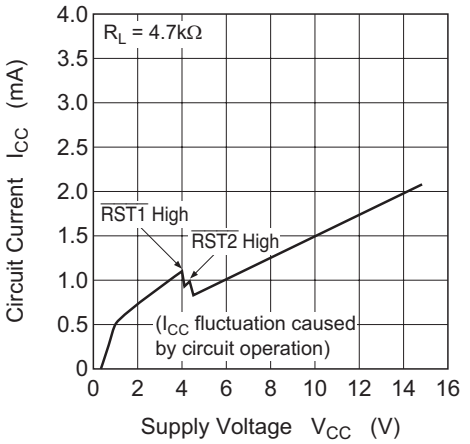
Detection Voltage vs. Ambient Temperature



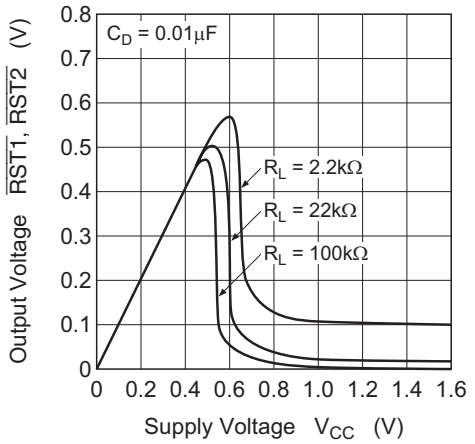
Circuit Current vs. Ambient Temperature



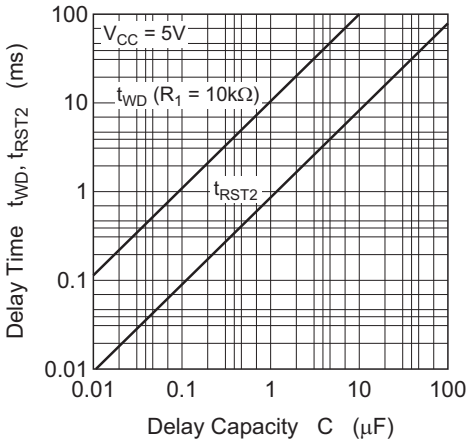
Circuit Current vs. Supply Voltage



Critical Operation Voltage Characteristics



Delay Time vs. Delay Capacity



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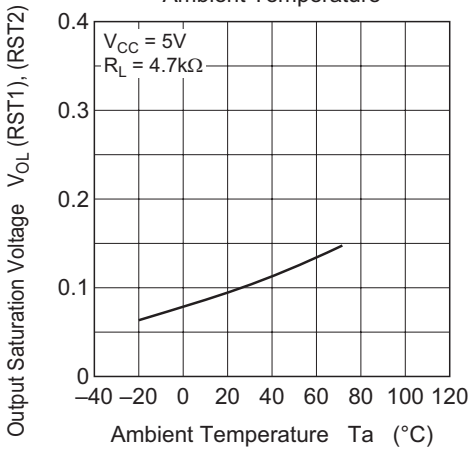
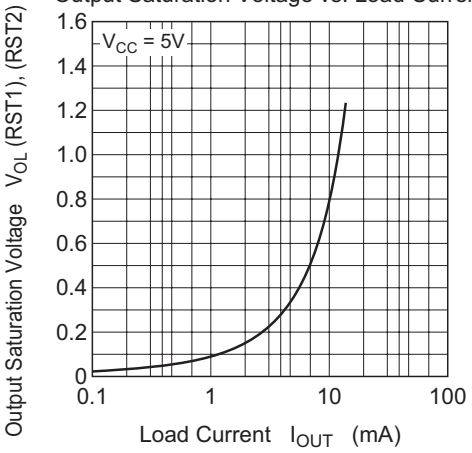
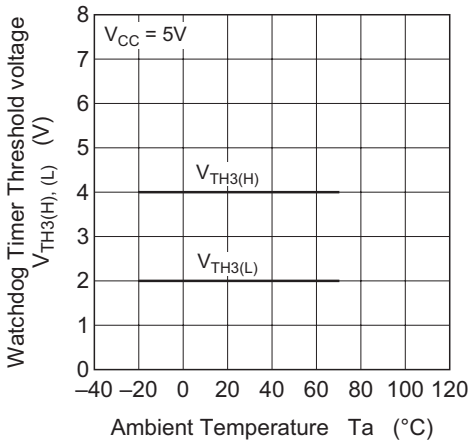
Output Saturation Voltage vs. Ambient Temperature



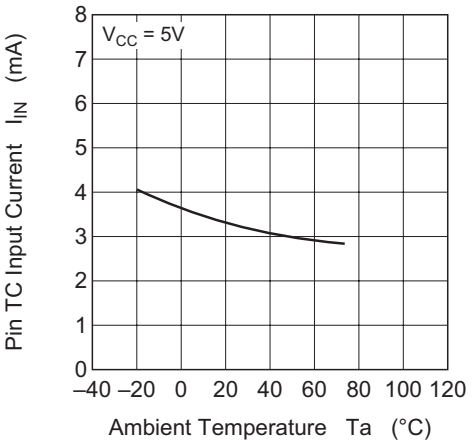
Output Saturation Voltage vs. Load Current



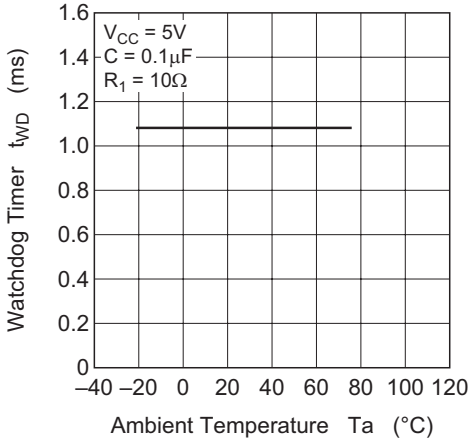
Watchdog Timer Threshold voltage vs. Ambient Temperature



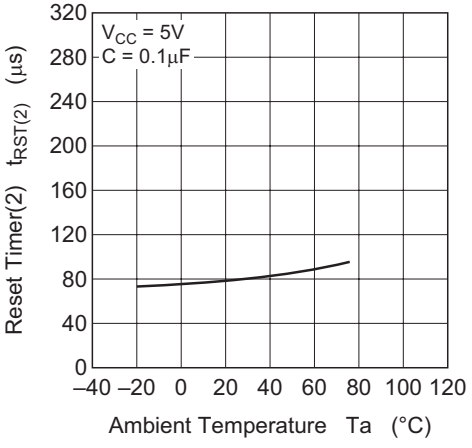
Pin TC Input Current vs. Ambient Temperature



Watchdog Timer vs. Ambient Temperature



Reset Timer(2) vs. Ambient Temperature



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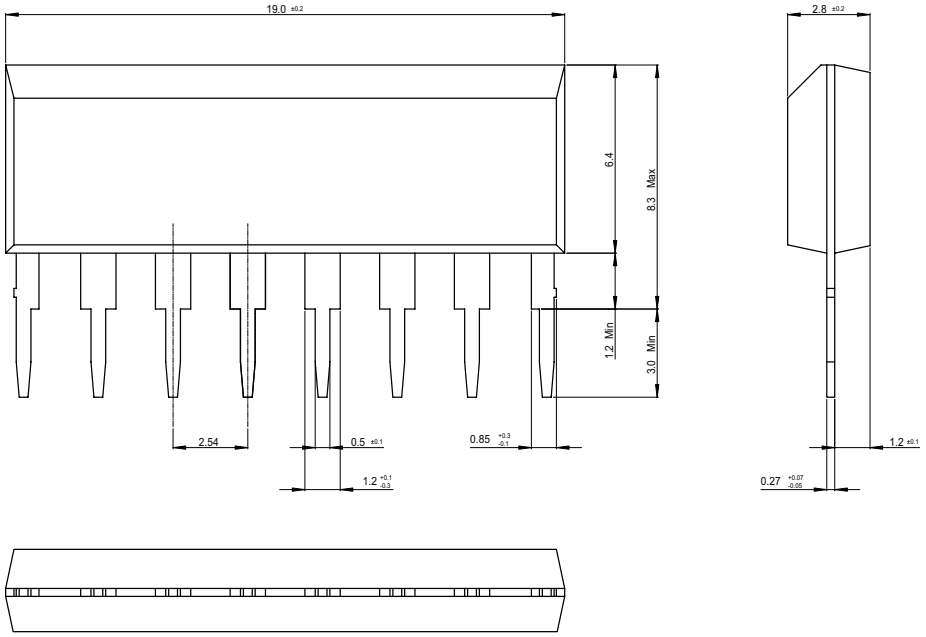
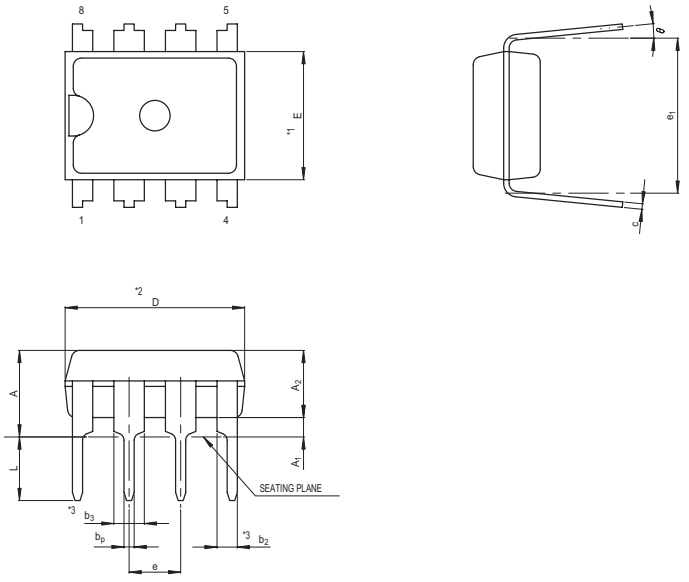
Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SIP8-6.4x19-2.54	PRSS0008AA-A	8P5	0.73g



JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP8-6.3x8.84-2.54	PRDP0008AA-A	8P4	0.5g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e_1	7.32	7.62	7.92
D	8.7	8.9	9.1
E	6.15	6.3	6.45
A	—	—	4.5
A_1	0.51	—	—
A_2	—	3.3	—
b_p	0.4	0.5	0.6
b_2	0.9	1.0	1.3
b_3	1.4	1.5	1.8
c	0.22	0.27	0.34
θ	0°	—	15°
e	2.29	2.54	2.79
L	3.0	—	—

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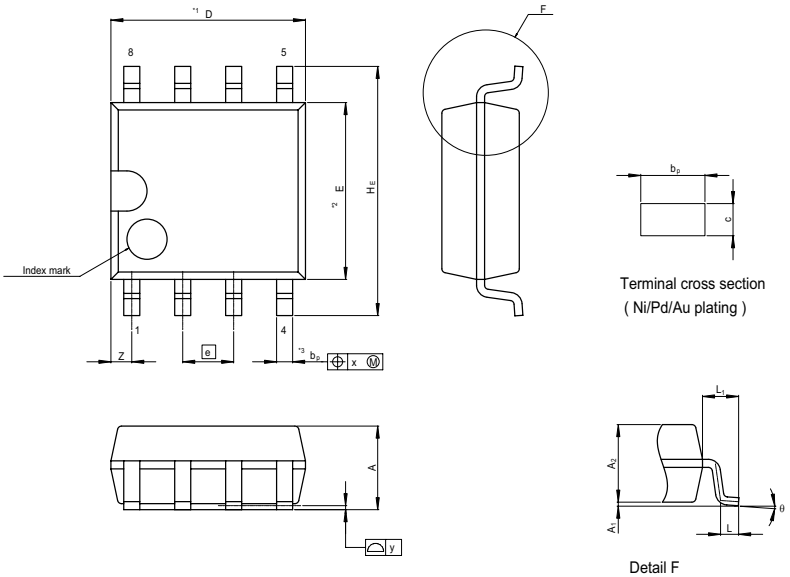
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP8-4.4x4.85-1.27	PRSP0008DE-C	—	0.1g



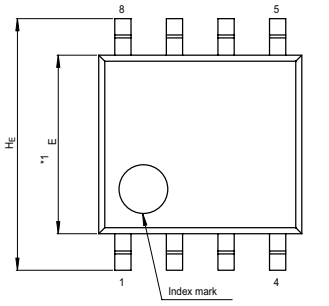
Terminal cross section
(Ni/Pd/Au plating)

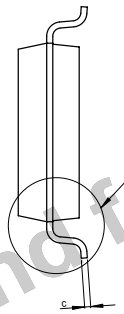
Detail F

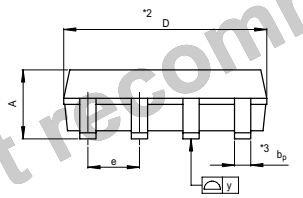
NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.

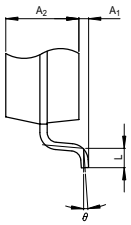
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.65	4.85	5.05
E	4.2	4.4	4.6
A_2	—	1.85	—
A_1	0.00	0.1	0.20
A	—	—	2.03
b_p	0.34	0.4	0.46
b_1	—	—	—
c	0.15	0.20	0.25
c_1	—	—	—
θ	0°	—	8°
H_E	5.7	6.2	6.5
e	1.12	1.27	1.42
x	—	—	0.12
y	—	—	0.10
Z	—	—	0.75
L	0.25	0.45	0.65
L_1	—	0.90	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP8-4.4x5-1.27	PRSP0008DA-A	8P2S-A	0.07g









Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.8	5.0	5.2
E	4.2	4.4	4.6
A_2	—	1.5	—
A_1	0.05	—	—
A	—	—	1.9
b_p	0.35	0.4	0.5
c	0.13	0.15	0.2
θ	0°	—	10°
H_E	5.9	6.2	6.5
e	1.12	1.27	1.42
y	—	—	0.1
L	0.2	0.4	0.6

not recommend for new design

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