HA16138PS

AC/DC Switching Converter Controller IC With High-Voltage Power MOS FET

HITACHI

ADE-204-032 (Z)
Preliminary
1st Edition
MAY 2000

Description

The HA16138PS is an IC with a high-voltage power MOS FET and current-mode type PWM controller mounted in a DILP-8 (DP-8) standard package, suitable for low-power power supplies in the 10 W class and below.

The HA16138PS includes an energy-saving mode for holding down power consumption when on standby (no load). When the energy-saving mode is entered, the operating frequency is reduced to 1/4 the normal frequency, reducing power consumption. A starter circuit is also provided on-chip, eliminating the need for the external start-up resistance needed with previous controller ICs. The starter circuit in this IC is turned off automatically after the IC starts up, enabling the start-up resistance power consumption to be decreased.

The HA16138PS includes a soft start circuit, OVP circuit, and remote on/off circuit, making it possible to configure a simple protection circuit with fewer external parts than previously. Also provided are a current sense resistance and a leading edge blanking circuit that masks spike noise on current sense input, making noise reduction in a power supply set comparatively easy.

The HA16138PS is equipped with an error amp circuit inverting input (FB) pin and output (COMP) pin, enabling special-purpose design for both flyback system secondary-side output voltage detection and primary-side back-up transformer output voltage detection types.

Features

- Built-in high-voltage power MOS FET
- Energy-saving mode (power saving through reduction of operating frequency to 1/4 normal frequency when on standby)
- Built-in starter circuit, reducing power loss of start-up resistance when on standby (external start-up resistance not necessary)
- Built-in soft start circuit, eliminating need for external connection
- Remote on/off function, enabling power saving by halting PWM output without turning off power supply
- Built-in current sense resistance and leading edge blanking circuit, for sense-resistance-less and noise-cancellation-filter-less implementation
- Built-in over voltage protection circuit
- Built-in over temperature protection circuit

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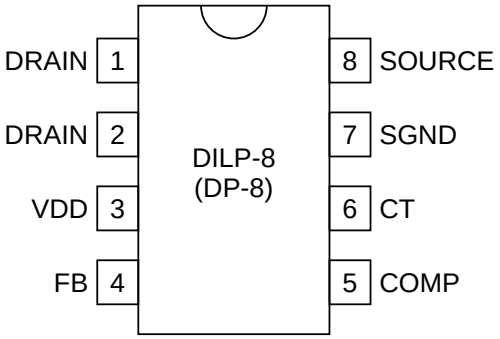
Pin Arrangement

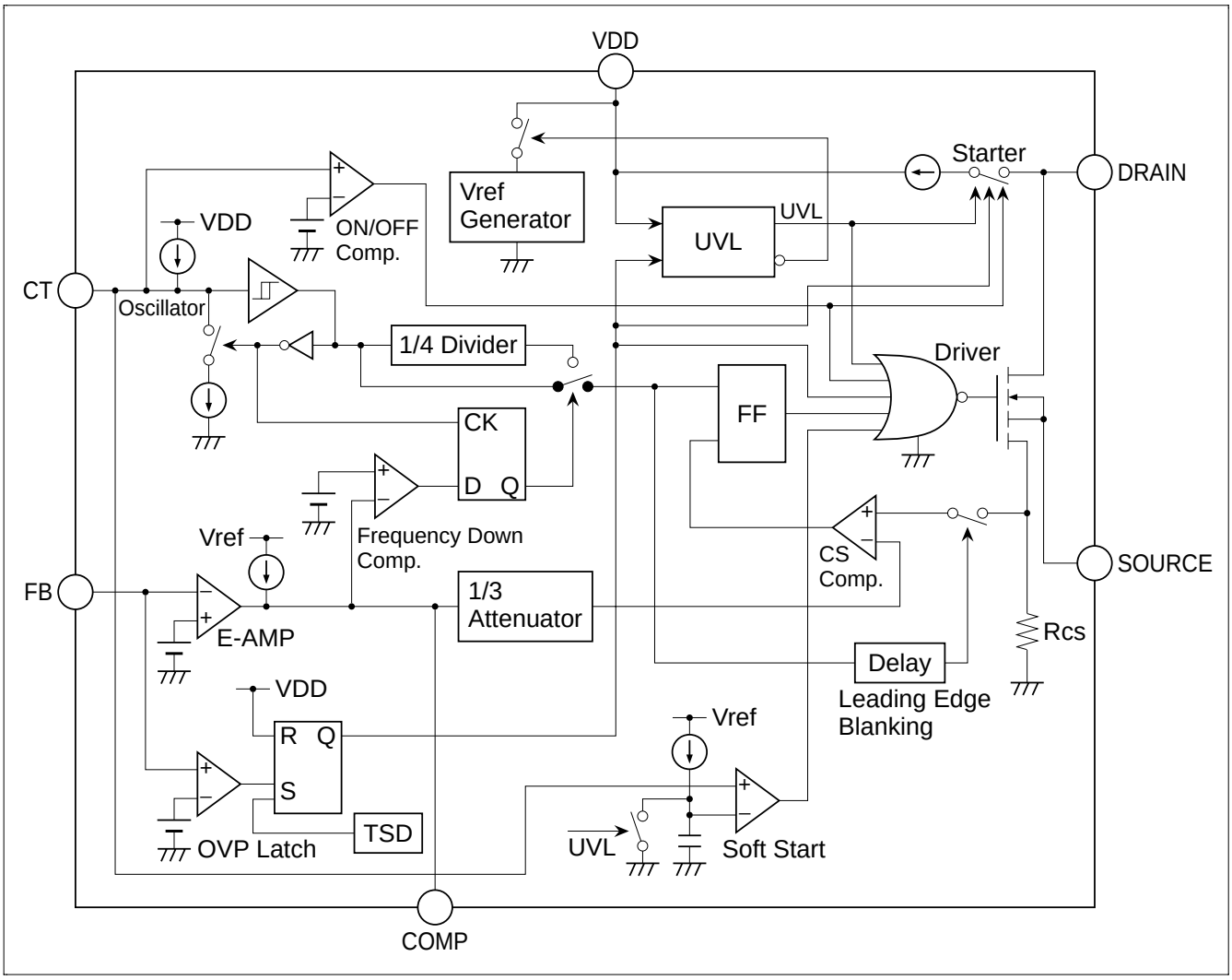


(Top view)

Pin Functions

Pin No.	Pin Name	Pin Function
1	DRAIN	On-chip power MOS FET drain pin / starter circuit input pin
2	DRAIN	On-chip power MOS FET drain pin / starter circuit input pin
3	VDD	Power supply voltage input pin
4	FB	Error amplifier inverting input pin / OVP latch circuit input pin
5	COMP	Error amplifier output pin
6	CT	Timing capacitance connection pin / on/off circuit input pin
7	SGND	Primary-side common connection pin
8	SOURCE	On-chip power MOS FET source pin

Block Diagram



Absolute Maximum Ratings (Ta = 25°C)

Item		Symbol	Rating	Unit
Power MOS FET block	Drain-source voltage	V_{DS}	–0.3 to 700	V
	Maximum drain current	I_{DS}	0.5	A
Controller block	Power supply voltage	V_{DD}	0 to 15	V
	CT pin voltage	V_{CT}	0 to V_{DD}	V
	FB pin voltage	V_{FB}	0 to V_{DD}	V
	COMP pin voltage	V_{COMP}	0 to 5	V
Overall	Operating temperature	Topr	–20 to +85	°C
	Junction temperature	Tjmax	+150	°C
	Storage temperature	Tstg	–55 to +150	°C

Electrical Characteristics (Tj = 25°C, V_{DD} = 12 V, fosc1 = 100 kHz)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Power	Drain-source voltage	BV_{DSS}	700	—	—	V	
MOS FET	Drain-source on resistance	$R_{DS(on)}$	—	12	20	Ω	I_D = 0.4 A
Starter	Start-up start drain voltage	V_{DRN}	55	75	95	V	
circuit	Start-up charge current	I_{CHG}	125	250	500	µA	
UVL circuit	Operation start power supply voltage	V_{TH}	10	11	12	V	
	Operation stop power supply voltage	V_{TL}	7	8	9	V	
	Operating power supply current	I_{DD}	—	2.5	4.0	mA	
Oscillation	Normal mode operating frequency	fosc1	88	100	112	kHz	C_T = 220 pF
circuit	F-down mode operating frequency	fosc2	22	25	28	kHz	C_T = 220 pF, V_{COMP} = 0 V
	Maximum on duty	Dumax	—	70	—	%	
Error	Open-loop voltage gain	A_V	50	65	—	dB	Rcomp = 220 kΩ
amplifier	Unity gain bandwidth	BW	—	550	—	kHz	Rcomp = 220 kΩ
	Output high voltage 1	V_{COMPH1}	4.5	5.0	—	V	Iosource = 0 µA
	Output high voltage 2	V_{COMPH2}	4.3	4.8	—	V	Iosource = 100 µA
	Output low voltage	V_{COMPL}	—	0.50	0.75	V	Iosink = 0 µA
	Non-inverting input voltage	$V_{(+)EA}$	3.4	3.8	4.2	V	
Power	Output rise time	t_r	—	100	—	ns	C_L = 1000 pF
MOS FET	Output fall time	t_f	—	80	—	ns	C_L = 1000 pF
gate drive	Output high voltage	V_{OH}	—	10	—	V	Iosource = 25 mA
circuit	Output low voltage	V_{OL}	—	0.5	—	V	Iosink = 25 mA
Current	Current sense voltage gain	A_{VCS}	—	3.0	—	V/V	
sense	Current sense response time	tpdcs	—	200	—	ns	Vcomp = 5.0 V
circuit	Leading edge blanking time	t_{BL}	—	300	—	ns	
OVP latch	OVP latch set voltage	Vovp	4.2	5.0	5.8	V	Vovp: FB pin voltage
circuit	OVP latch reset voltage	Vovpr	—	4.0	—	V	Vovpr: VDD pin voltage
	OVP latch current dissipation	Iovp	—	1.1	1.7	mA	V_{FB} = 6.0 V
Remote on/off circuit	Off mode start voltage	Voff	3.6	3.8	4.0	V	Voff: CT pin voltage
Soft start circuit	Soft start time	tst	(1.0)	2.0	(3.0)	ms	Time from start-up to max. duty
f-down comparator	F-down mode start voltage	Vfdcp	0.7	0.85	1.0	V	
Over temperature protection circuit	Over temperature protection start temperature	TSD	—	150	—	°C	TSD: Power MOS FET junction temperature

Functional Description

Note: Unless specified otherwise, characteristic values in the text and figures are typical values or design values.

Starter Circuit

When power is turned on, the starter circuit operates during standby mode, and a constant current is supplied from the drain pins to the VDD pin. This constant current supplies the external capacitance charge current for charging up the VDD pin and the standby current consumed by the IC itself while on standby.

Therefore, the start-up bleeder resistance required by previous products with no on-chip starter circuit is no longer necessary. The starter circuit detects both the drain voltage and the VDD pin voltage, and controls VDD so that the IC does not start up if the drain voltage is less than 75 V.

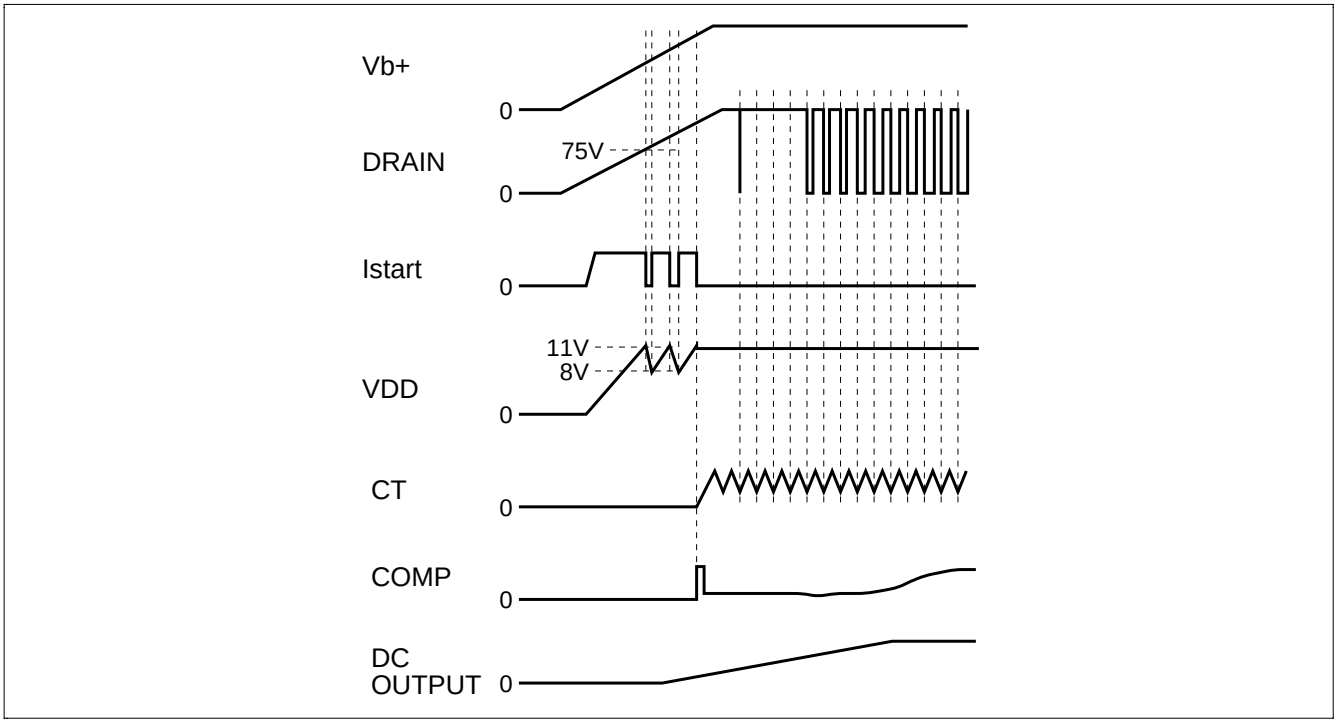


Figure 1 Start-Up Timing

UVL Circuit

The UVL circuit is a function that monitors the VDD voltage, and stops IC operation if VDD is low. The VDD detection voltage has a hysteresis characteristic; the operating start VDD voltage is 11 V, and the operation stop voltage, 8 V.

In standby mode at the operation stop voltage or below, the UVL circuit keeps the power MOS FET turned off, and performs control of soft start circuit resetting, internal reference voltage circuit stoppage, and so forth.

Error Amplifier

The error amplifier comprises a constant-current source type Pch top differential amplifier. As the inverting input (FB) pin and output (COMP) pin are provided as external pins, use for both a simple flyback power supply back-up voltage feedback type and a high-precision secondary voltage detection type is possible.

Current Sense Circuit

This is a 200 ns high-speed comparator circuit suitable for current mode control. The current sense controller reference voltage depends on the COMP pin voltage, being always 1/3 of the COMP pin voltage.

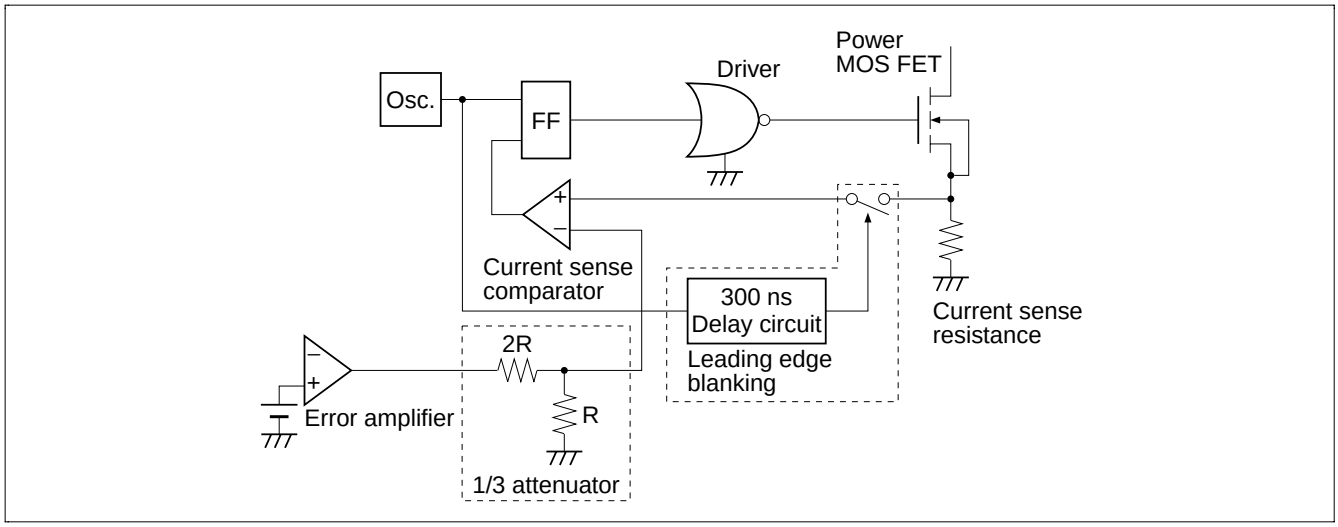


Figure 2 Current Sense Peripheral Circuitry

Leading Edge Blanking Circuit

The on-chip leading edge blanking circuit masks the current sense comparator input signal for a period of 300 ns after the power MOS FET gate voltage goes high. This reduces the erroneous operation due to spike-shaped noise caused by discharge of various capacitance components when the power MOS FET is turned on.

Oscillation Circuit

The oscillator generates a triangular voltage waveform through the discharge of the timing capacitance CT. With a 220 pF CT connected, the oscillator operates at 100 kHz.

The triangular voltage waveform has a discharge time ratio of 3:1, with the charge side set to PWM on-pulses, and the discharge side to dead-band pulses. The maximum PWM on duty can be controlled up to 70%.

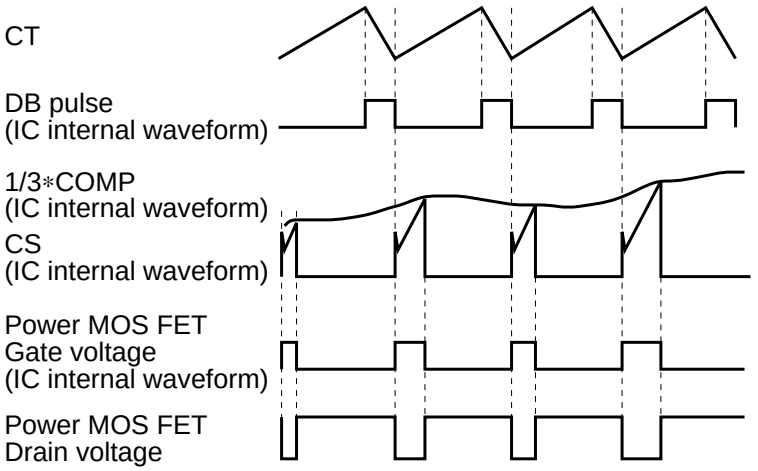


Figure 3 Oscillation Circuit Peripheral Waveform Timing

OVP Latch Circuit

When the FB pin voltage reaches 5 V or above, the OVP latch circuit operates and forcibly stops PWM output and the reference voltage generation circuit. While OVP latching is stopped, the starter circuit is also stopped. Latch resetting can be performed by driving power supply voltage VDD to 4 V or below.

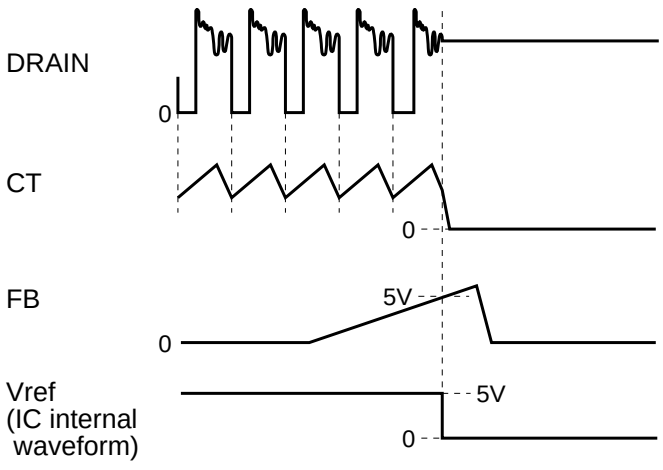


Figure 4 OVP Latch Operation Timing

Remote On/Off Circuit

When the CT pin voltage is pulled up to 3.8 V or above, the remote on/off circuit operates and PWM output can be stopped without turning off the power supply. When stoppage is executed by means of the on/off circuit, PWM output and the starter circuit are stopped, and the soft start circuit is reset, but the reference voltage generation circuit does not stop.

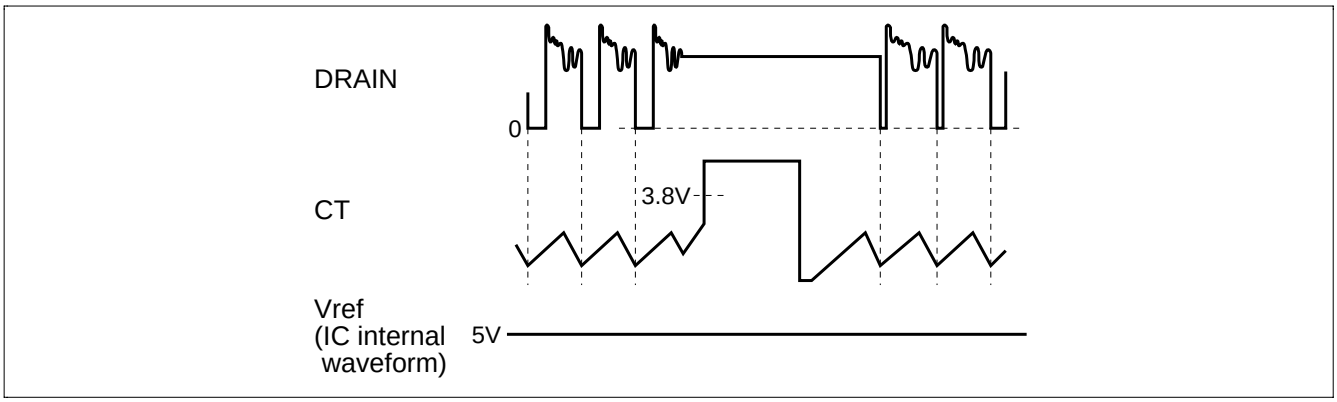


Figure 5 Remote On/Off Operation Timing

Soft Start Circuit

This circuit implements a soft start function with a 2 ms time constant without the use of external parts. During a soft start, the PWM output pulse width gradually increases. The soft start time is defined as the time from the point at which the UVL circuit start voltage is exceeded to the point at which PWM output reaches its maximum duty.

f-down Comparator

An "energy-saving mode" is provided to hold down power consumption during standby, with the operating frequency in the unloaded state reduced to 1/4 of its steady operation value.

The f-down comparator detects the COMP pin voltage, and if it falls to 0.85 V or below, switches to energy-saving mode. As COMP pin voltage detection is performed pulse-by-pulse, a skip mode comes into effect in the vicinity of the threshold voltage according to the timing.

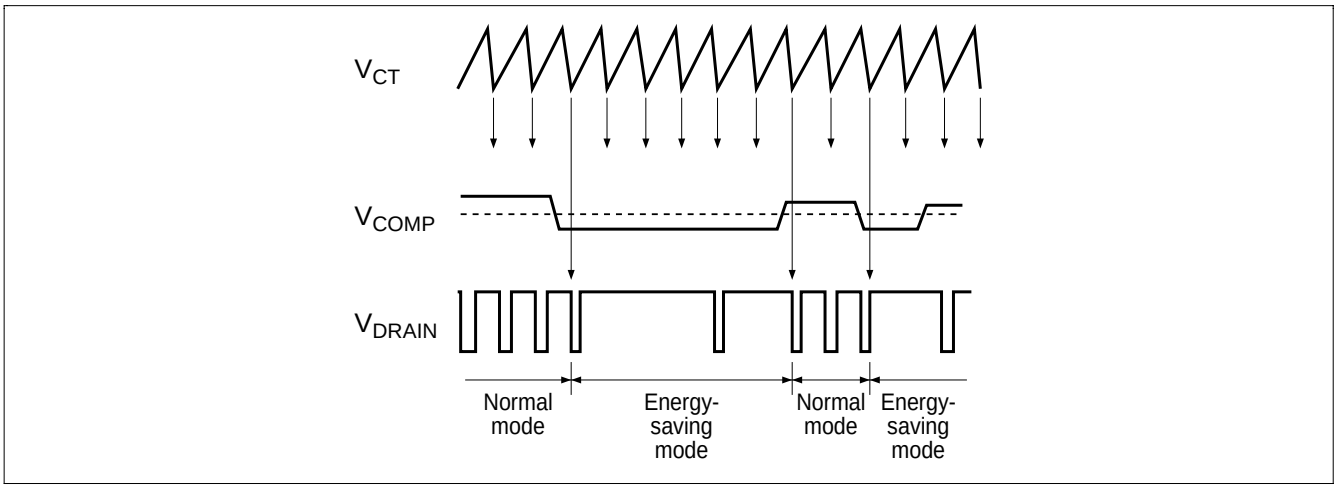


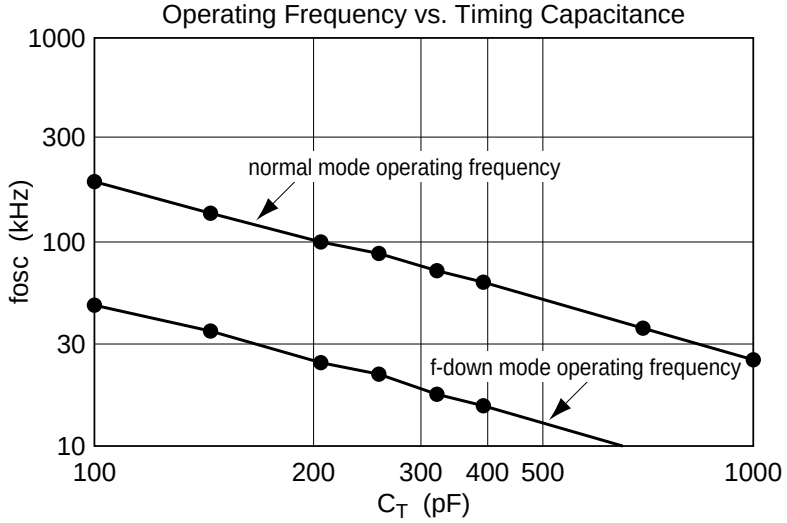
Figure 6 Energy-Saving Mode Switching Waveform Timing

Over Temperature Protection Circuit

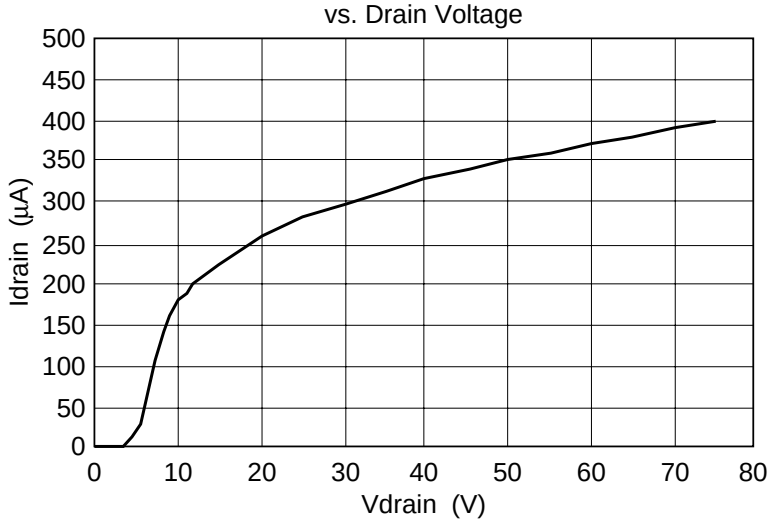
If the power MOS FET junction temperature reaches +150°C, the over temperature protection circuit operates, shutting down the IC. The over temperature protection circuit is coupled to the OVP latch circuit, so that the latch is reset if the power supply voltage is driven to 4 V or below while the junction temperature is lower than the overheating protection start temperature.

Main Characteristics

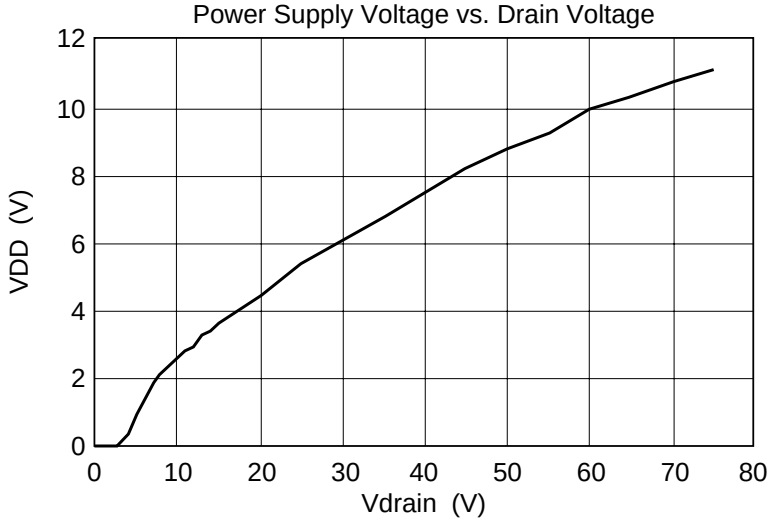
Operating Frequency vs. Timing Capacitance



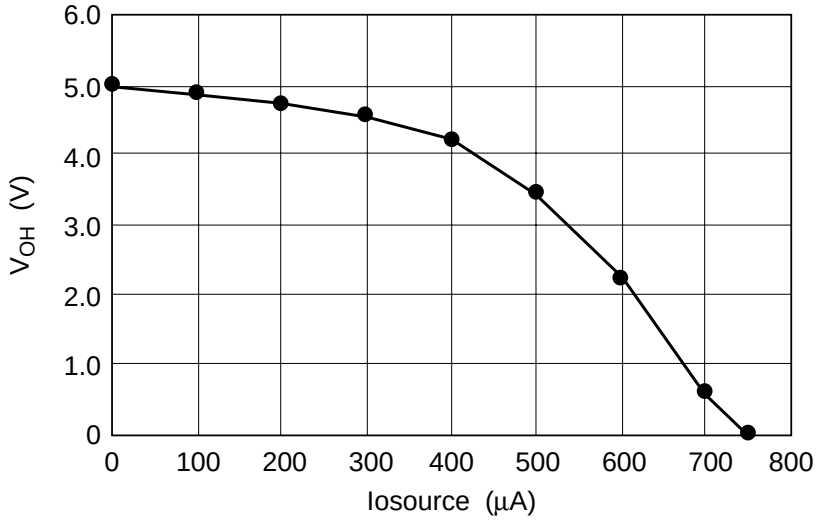
Start-up Current (Charge Current + Standby Current) vs. Drain Voltage



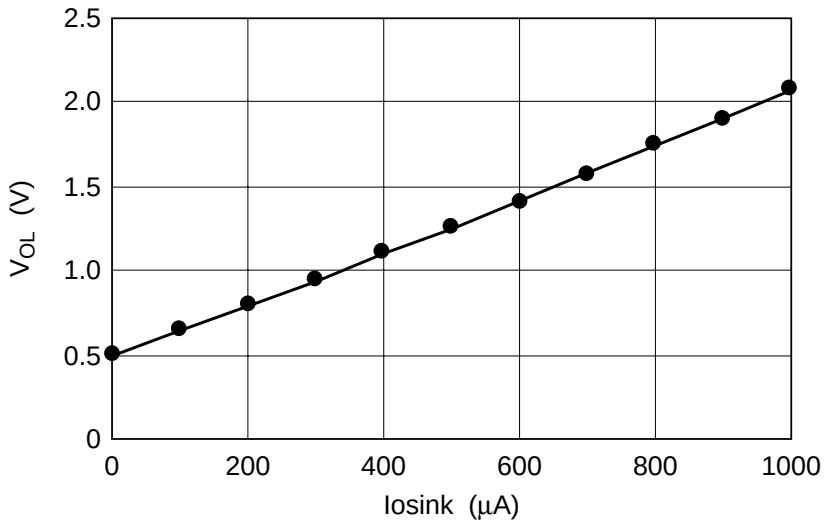
Power Supply Voltage vs. Drain Voltage



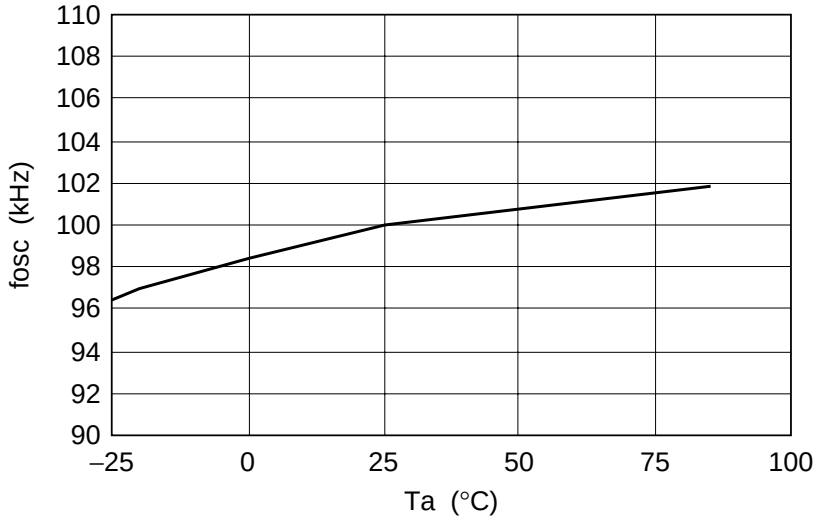
Error Amplifier Output High Voltage vs. Output Source Current



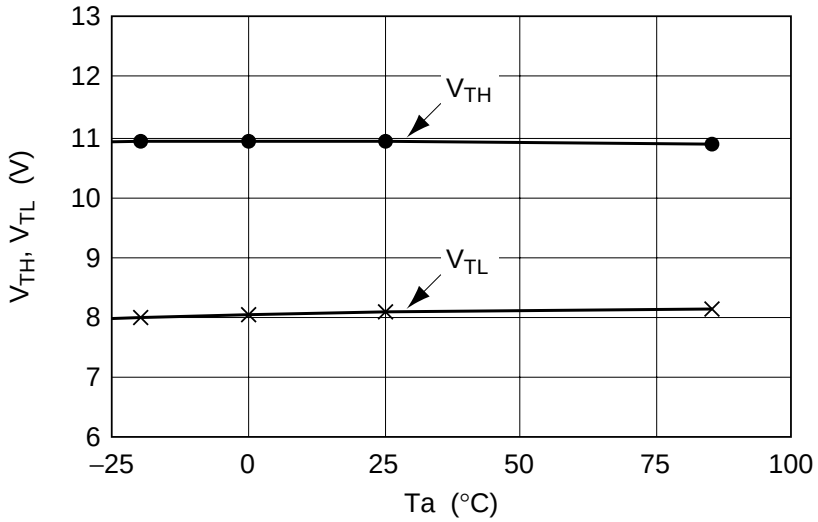
Error Amplifier Output Low Voltage vs. Output Sink Current

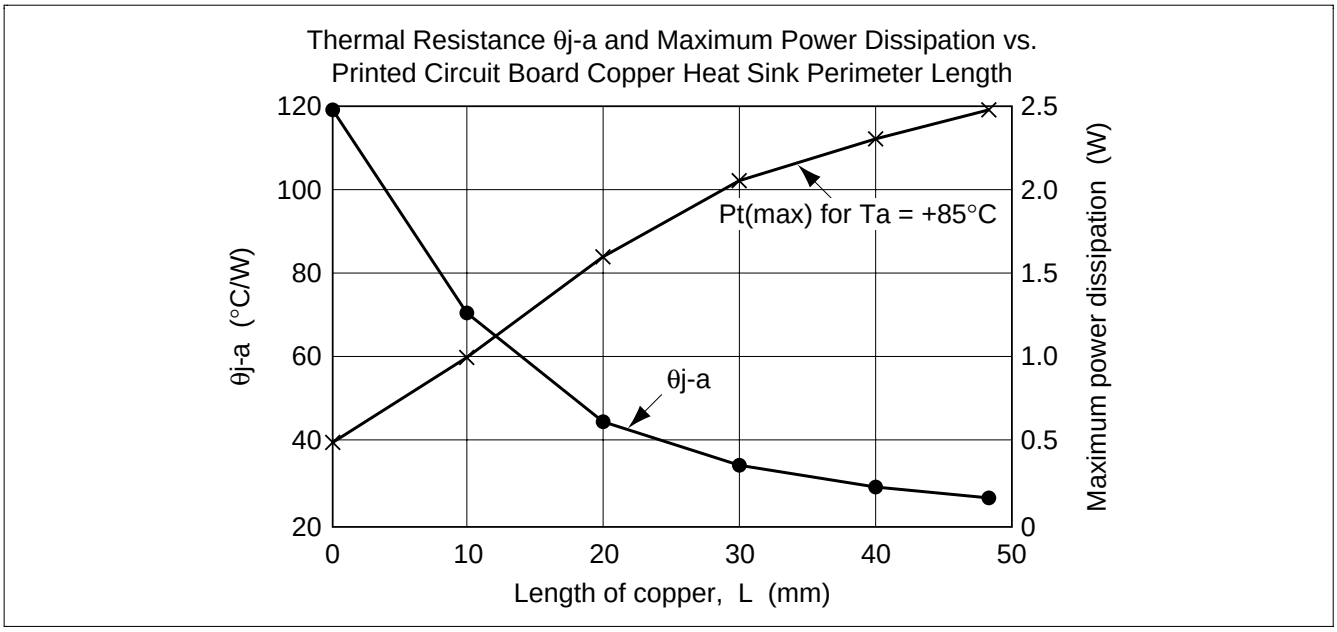


Operating Frequency (Normal Mode) vs. Ambient Temperature



Operating Start/Stop Power Supply Voltage vs. Ambient Temperature





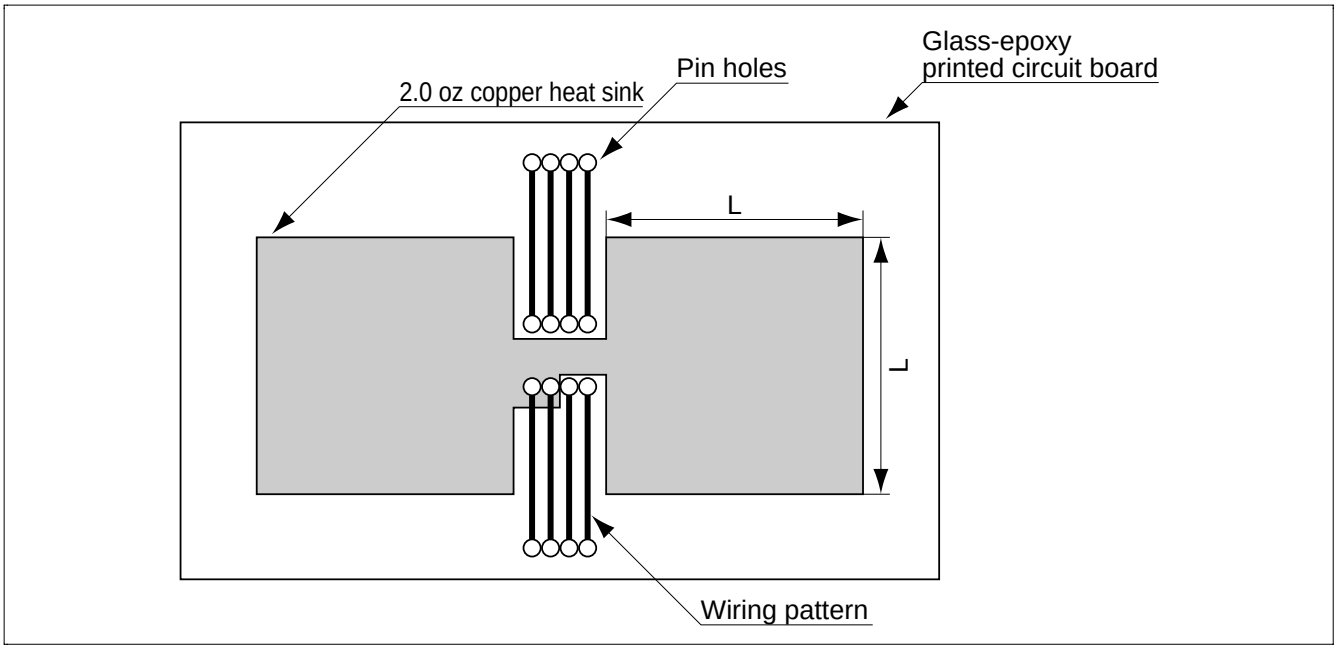
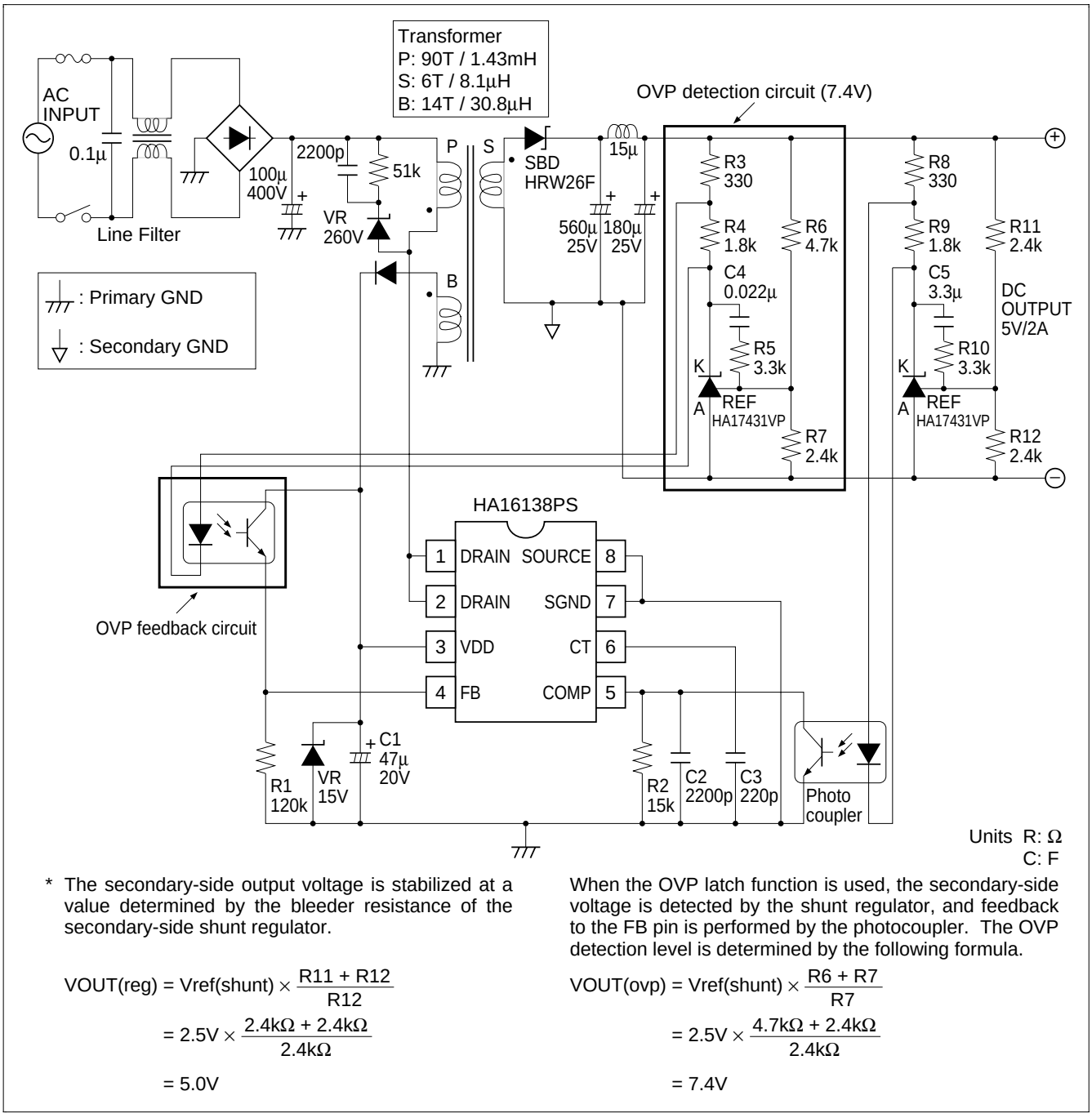


Figure 7 Sample Printed Circuit Board Copper Heat Sink Pattern

Application Circuit Examples 1

The application circuit example shown here detects the secondary-side output voltage of a flyback power supply. Secondary-side output voltage detection and feedback are performed by a shunt regulator and photocoupler.

When the OVP latch function is used for secondary-side output voltage overvoltage protection, the FB pin should be pulled up to VDD by the shunt regulator and photocoupler.



* The secondary-side output voltage is stabilized at a value determined by the bleeder resistance of the secondary-side shunt regulator.

$$VOUT(reg) = Vref(shunt) \times \frac{R11 + R12}{R12}$$

$$= 2.5V \times \frac{2.4k\Omega + 2.4k\Omega}{2.4k\Omega}$$

$$= 5.0V$$

When the OVP latch function is used, the secondary-side voltage is detected by the shunt regulator, and feedback to the FB pin is performed by the photocoupler. The OVP detection level is determined by the following formula.

$$VOUT(ovp) = Vref(shunt) \times \frac{R6 + R7}{R7}$$

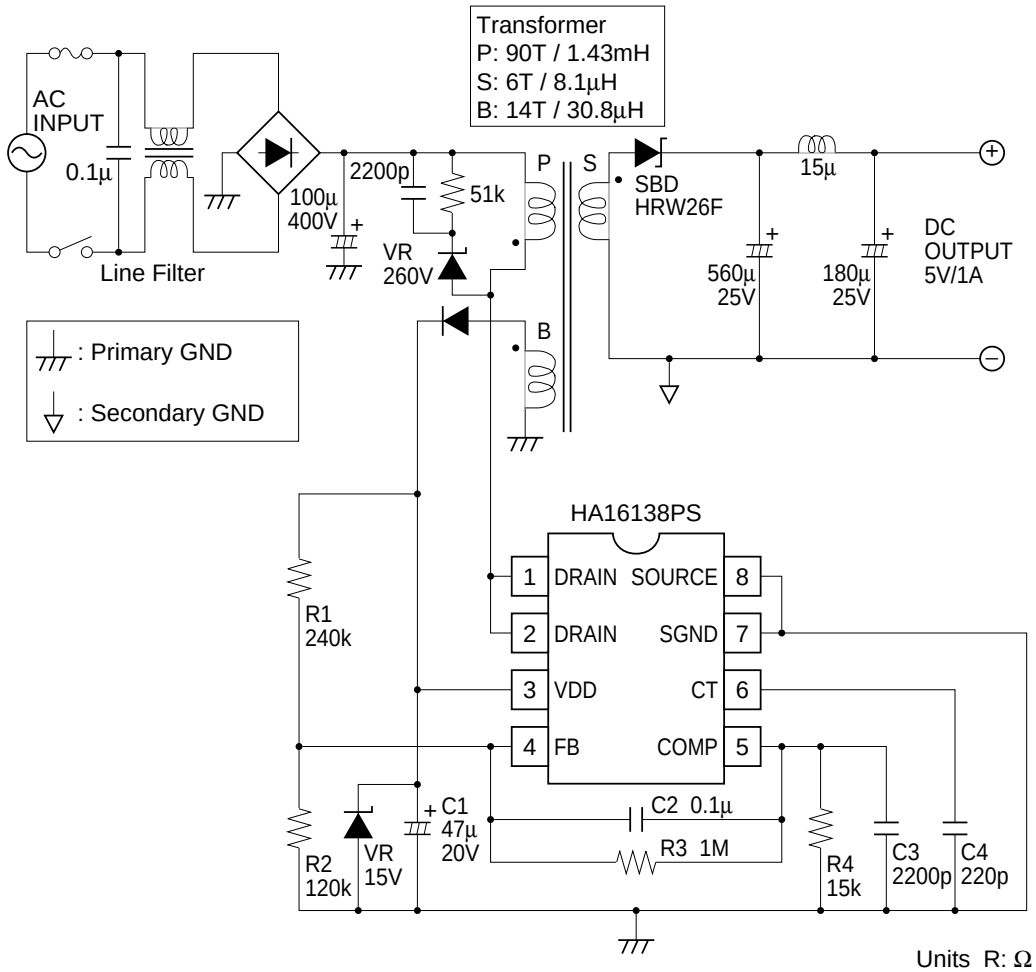
$$= 2.5V \times \frac{4.7k\Omega + 2.4k\Omega}{2.4k\Omega}$$

$$= 7.4V$$

Application Circuit Examples 2

The application circuit example shown here detects the primary-side back-up output voltage of a flyback power supply. As the back-up output voltage, VDD is resistance-divided and feedback is performed to the FB pin. The back-up output voltage and secondary-side output voltage are proportional to the ratio of transformer windings. Using this characteristic enables the system to be configured with simple circuitry as shown in the figure below.

The VDD-to-FB feedback resistance can also be used as the back-up output voltage OVP detection resistance.



Units R: Ω
C: F

* If feedback resistance R1 = 240 kΩ and R2 = 120 kΩ, feedback is performed so that the FB pin voltage is non-inverting input voltage $V_{(+)EA}$, and the VDD voltage is stabilized.

$$VDD(reg) = V_{(+)EA} \times \frac{R1 + R2}{R2}$$

$$= 3.8V \times \frac{240k\Omega + 120k\Omega}{120k\Omega}$$

$$= 11.4V$$

When the FB pin voltage reaches OVP latch set voltage Vovp, the OVP latch circuit operates, shutting down the IC. The VDD voltage in this case is given by the following formula.

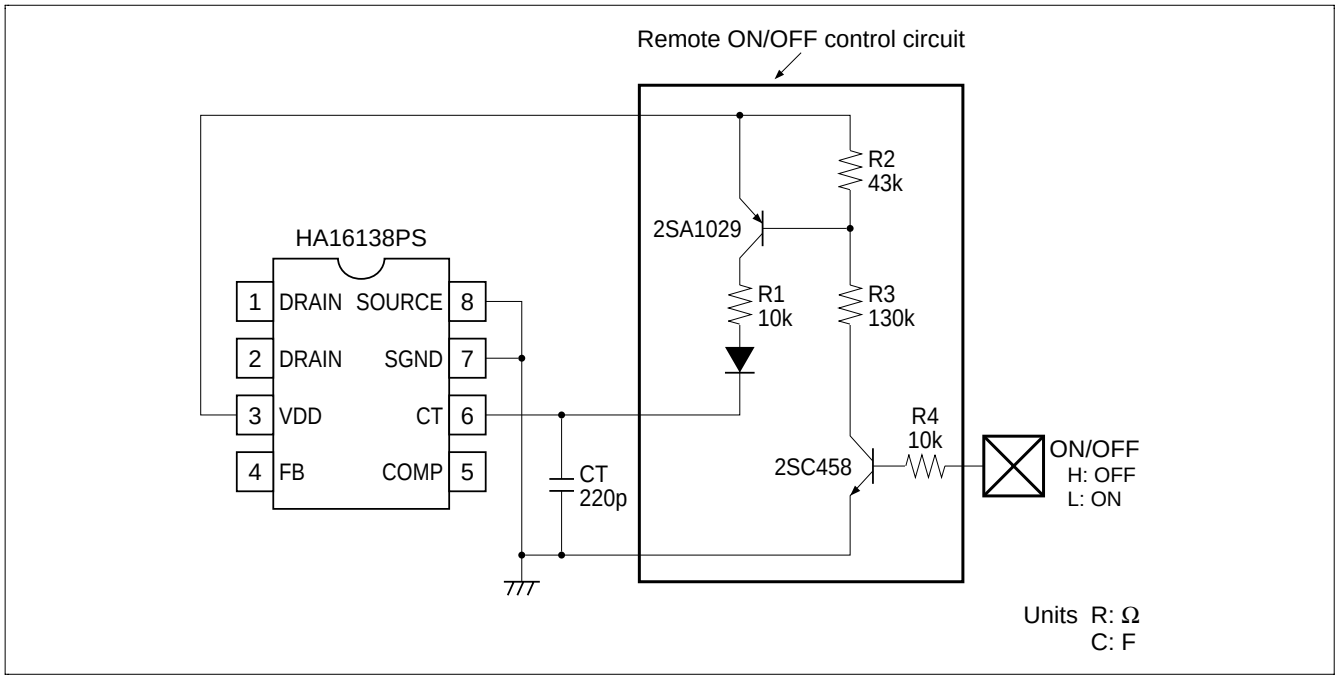
$$VDD(ovp) = Vovp \times \frac{R1 + R2}{R2}$$

$$= 5.0V \times \frac{240k\Omega + 120k\Omega}{120k\Omega}$$

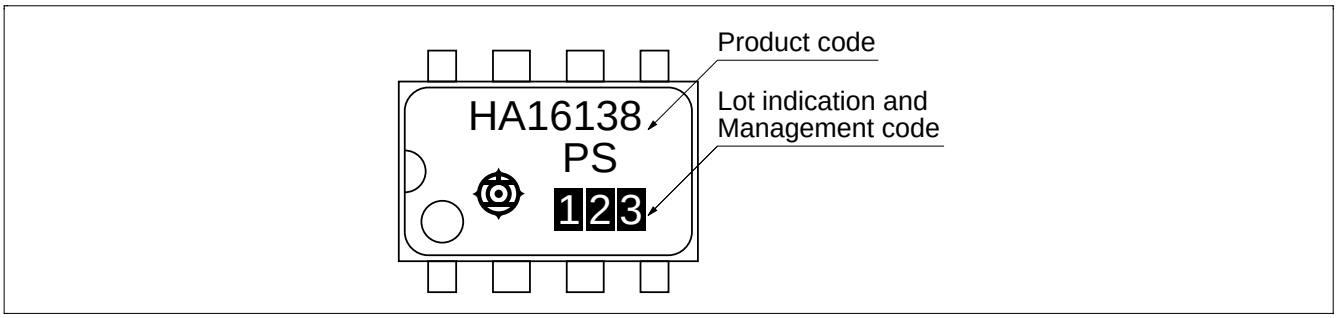
$$= 15V$$

Application Circuit Examples 3

As this IC is provided with a remote on/off function, it is possible to implement power management without turning off the power supply. Using a remote on/off control circuit as shown in the figure below, the CT pin voltage is pulled up to the off mode start voltage or above, and the IC is stopped. In the off mode, control of PWM output stoppage, soft start resistance resetting, and starter circuit stoppage is performed without stopping the internal reference voltage generation circuit. With this function, also, latch operation is not performed, and an auto-restart is executed as soon as the CT pin voltage falls below the off mode start voltage. It is recommended that the remote on/off control signal be controlled by a microcomputer or other logic signal.



Laser Marking Specifications



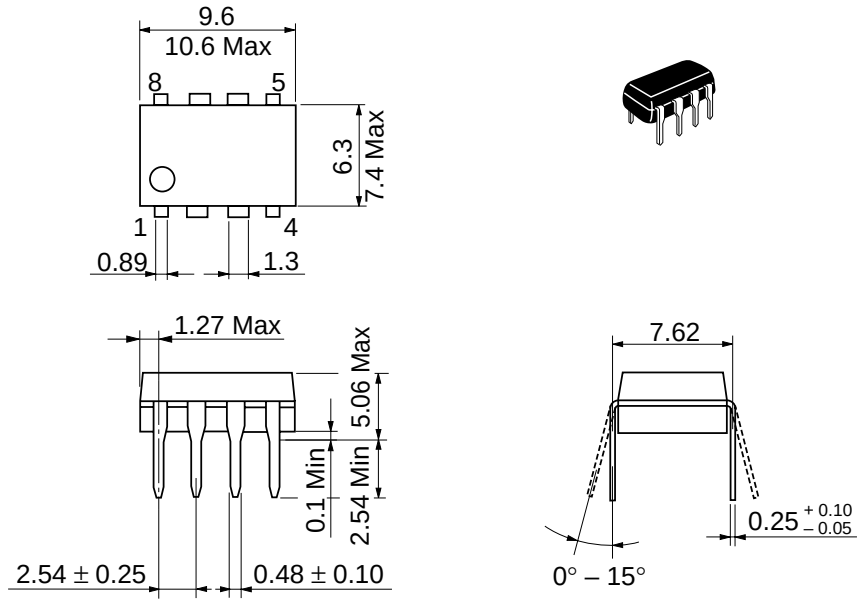
Lot Indication and Management Code Contents

1 : The last digit of the production year.
2 : Production month code
3 : Management code

Production month	1	2	3	4	5	6	7	8	9	10	11	12
Month code	A	B	C	D	E	F	G	H	J	K	L	M

Package Dimensions

Unit: mm



Hitachi Code	DP-8
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.54 g

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Hitachi, Ltd.
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Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
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For further information write to:

Hitachi Semiconductor (America) Inc.
179 East Tasman Drive,
San Jose,CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe GmbH
Electronic components Group
Dornacher Straβe 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building. No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX