

HA16150T/P

High-Speed Current Mode Push-Pull PWM Control IC

REJ03F0146-0300

Rev.3.00

Jan 30, 2007

Description

The HA16150 is a high-speed current mode PWM control IC with push-pull dual outputs, suitable for high-reliability, high-efficiency, high-mounting-density isolated DC-DC converter and high-output AC-DC converter control.

The HA16150 can be used in various applications, including push-pull converters and half-bridge, double-forward, and single-forward applications.

The HA16150 incorporates 180-degree phase-inverted push-pull dual outputs, and directly drives a power MOS FET. Operation at a maximum of 1 MHz is possible on an oscillator reference frequency.

The package lineup comprises an ultra-thin surface-mount TSSOP-16 suitable for slim communication system modules, and a general-purpose insertion DILP-6 suitable for characteristics evaluation.

Features

<Maximum Ratings>

- Supply voltage V_{CC} : 20 V
- Peak output current I_{pk-out} : ± 1.0 A
- Operating junction temperature T_{jopr} : -40°C to $+125^{\circ}\text{C}$

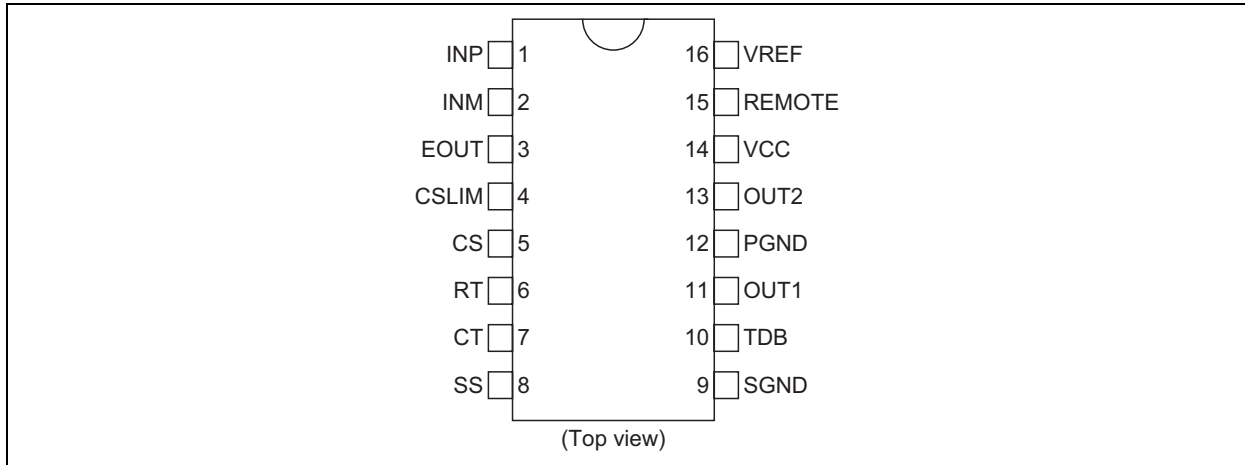
<Electrical Characteristics>

- VREF output voltage V_{REF} : $5.0\text{ V} \pm 1\%$
- UVLO start threshold V_H : $9.3\text{ V} \pm 0.7\text{ V}$
- UVLO shutdown threshold V_L : $8.3\text{ V} \pm 0.7\text{ V}$
- Operating current I_{CC} : 4 mA typ.
- Standby current I_S : 150 μA typ.

<Functions>

- Soft start (one external timing capacitance)
- Remote on/off control
- Independent dead band time adjustment
- Current limiter adjustment (set drooping characteristic adjustment)
- Push-pull/single-end output switching
- Package lineup: TSSOP-16/DILP-16

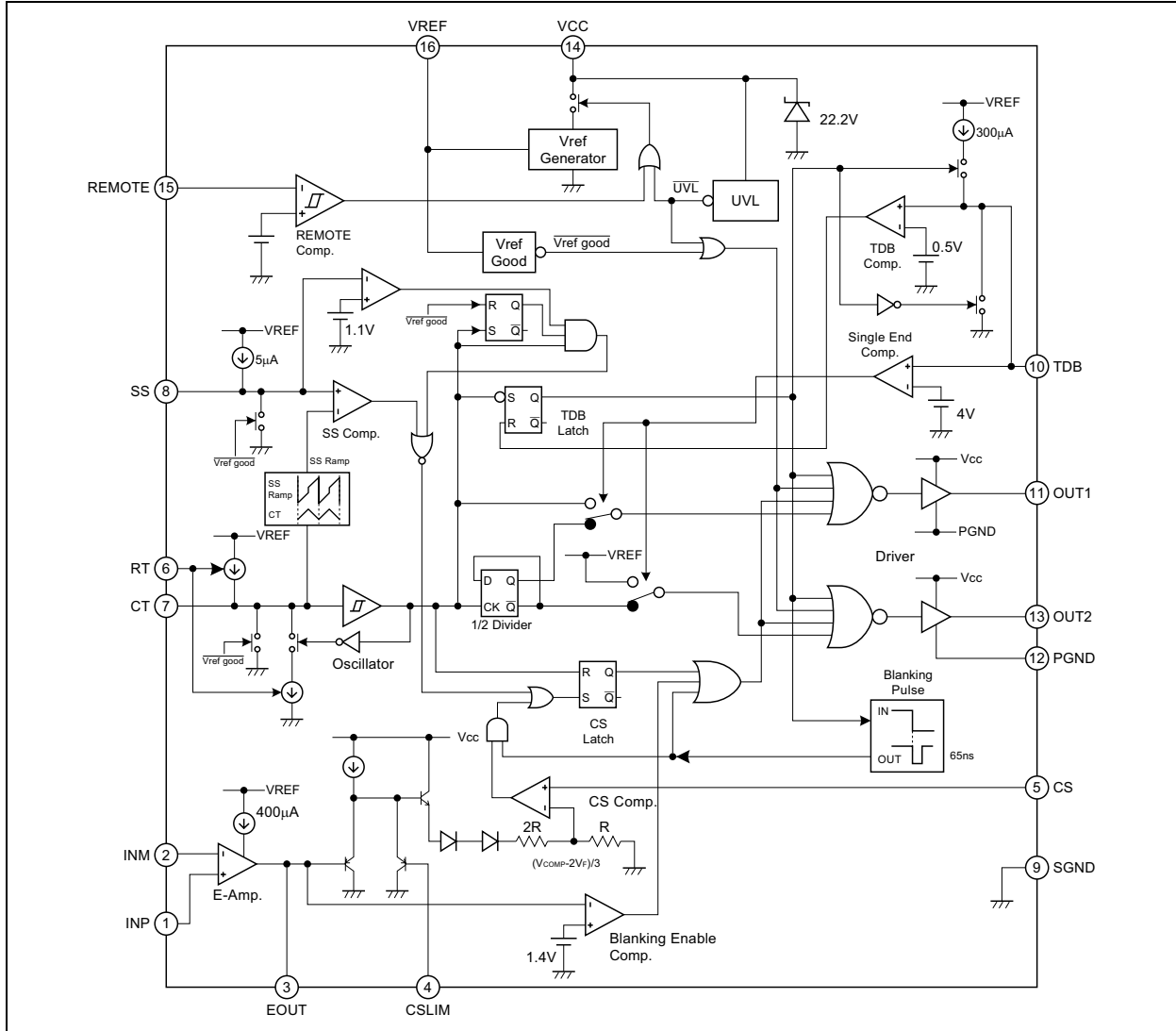
Pin Arrangement



Pin Functions

Pin No.	Pin Name	Pin Functions
1	INP	Error amplifier non-inverted (+) input
2	INM	Error amplifier inverted (-) input
3	EOUT	Error amplifier output
4	CSLIM	Current limiter level adjustment
5	CS	Current sense signal input
6	RT	Operating frequency setting resistance connection
7	CT	Operating frequency setting capacitance connection
8	SS	Soft start time setting timing capacitance connection
9	SGND	Small signal system ground
10	TDB	Dead band time setting timing capacitance connection
11	OUT1	Power MOS FET driver output 1
12	PGND	Power system ground
13	OUT2	Power MOS FET driver output 2
14	VCC	Supply voltage
15	REMOTE	Remote on/off control
16	VREF	Reference voltage

Block Diagram



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit	Note
Power supply voltage	Vcc	20	V	
OUT1 output current (peak)	Ipk-out1	±1.0	A	3
OUT2 output current (peak)	Ipk-out2	±1.0	A	3
OUT1 output current (DC)	I _{dc} -out1	±0.1	A	
OUT2 output current (DC)	I _{dc} -out2	±0.1	A	
OUT1 output voltage	Vout1	-0.3 to Vcc	V	
OUT2 output voltage	Vout2	-0.3 to Vcc	V	
INM pin voltage	V _{inm}	-0.3 to Vcc	V	
REMOTE pin voltage	V _{remote}	-0.3 to Vcc	V	
REMOTE pin current	I _{remote}	+0.2	mA	
INP pin voltage	V _{inp}	-0.3 to Vcc	V	
SS pin voltage	V _{ss}	-0.3 to Vref	V	
RT pin voltage	V _{rt}	-0.3 to Vref	V	
RT pin current	I _{rt}	-0.2	mA	
CT pin voltage	V _{ct}	-0.3 to Vref	V	
CSLIM pin voltage	V _{cslim}	-0.3 to Vref	V	
EOUT pin voltage	V _{eout}	-0.3 to Vref	V	
VREF pin voltage	V _{ref}	-0.3 to Vref	V	
TDB pin voltage	V _{tdb}	-0.3 to Vref	V	
CS pin voltage	V _{cs}	-0.3 to Vref	V	
Operating junction temperature	T _{j-opr}	-40 to +125	°C	4
Storage temperature	T _{stg}	-55 to +150	°C	

- Notes: 1. Rated voltages are with reference to the GND (SGND, PGND) pin.
 2. For rated currents, inflow to the IC is indicated by (+), and outflow by (-).
 3. Shows the transient current when driving a capacitive load.
 4. HA16150T (TSSOP): $\theta_{ja} = 250^{\circ}\text{C/W}$
 This value is based on actual measurements on a 110% wiring density
 glass epoxy circuit board (55 mm × 45 mm × 1.6 mm).
 HA16150P (DILP): $\theta_{ja} = 124^{\circ}\text{C/W}$

Electrical Characteristics

(Ta = 25°C, Vcc = 12 V, Fosc = 100 kHz)

	Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Supply	Start threshold	VH	8.6	9.3	10.0	V	
	Shutdown threshold	VL	7.6	8.3	9.0	V	
	UVLO hysteresis	dV _{UVL}	0.7	1.0	1.3	V	
	Start-up current	I _s	100	150	250	μA	V _{cc} = 8V
	Operating current	I _{cc}	–	4	6	mA	V _{inm} = 1.0V, V _{inp} = 1.25V, V _{cs} = 0V
	V _{cc} zener shunt voltage	V _z	21.2	22.2	23.2	V	I _{cc} = 10mA
	V _z temperature stability	dV _z /dT _a	–	4.5	–	mV/°C	I _{cc} = 10mA * ¹
VREF	Output voltage	V _{ref}	4.95	5.0	5.05	V	I _{ref} = –1mA
	Line regulation	V _{ref} -line	–	5	20	mV	V _{cc} = 11V to 18V
	Load regulation	V _{ref} -load	–	5	20	mV	I _{ref} = –1mA to –20mA
	Temperature stability	dV _{ref} /dT _a	–	80	–	ppm/°C	T _a = –40 to 125°C
Oscillator	Oscillator frequency	f _{osc}	88	100	112	kHz	Measured at OUT1 and OUT2 RT = 27kΩ, CT = 1000pF
	Temperature stability	df _{osc} /dT _a	–	±0.1	–	%/°C	T _a = –40 to 125°C * ¹
PWM Comparator	High voltage	V _{th}	–	3.0	–	V	DC * ¹
	Low voltage	V _{tl}	–	2.0	–	V	DC * ¹
	Differential voltage	dV _t	–	1.0	–	V	DC * ¹
Error amplifier	Input bias current	I _{fb}	–1	–	+1	μA	
	Open loop gain	A _v	–	70	–	dB	f = 1.0kHz * ¹
	EOUT sink current	I _{snk-eout}	–	3.0	–	mA	V _{eout} = 1.1V * ¹
	EOUT source current	I _{src-eout}	–	–0.4	–	mA	V _{eout} = 3.0V * ¹
	Low voltage	V _{ol-eout}	–	0.8	1.1	V	EOUT : Open
	High voltage	V _{oh-eout}	4.7	5.0	–	V	EOUT : Open
Current sense	Voltage gain	A _{vcs}	2.85	3.00	3.15	V/V	
	Delay to output	t _{d-cs}	–	150	230	ns	
	Leading edge blanking time	t _{bl}	–	65	–	ns	* ¹
	Leading edge blanking disable voltage	V _{bl-off}	1.3	1.4	1.5	V	Measured pin : EOUT
Remote	On threshold voltage	V _{on}	1.40	–	–	V	* ¹
	Off threshold voltage	V _{off}	–	–	3.00	V	* ¹
	Sink current	I _{remote}	60	90	120	μA	V _{remote} = 4V
Soft start	Source current	I _{ss}	–7.0	–5.0	–3.0	μA	V _{ss} = 1V

Note: 1. Reference values for design.

Electrical Characteristics (cont.)

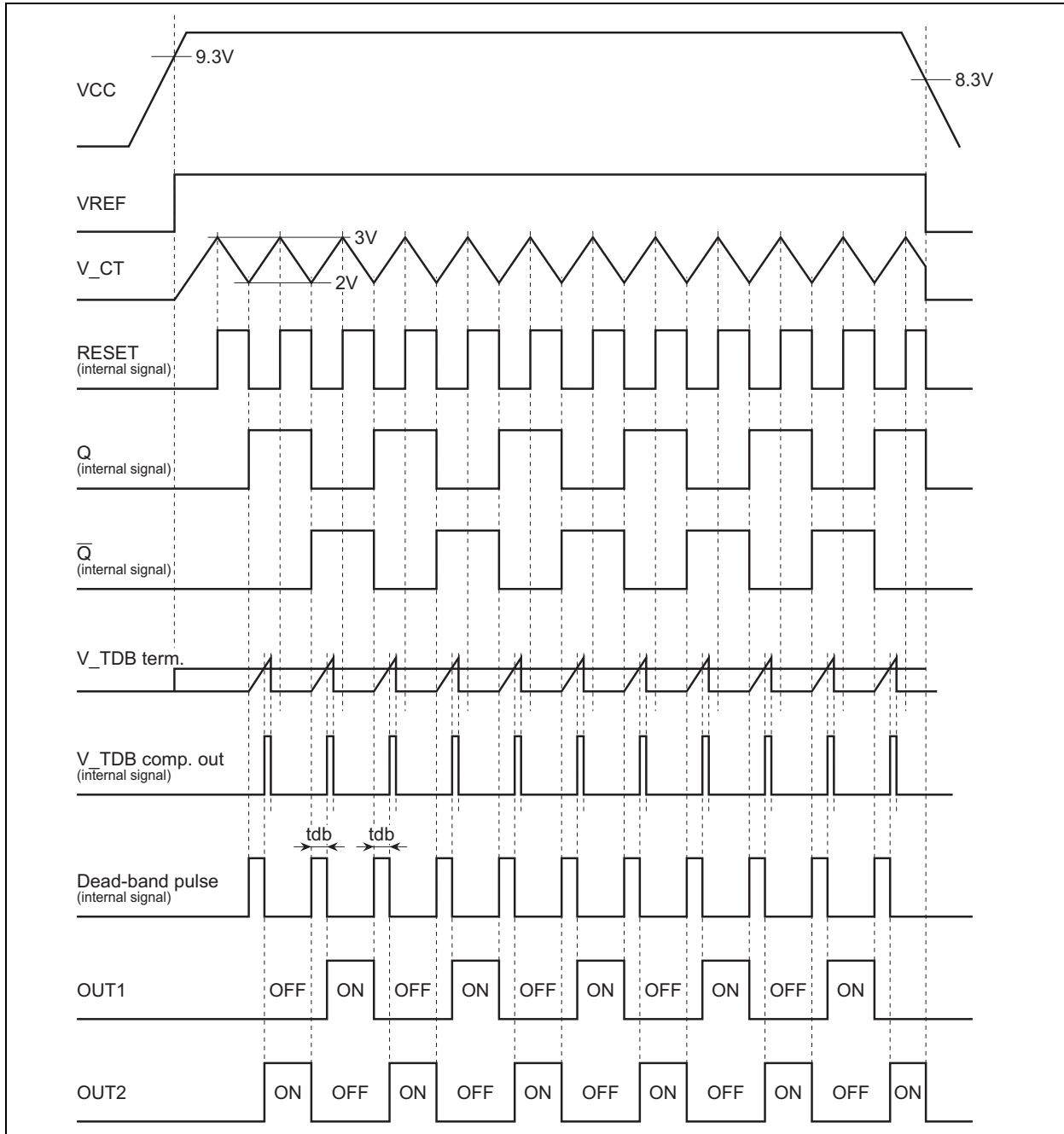
(Ta = 25°C, Vcc = 12 V, Fosc = 100 kHz)

	Item	Symbol	Min	Typ	Max	Unit	Test Conditions
OUT1	Minimum duty cycle	Dmin-out1	–	–	0	%	Veout = 0V
	Maximum duty cycle	Dmax-out1	48	49	–	%	TDB : OPEN
	Rise time	tr-out1	–	30	65	ns	CL = 1000pF
	Fall time	tf-out1	–	30	65	ns	CL = 1000pF
	Low voltage	Vol1-out1	–	0.05	0.2	V	Iout = 20mA
		Vol2-out1	–	0.5	2.0	V	Iout = 200mA (pulse)
	High voltage	Voh1-out1	11.5	11.9	–	V	Iout = –20mA
Voh2-out1		10.0	11.0	–	V	Iout = –200mA (pulse)	
OUT2	Minimum duty cycle	Dmin-out2	–	–	0	%	Veout = 0V
	Maximum duty cycle	Dmax-out2	48	49	–	%	TDB : OPEN
	Rise time	tr-out2	–	30	65	ns	CL = 1000pF
	Fall time	tf-out2	–	30	65	ns	CL = 1000pF
	Low voltage	Vol1-out2	–	0.05	0.2	V	Iout = 20mA
		Vol2-out2	–	0.5	2.0	V	Iout = 200mA (pulse)
	High voltage	Voh1-out2	11.5	11.9	–	V	Iout = –20mA
Voh2-out2		10.0	11.0	–	V	Iout = –200mA (pulse)	
Dead-band time	Dead-band time	tdb0	–	60	–	ns	TDB : OPEN *1
		tdb	–	140	–	ns	Ctdb = 47pF *1

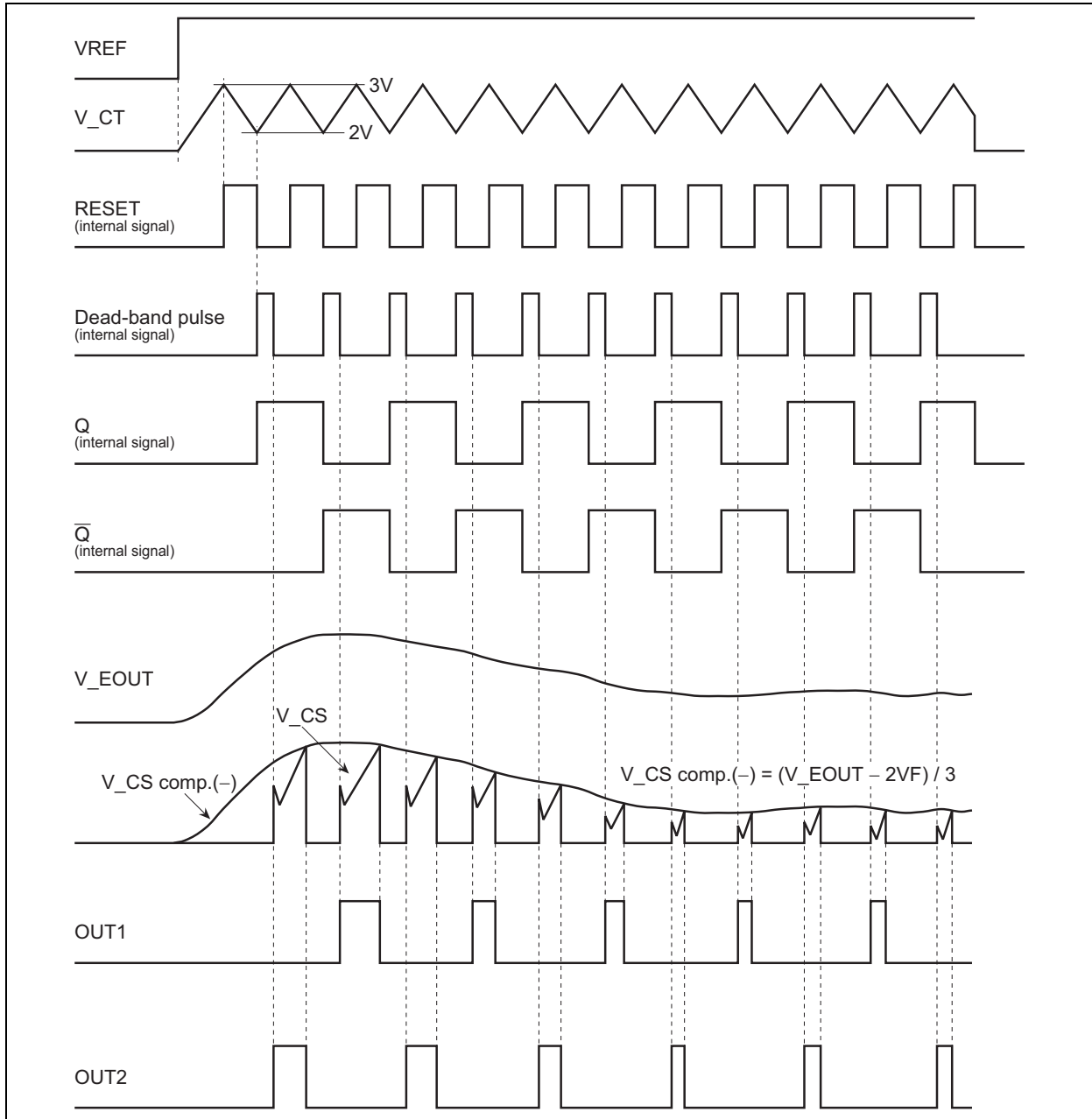
Note: 1. Reference values for design.

Timing Diagram

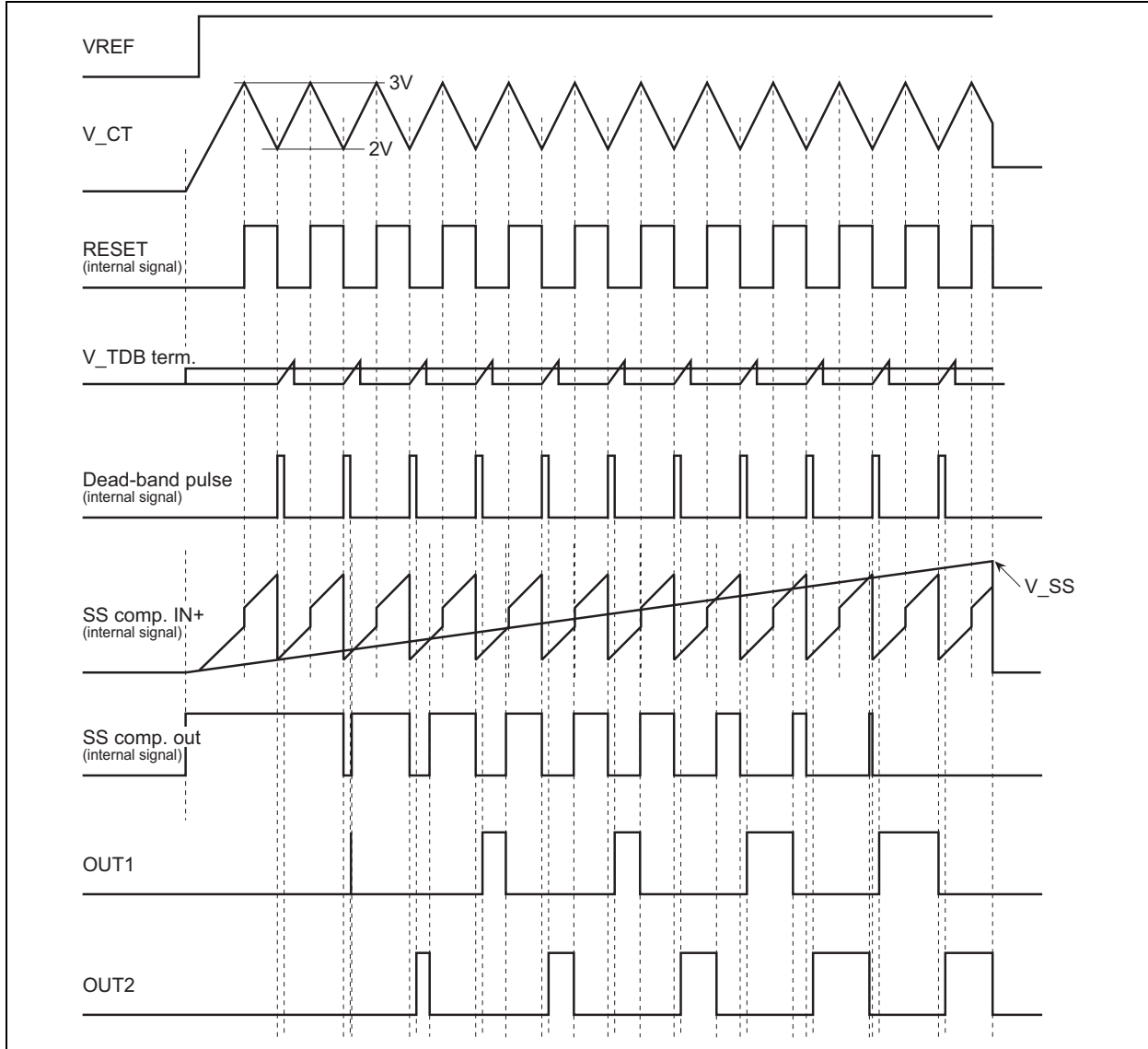
1. Start-up Timing



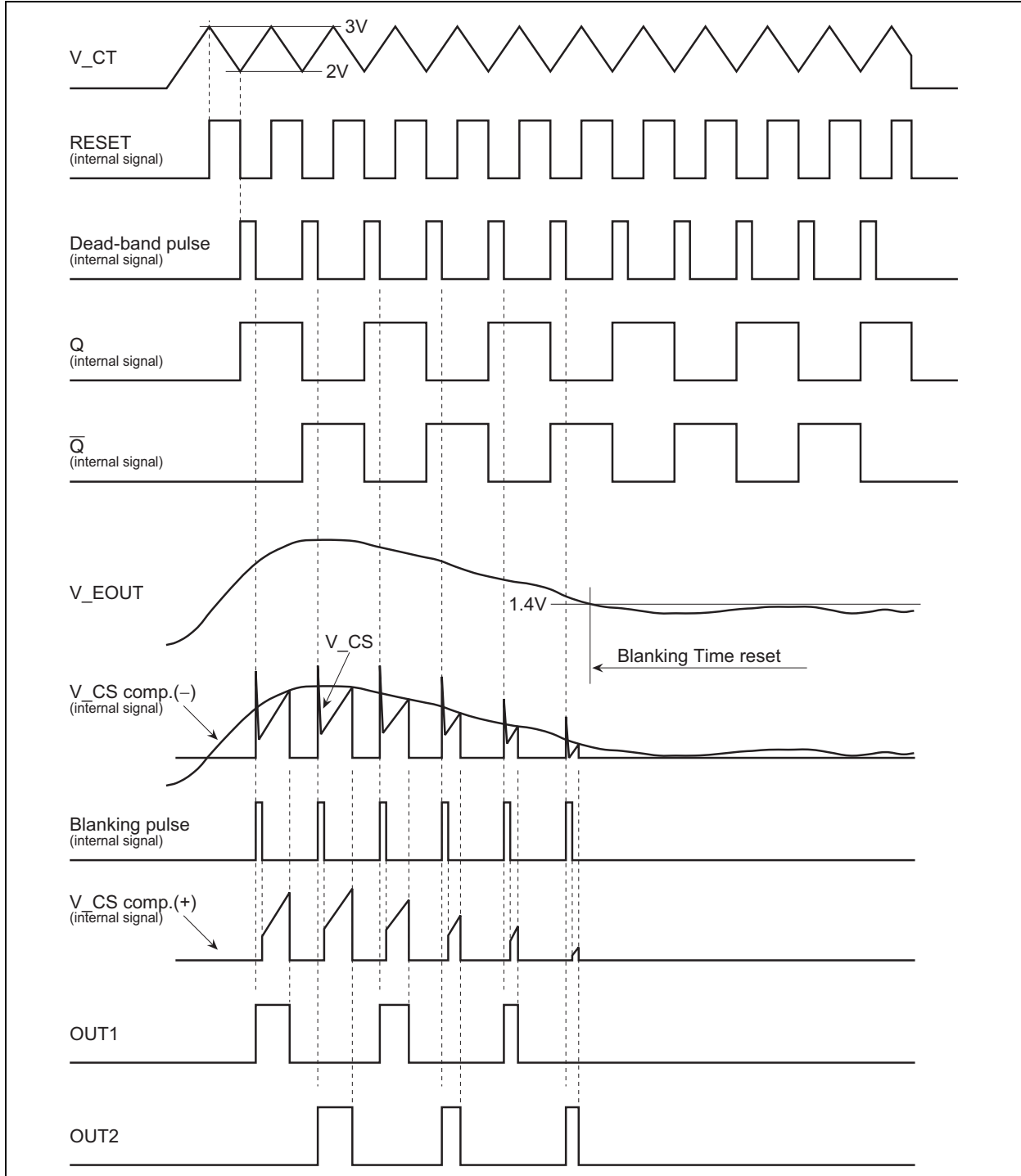
2. Current Sense



3. Soft Start

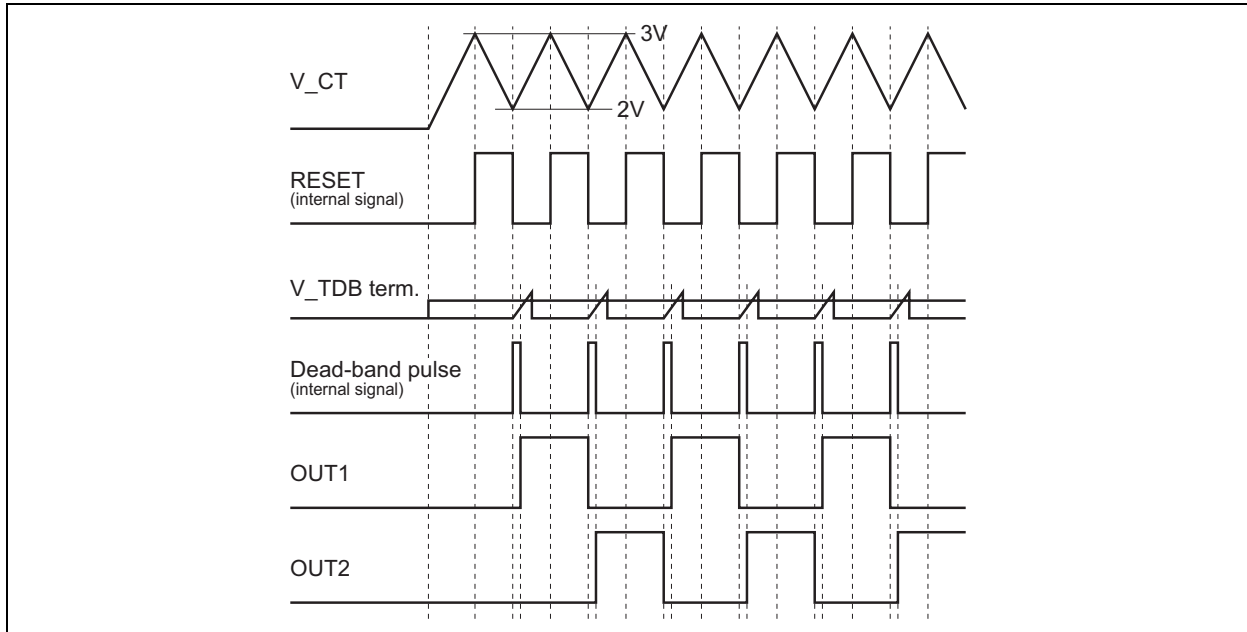


4. Leading Edge Blanking

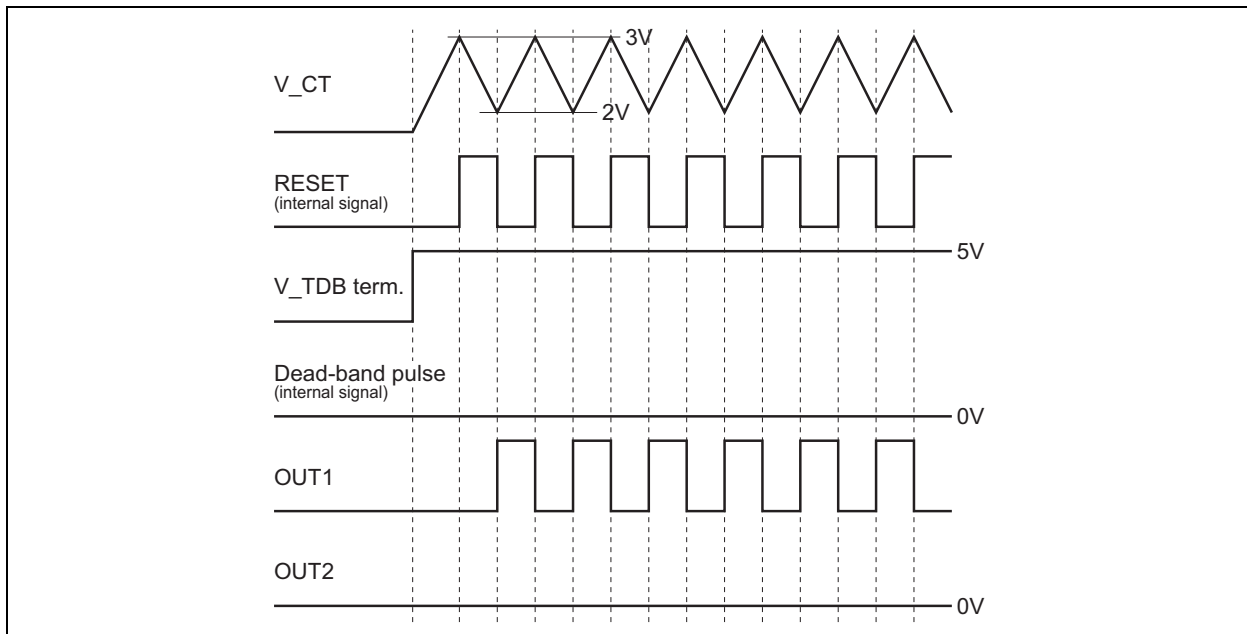


5. Push-Pull/Single-End Switching

(1) Push-pull operation: Leave the TDB pin open or connect a capacitance to GND



(2) Single-end operation: Perform pull-up connection of the TDB pin to the VREF pin



Functional Description

1. UVL Circuit

The UVL circuit monitors the Vcc voltage and halts operation of the IC in the event of a low voltage.

The voltage for detecting Vcc has a hysteresis characteristic, with 9.3 V as the start threshold and 8.3 V as the shutdown threshold.

When the IC has been halted by the UVL circuit, control is performed to fix driver circuit output low, halt VREF output and the oscillator, and reset the soft start circuit.

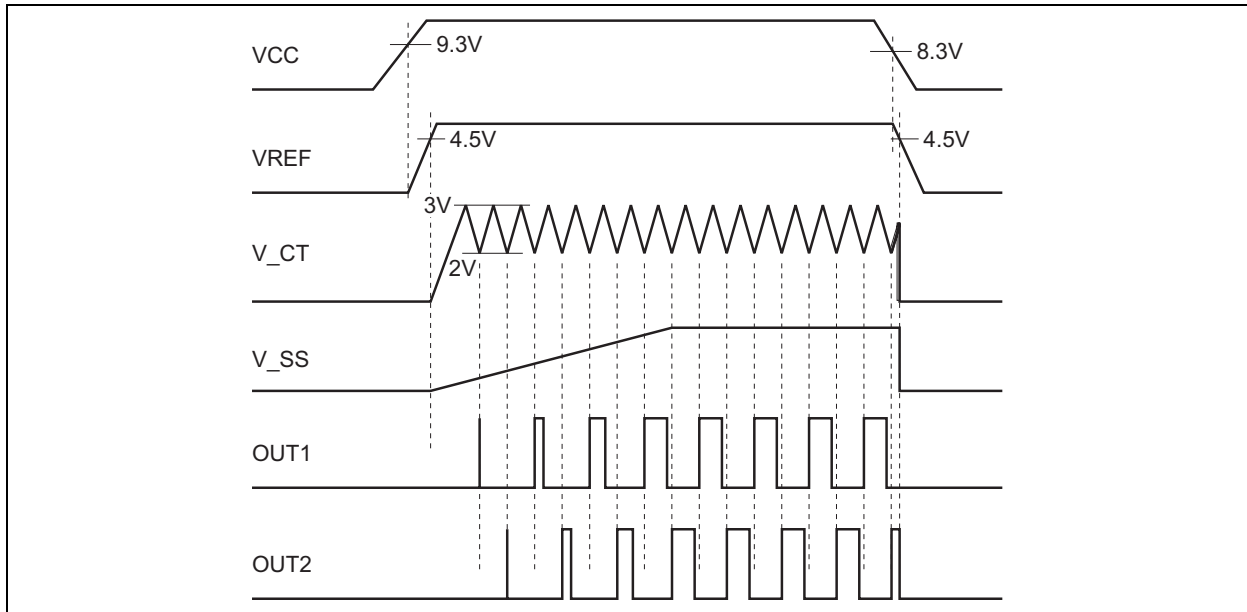


Figure 1

2. Remote ON/OFF Circuit

A remote on/off control function is incorporated, enabling the IC to be halted without cutting the supply voltage by pulling the REMOTE pin up to 3.0 V or higher.

This function halts VREF output and driver output.

At this time the IC enters Remote-OFF mode and IC current dissipation can be decreased. This function can thus be used for power management, etc.

When remote off control is performed, the soft start circuit is also reset, and therefore a soft start is effected when restarting, preventing overshoot.

However, when restarting by the remote on control function before the SS pin is completely discharged, soft start operation may not be performed normally. In such a case, add a circuit to pull the SS pin out in conjunction with a remote off signal.

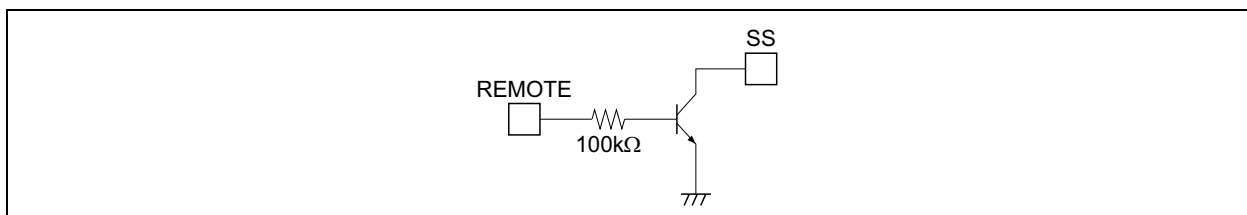


Figure 2 Example of Circuit to Pull out SS Pin

If the remote on/off control function is not used, the REMOTE pin should be permanently pulled down to GND with a resistance of about 100 kΩ.

The remote on/off control function halts only reference voltage. Other functions will be stopped when the reference voltage is below 4.5 V (typ.). Large stabilizing capacitance of the VREF pin results in a difference between the timing of remote off signal and the timing to stop the IC

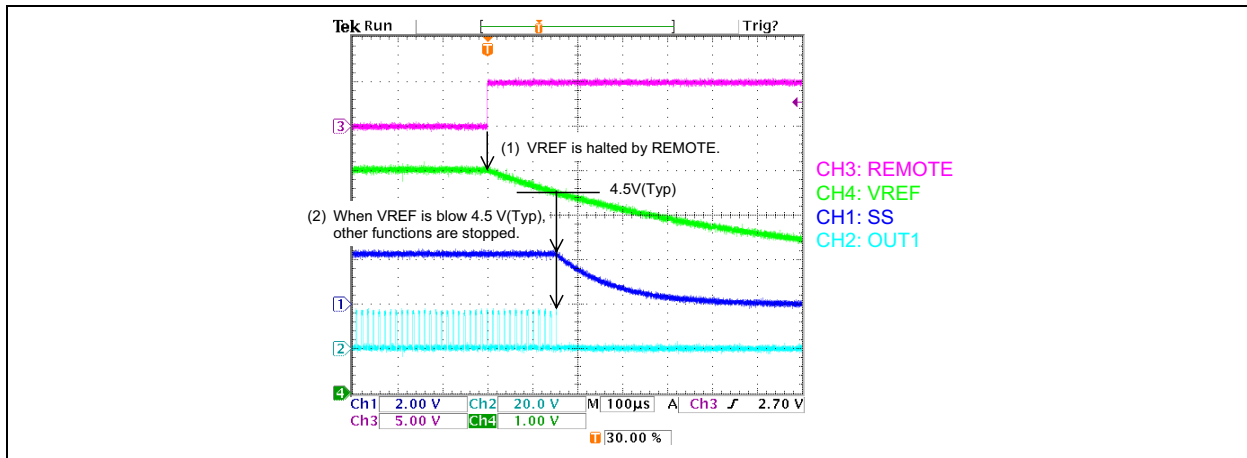


Figure 3 Operation When Remote is Off (Reference Data)

3. Soft Start Circuit

This function gradually increases the pulse width of the OUT pin from 0% duty at start-up to prevent a sudden increase in the pulse width that may cause problems such as transient stress on external parts or overshoot of the secondary-side output voltage.

The soft start time can easily be set with a single external capacitance.

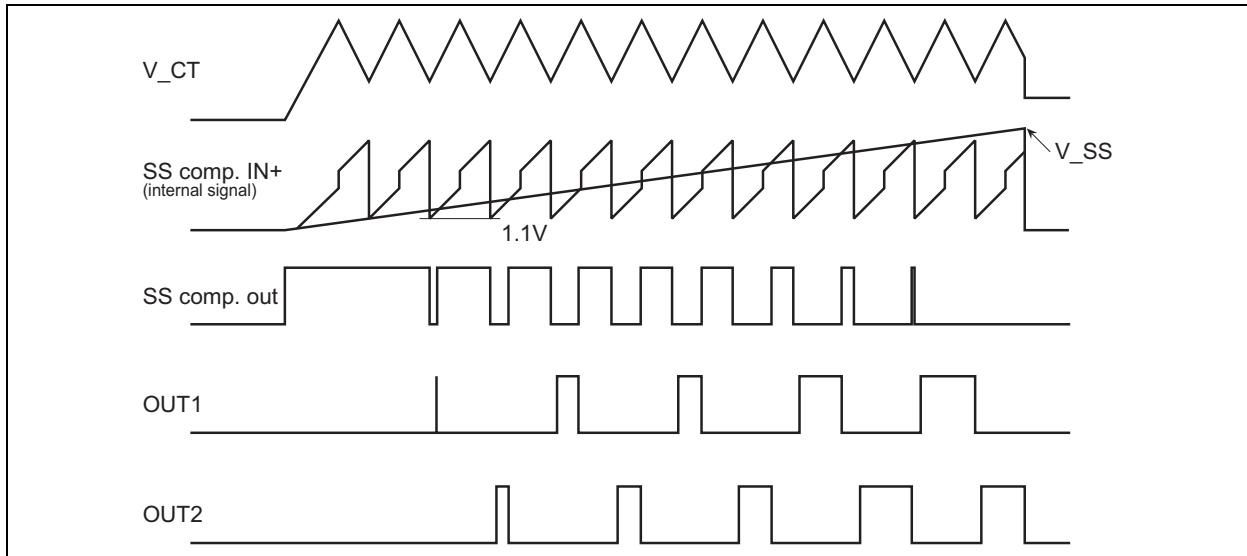


Figure 4

Soft start time t_{ss} is determined by SS pin connection capacitance C_{ss} and an internal constant, and can be estimated using the equation shown below.

Soft start time t_{ss} is the time until the first pulse is output to the driver output OUT pin after VREF starts up following UVLO release.

This is equivalent to the time until the SS pin voltage reaches IC-internal SS comparator reference voltage VTL (1.1 V), and can be calculated using the approximate equation shown below.

Soft start time t_{ss} when C_{ss} is 1000pF is given by the following equation.

$$t_{ss} = \frac{C_{ss} \times V_{TL}}{I_{ss}} = \frac{1000 \text{ [pF]} \times 1.1 \text{ [V]}}{5 \text{ [\mu A]}}$$

$$\approx 220 \text{ [\mu s]}$$

* I_{ss} : SS pin source current, 5 μ A typ.

Note: A soft start circuit operates only once at the start-up of the IC (after the VREF pin voltage is launched and the VrefGOOD circuit is operated). If the SS pin is lowered to 1.1 V or less after the SS pin becomes once high, the pulse of OUT1 and OUT2 is not halt. Each duty cycle of OUT1 and OUT2 is fixed to 25%.

4. Dead Band Generation Circuit

"Dead band" refers to the time when both push-pull dual outputs are off.

By setting the dead band time arbitrarily, it is possible to configure a system in which the dual outputs are never on simultaneously with respect to input and load variations.

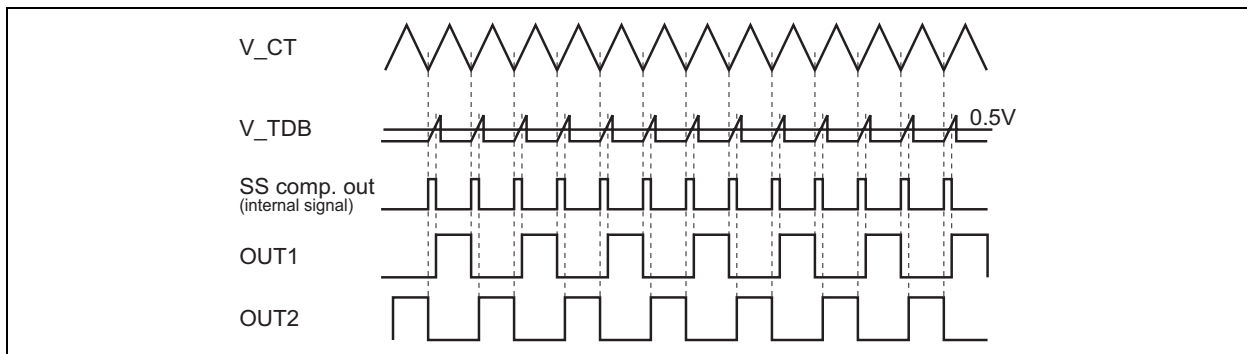


Figure 5

Dead band time t_{db} is determined by TDB pin connection capacitance C_{db} and an internal constant, and can be estimated using the equation shown below.

Even when the TDB pin is open, the dead band time does not become zero due to floating capacitance of the IC package, etc. This dead band time is designated t_{db0} .

Dead band time t_{db} when C_{db} is 47 pF is given by the following equation.

$$t_{db} = t_{db0} + \frac{C_{db} \times V_{th}}{I_{db}} = t_{db0} + \frac{47 \text{ [pF]} \times 0.5 \text{ [V]}}{300 \text{ [\mu A]}}$$

$$= 60 \text{ [ns]} + 78 \text{ [ns]}$$

$$= 138 \text{ [ns]}$$

* I_{db} : TDB pin source current, 300 μ A typ.

* V_{th} : IC-internal TDB comparator reference voltage

5. Operating Frequency

The operating frequency is adjusted by means of CT and RT.

Adjustment examples are shown in the graph below. This graph shows driver output operating frequencies. The reference operating frequency generated at the CT pin is twice the driver output frequency.

The driver output operating frequency can be estimated using the approximate equation shown below.

This is only an approximate equation, and the higher the frequency, the greater will be the degree of error of the approximate equation due to the effects of CT pin voltage overshoot, undershoot and so forth.

When the operating frequency is adjusted, it is essential to confirm operation using the actual system.

$$\begin{aligned} f_{osc} &= \frac{8}{3 \times CT \times RT} = \frac{8}{3 \times C6 \times R7} \\ &= \frac{8}{3 \times 470 \text{ [pF]} \times 27 \text{ [k}\Omega\text{]}} \\ &= 210 \text{ [kHz]} \end{aligned}$$

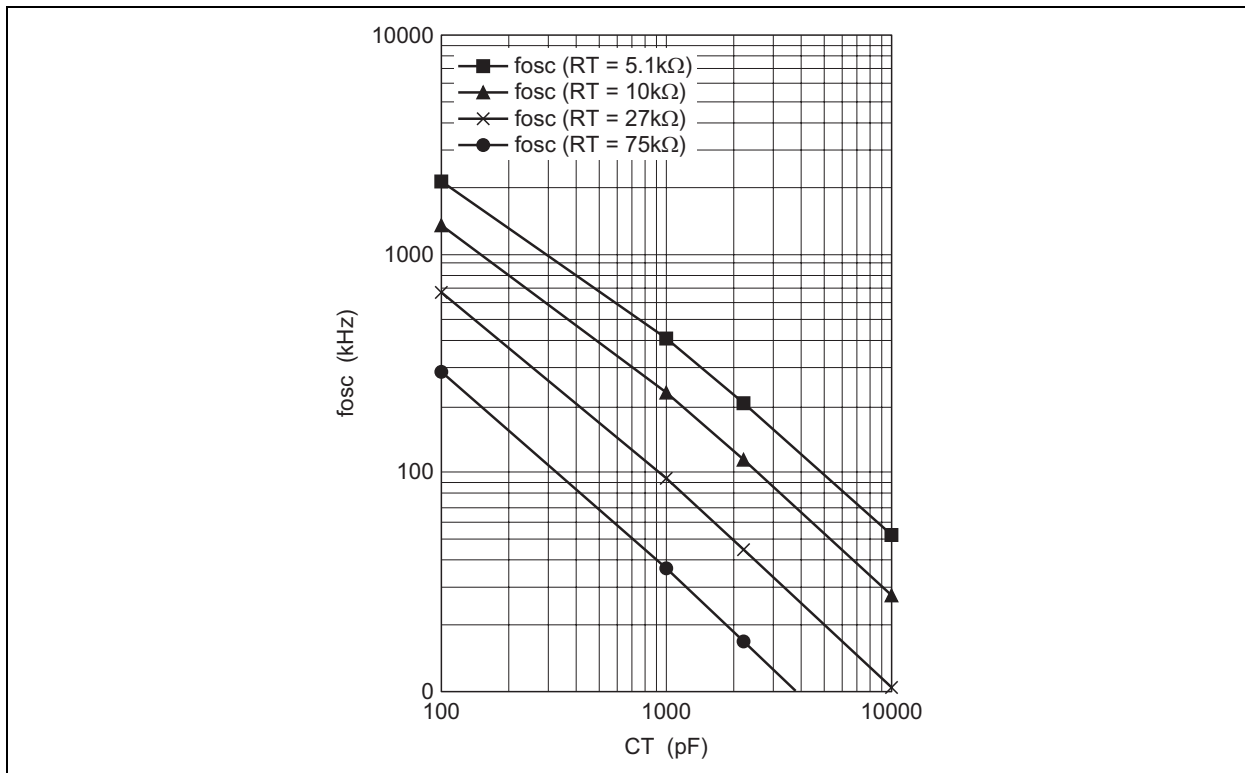


Figure 6

6. Current Limiter Level

The drooping characteristic of the power supply output can be adjusted by adjusting the CSLIM pin voltage.

For example, the drooping characteristic can easily be adjusted, as shown in the figure below, by setting VREF to a divided value with resistances R1 and R2 and connecting adjustment resistance Rx in parallel to R2.

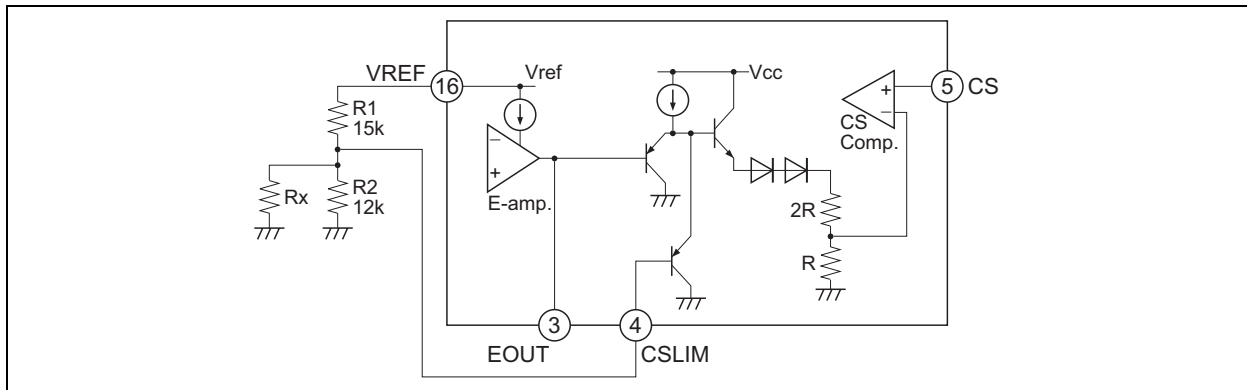


Figure 7 CSLIM Peripheral Circuit

The graph below shows examples of power supply output drooping characteristic adjustment in a push-pull converter.

As shown in this graph, the point at which the power supply output current limit begins to be applied can be adjusted by adjustment of the CSLIM pin voltage.

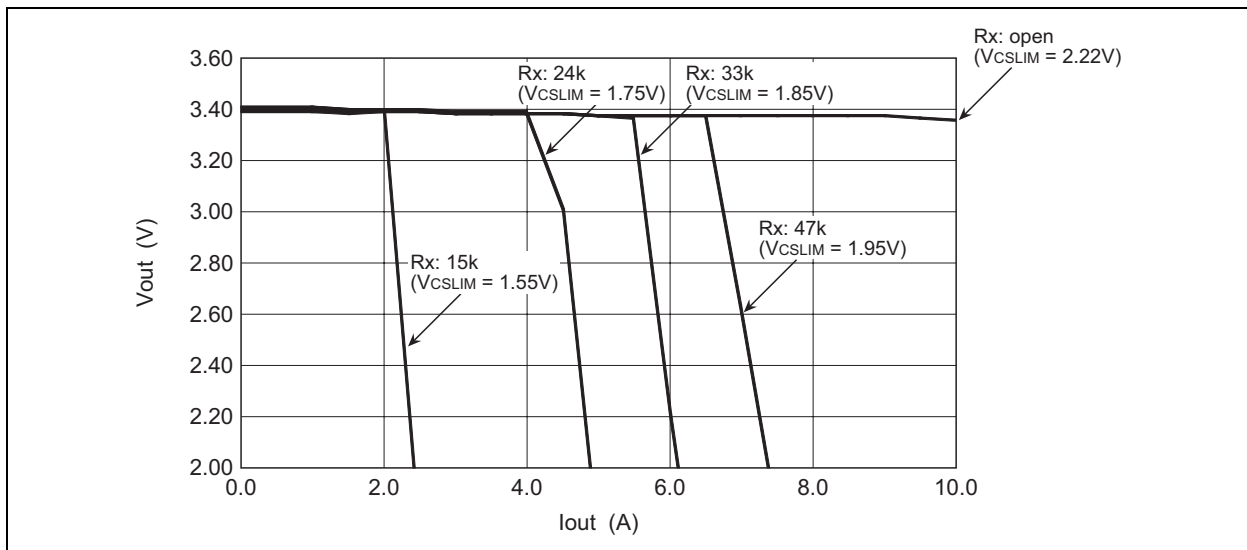


Figure 8 Adjustment of Power Supply Output Drooping Characteristic

7. VREF Circuit

- (1) For the VREF pin, make sure to connect stabilizing capacitance to GND.
- (2) When the value of stabilizing capacitance is small or the load of VREF pin is heavy, either OUT1 or OUT2 may be halted at high level if the IC is stopped by a remote off function. In such a case, increase the capacitance value. The minimum value of capacitance to be connected is approximated by the following equation.

$$C_{ref} > \frac{10\mu\text{s} \times (I_{ref} + 6\text{mA})}{4.95\text{V}}$$

- (3) Depending on the value of capacitance to be connected, overshoot may result at the rising of the VREF pin (see the figure below). Take extra care when the VREF pin voltage is used as the power supply and reference voltage of external circuit.

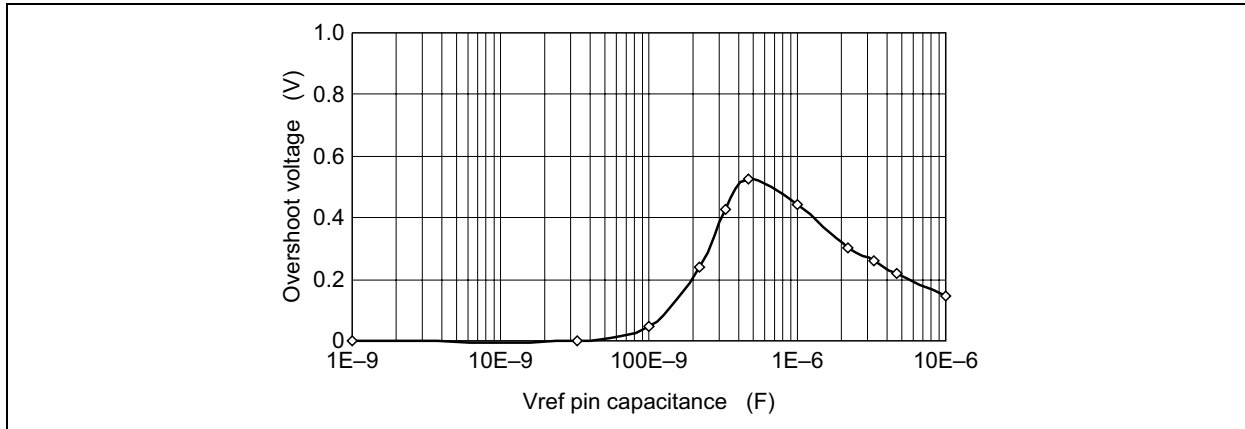


Figure 9 Overshoot Voltage of Vref Pin (Reference Data)

8. CS Pin

RC filter is generally inserted into the CS pin to prevent the pin from malfunction due to noise. The CS pin has an internal circuit to pull out electric charge while both of the OUT1 and OUT2 are at the low level (dead band time). However, please be aware that the electric charge may not be pulled out when the duration of dead band time is short and the filter constant is not appropriate.

9. Usage on Half-bridge Power Supply

The HA16150 is operated in the current mode. However, the half-bridge power supply becomes unstable in principle by using current mode control. The HA16150, therefore, cannot be used basically. In order to use the HA16150 with the half-bridge power supply, add a circuit as shown below and operate the HA16150 in the voltage mode.

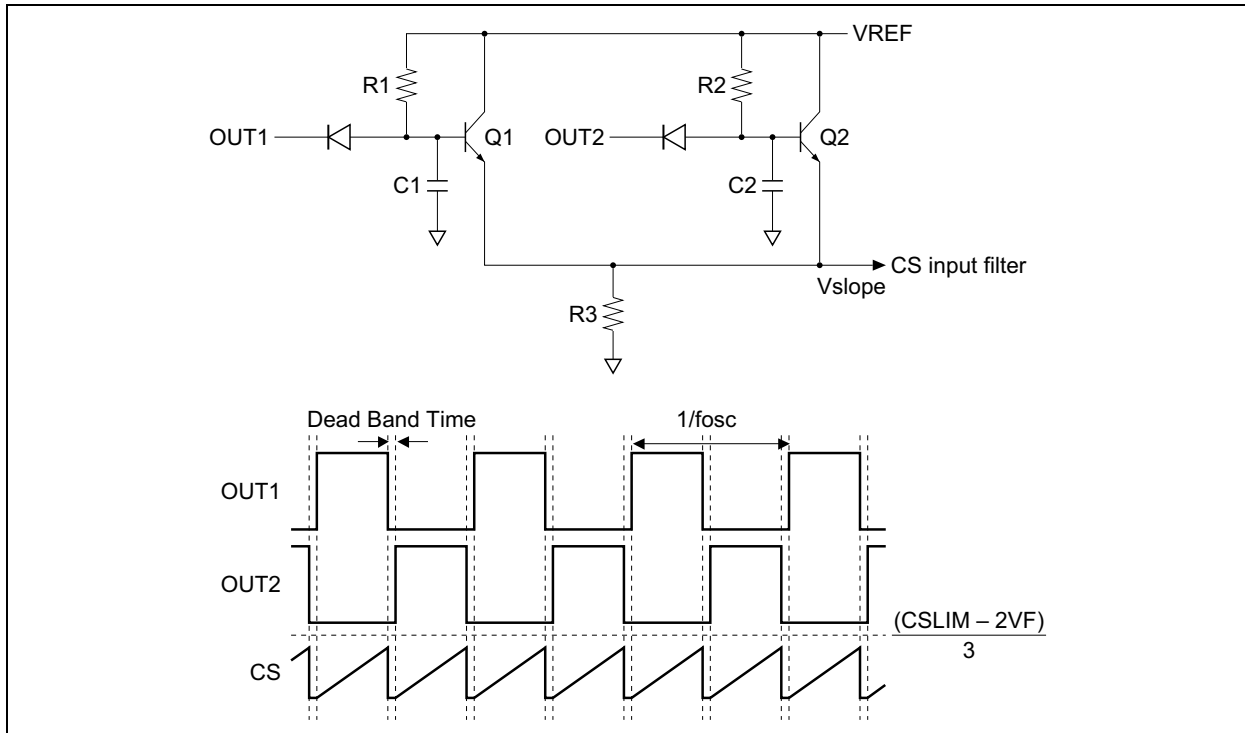
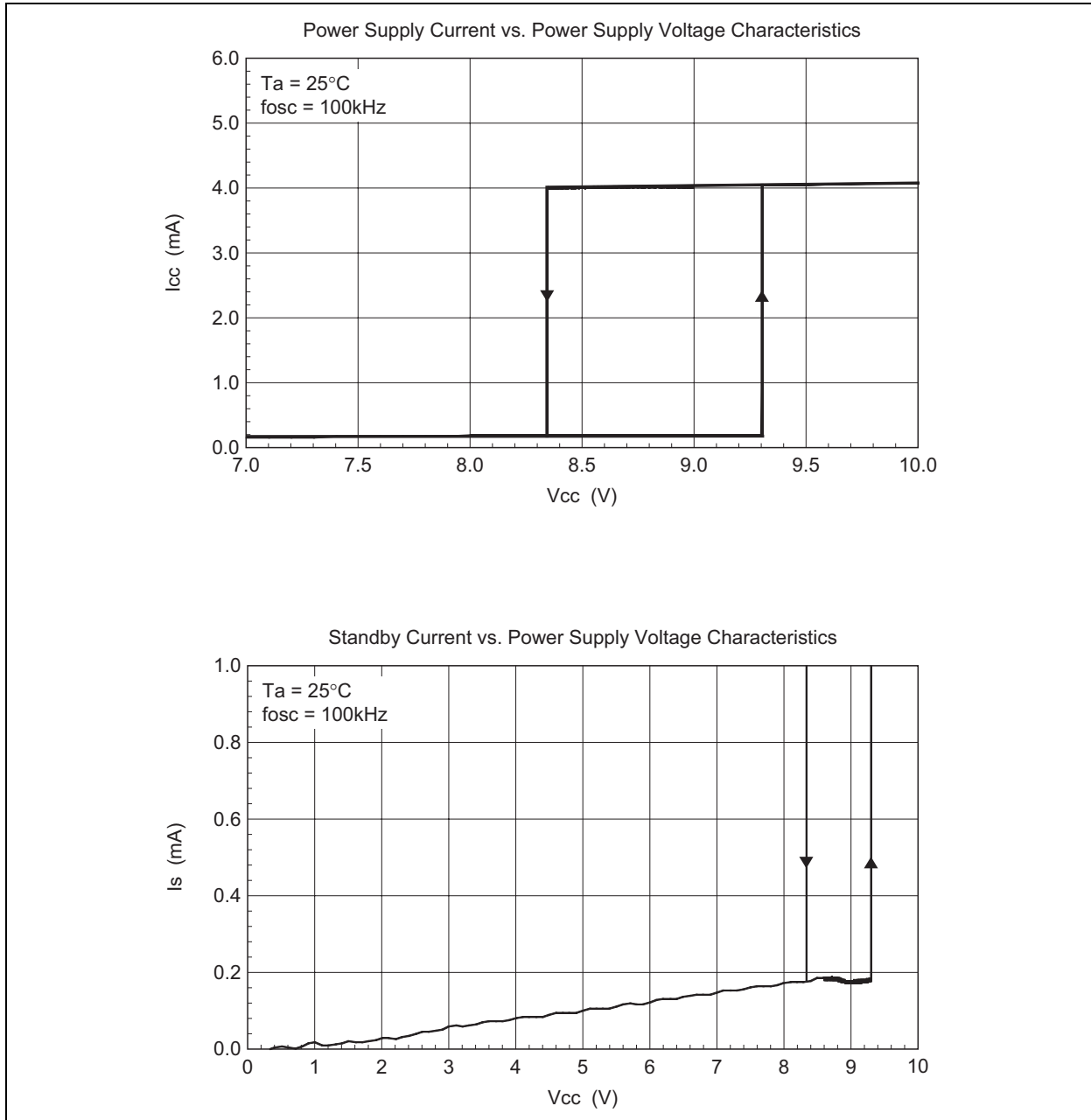


Figure 10 Example of Circuit for Voltage Mode Operation

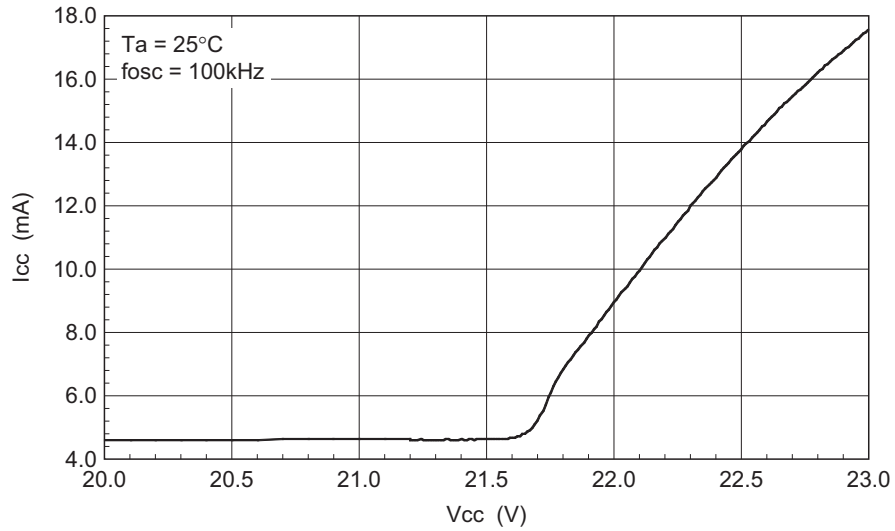
Design the charging circuits for R1 (R2), C1 (C2), Q1 (Q2) and R3 so that the peak voltage of CS is lower than $(CSLIM - 2VF)/3$ at the maximum ON pulse width of OUT1 and OUT2.

Furthermore, set the input filter values between R3 and CS pin so that the CS voltage is discharged assuredly while both of the OUT1 and OUT2 are at low level.

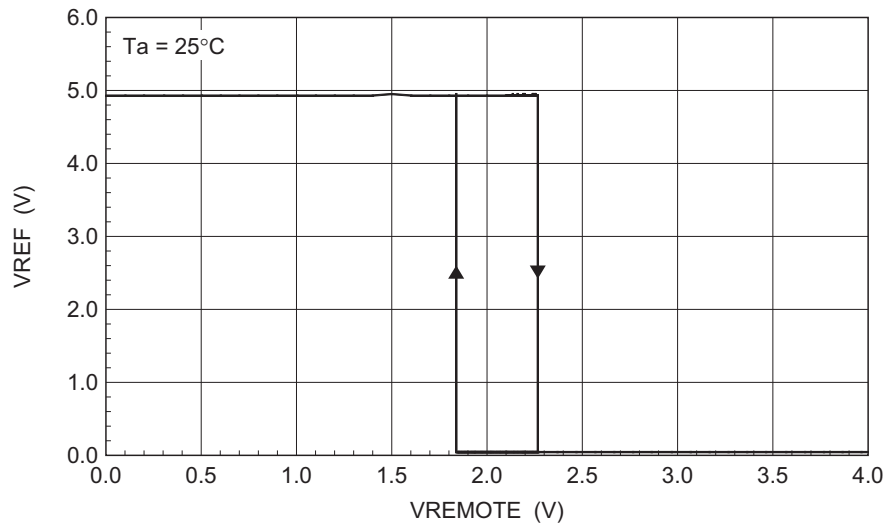
Characteristic Curves

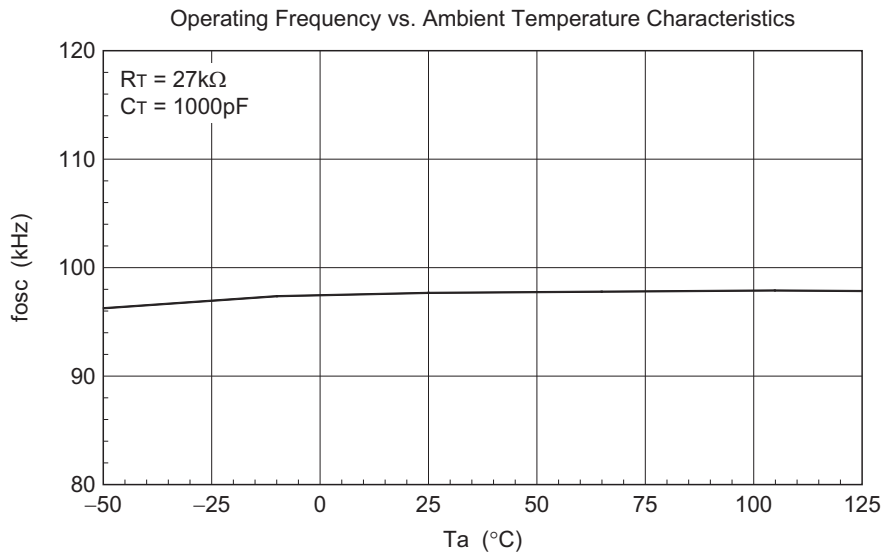
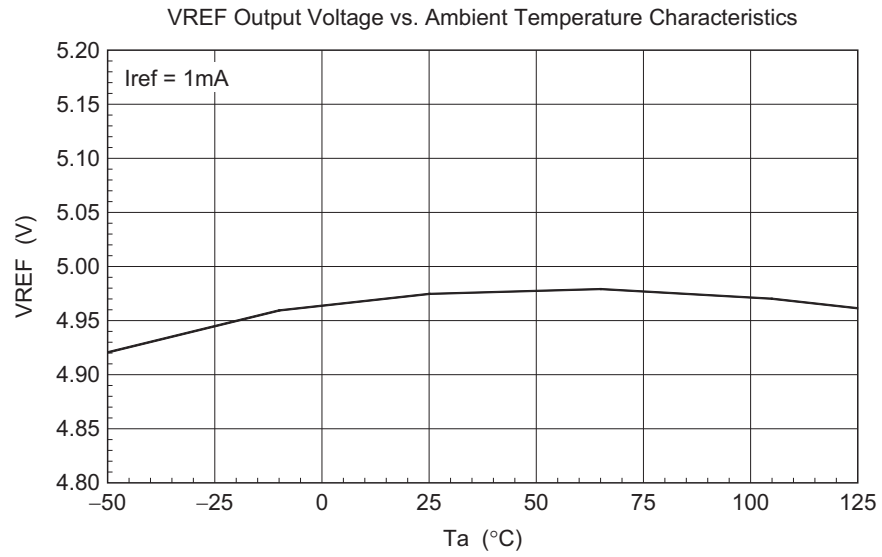


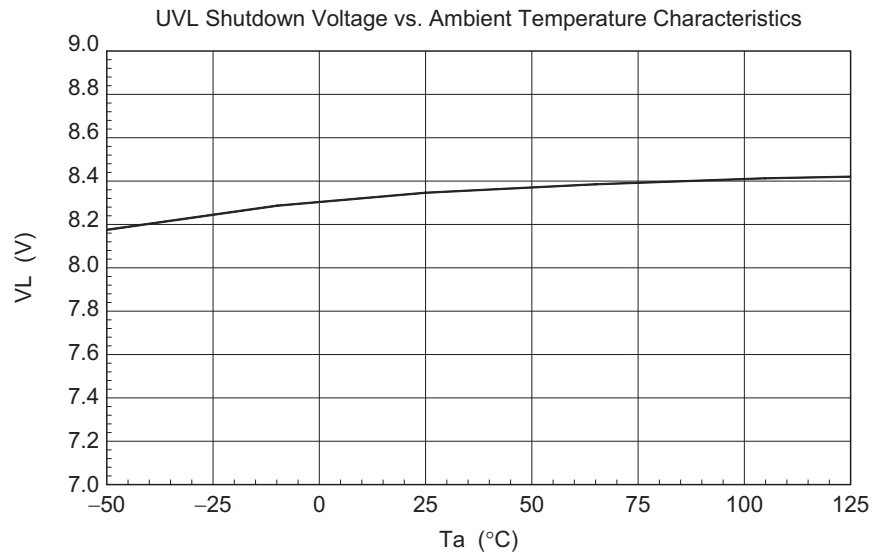
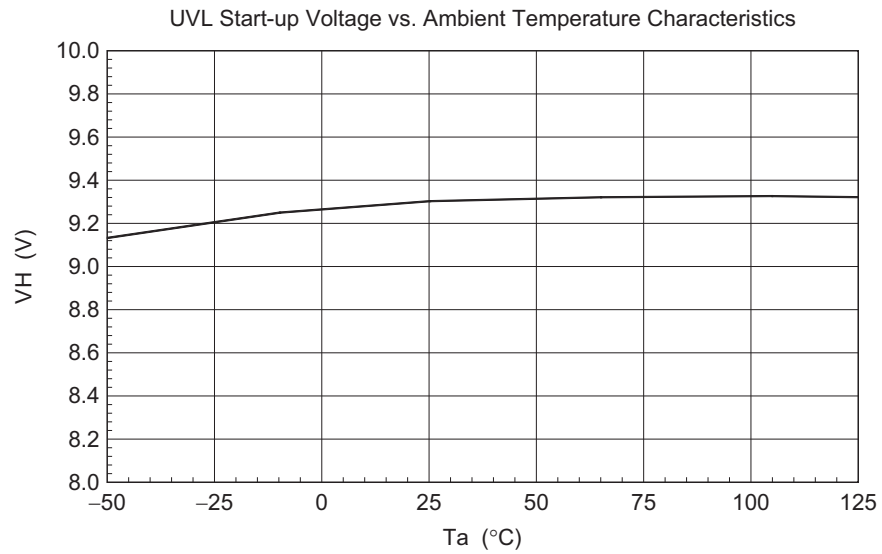
Power Supply Current vs. Power Supply Voltage (Clamp Zener Voltage) Characteristics



VREF Output Voltage vs. REMOTE Pin Voltage Characteristics

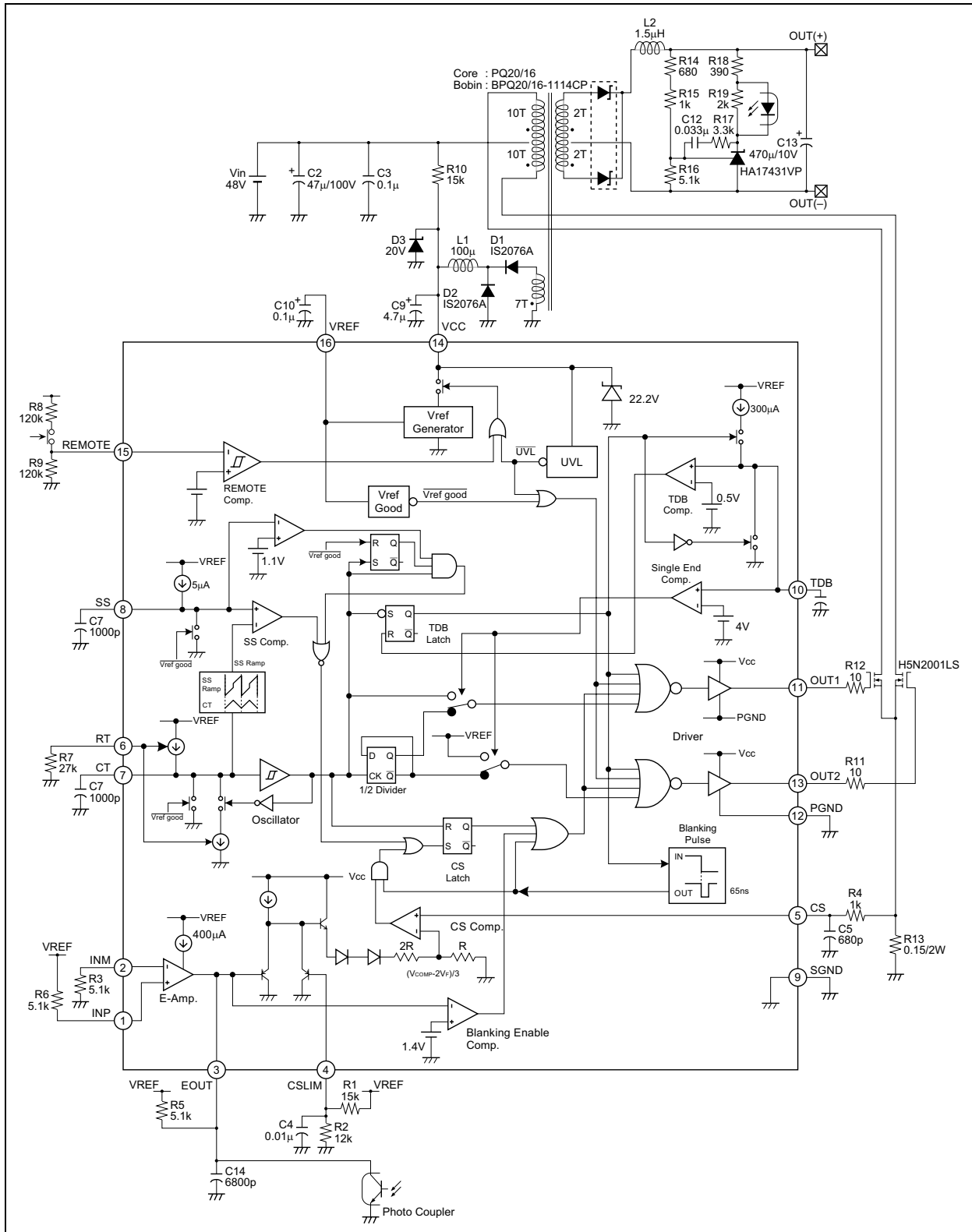




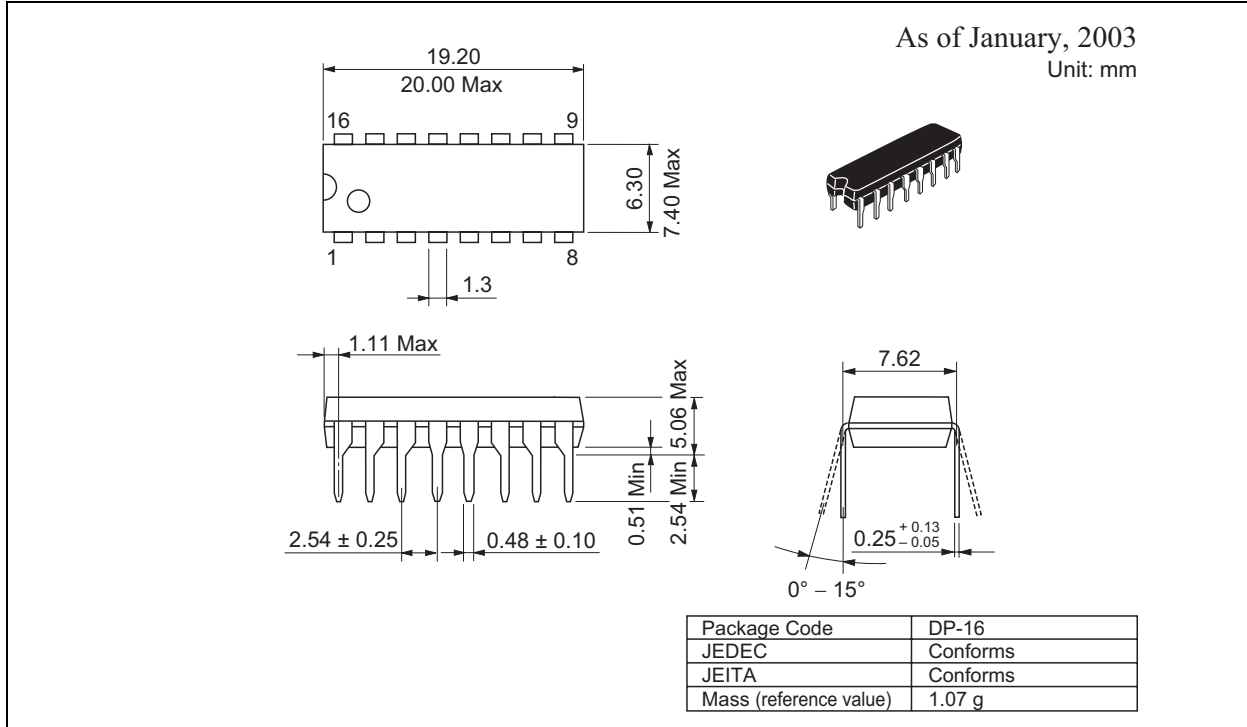


Application Circuit Example

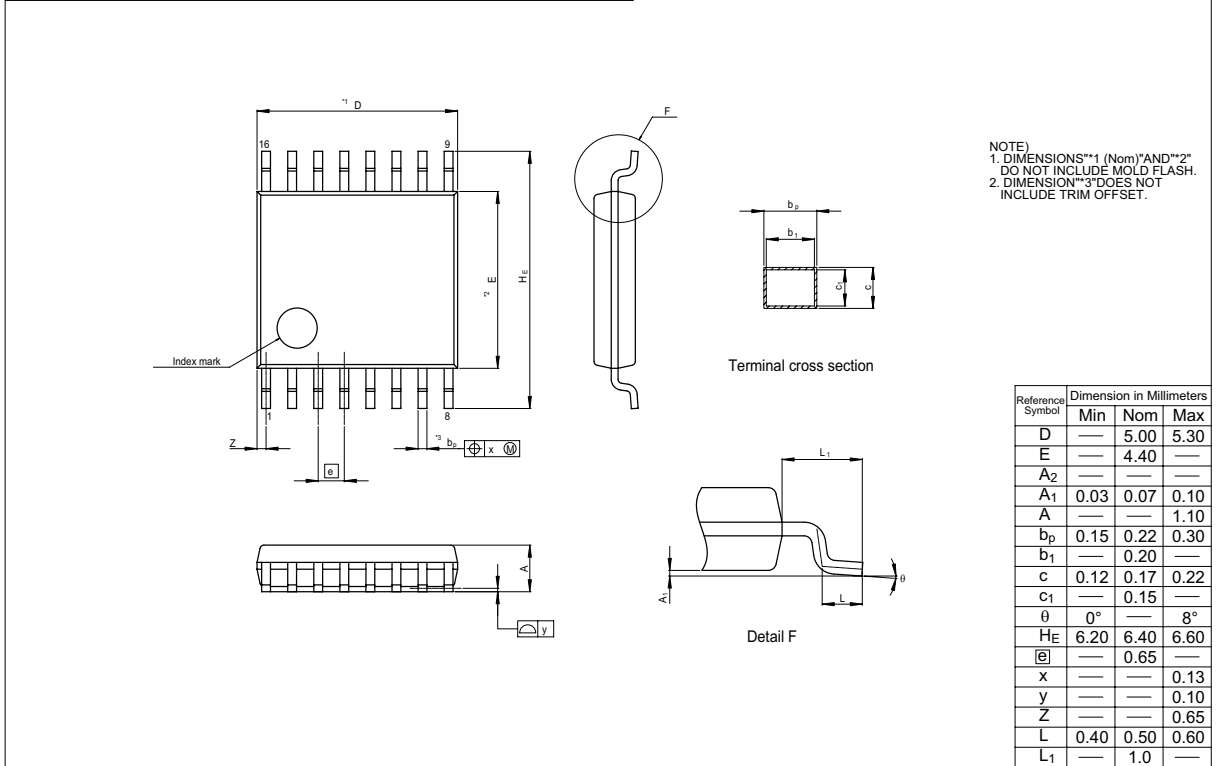
The following diagram shows a sample application circuit for a push-pull converter with a 48 V input voltage, 3.3 V output voltage, and 10 A output current.



Package Dimensions



JEITA Package Code	RENEASAS Code	Previous Code	MASS[Typ.]
P-TSSOP16-4.4x5-0.65	PTSP0016JB-B	TTP-16DA	0.05g



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