
HA16158P/FP

PFC & PWM Control IC

RENESAS

ADE-204-072 (Z)

Rev.0
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Description

The HA16158 is a power supply controller IC combining an AC-DC converter switching controller for power factor correction and an off-line power supply switching controller. The PFC (power factor correction) section employs average current mode PWM and the off-line power supply control section employs peak current mode PWM.

The HA16158 allows the operating frequency to be varied with a single timing resistance, enabling it to be used for a variety of applications.

The PFC operation can be turned on and off by an external control signal. Use of this on/off function makes it possible to disable PFC operation at a low line voltage, or to perform remote control operation from the transformer secondary side.

The PWM controller includes a power-saving function that reduces the operating frequency to a maximum of 1/64 in the standby state, greatly decreasing switching loss.

The PFC section and PWM section are each provided with a soft start control pin, enabling a soft start time to be set easily.

Features

<Maximum Ratings>

- Supply voltage V_{cc} : 24 V
- Operating junction temperature T_{jopr} : -40°C to $+125^{\circ}\text{C}$

<Electrical Characteristics>

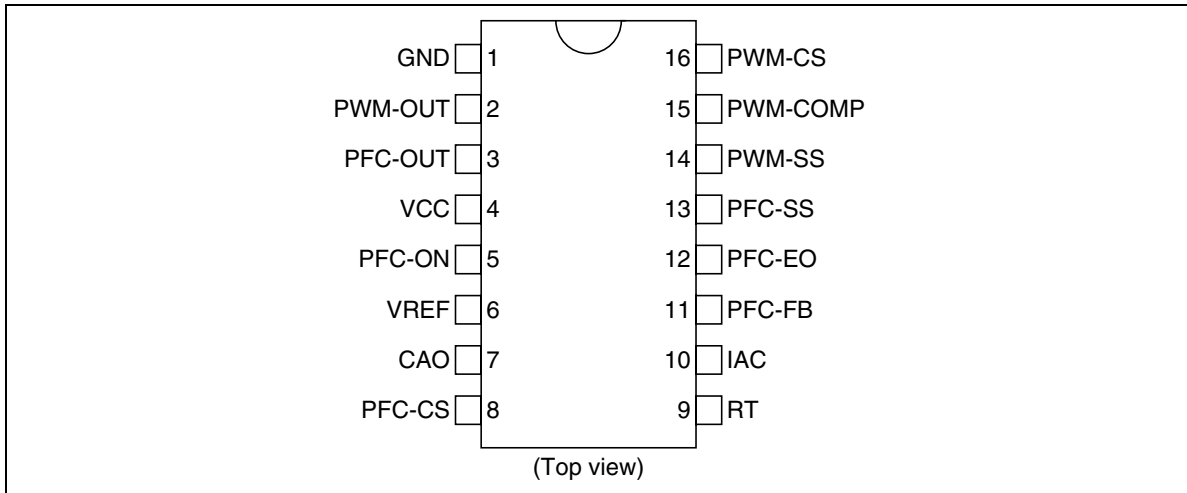
- VREF output voltage V_{REF} : $5.0\text{ V} \pm 2\%$
- UVLO start threshold V_H : $16.0\text{ V} \pm 1.0\text{ V}$
- UVLO shutdown threshold V_L : $10.0\text{ V} \pm 0.6\text{ V}$
- PFC output maximum duty cycle $D_{max-pfc}$: 95% typ.
- PWM output maximum duty cycle $D_{max-pwm}$: 45% typ.

<Functions>

- Synchronized PFC and PWM timing
- PFC function on/off control
- PWM power-saving function (frequency reduced to maximum of 1/64)
- PWM overvoltage latch protection circuit
- Soft start control circuits for both PFC and PWM
- Package lineup: SOP-16/DILP-16

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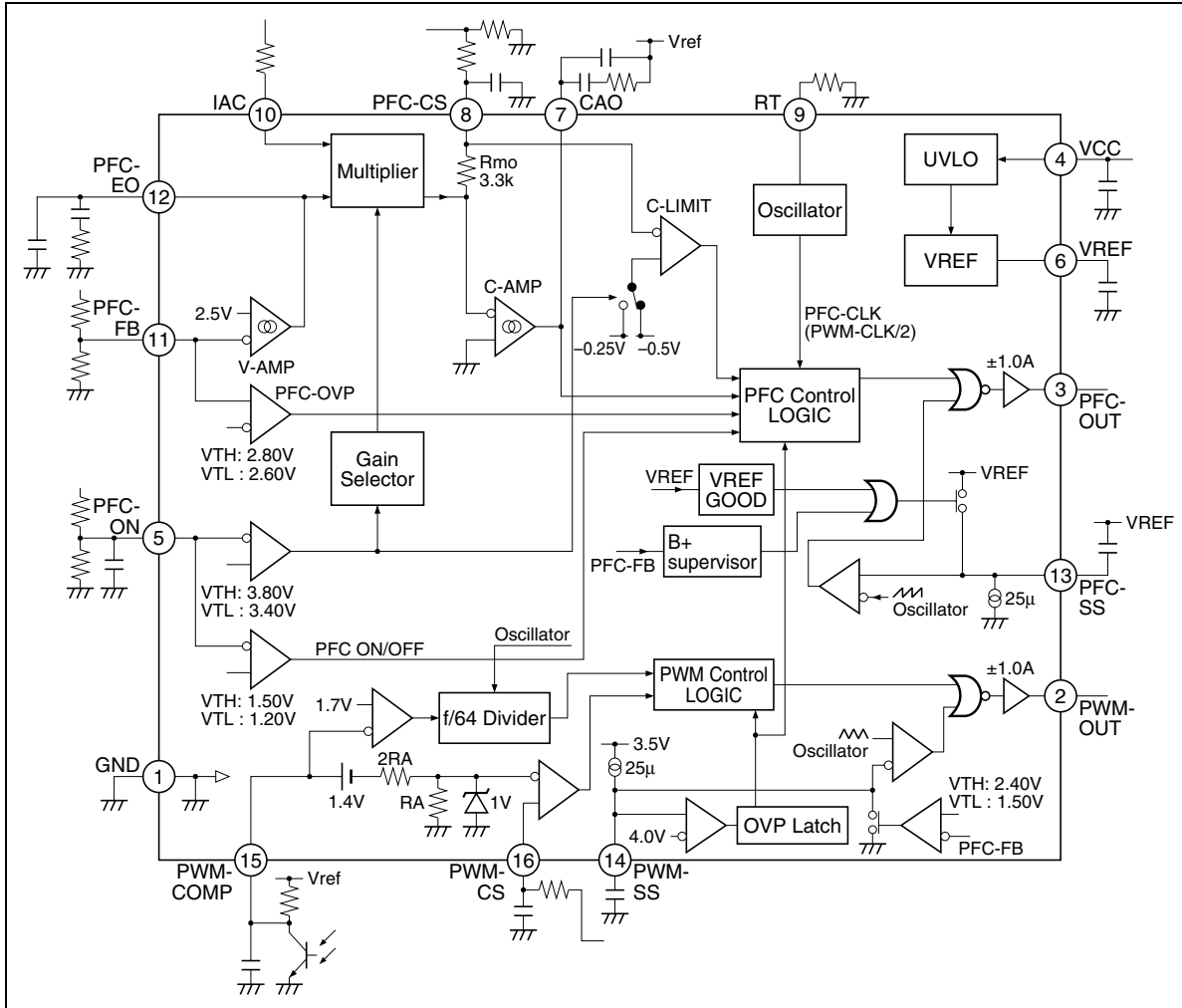
Pin Arrangement



Pin Functions

Pin No.	Pin Name	Pin Function
1	GND	Ground
2	PWM-OUT	Power MOS FET driver output (PWM control)
3	PFC-OUT	Power MOS FET driver output (PFC control)
4	VCC	Supply voltage
5	PFC-ON	PFC function on/off signal input
6	VREF	Reference voltage
7	CAO	Average current control error amplifier output
8	PFC-CS	PFC control current sense signal input
9	RT	Operating frequency setting timing resistance connection
10	IAC	Multiplier reference current input
11	PFC-FB	PFC control error amplifier input
12	PFC-EO	PFC control error amplifier output
13	PFC-SS	PFC control soft start time setting capacitance connection
14	PWM-SS	PWM control soft start time setting capacitance connection
15	PWM-COMP	PWM control voltage feedback
16	PWM-CS	PWM control current sense signal input

Block Diagram



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Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit	Note
Power supply voltage	Vcc	24	V	
PFC-OUT output current (peak)	Ipk-out1	±1.0	A	3
PWM-OUT output current (peak)	Ipk-out2	±1.0	A	3
PFC-OUT output current (DC)	I _{dc} -out1	±0.1	A	
PWM-OUT output current (DC)	I _{dc} -out2	±0.1	A	
Pin voltage	Vi-group1	-0.3 to Vcc	V	4
	Vi-group2	-0.3 to Vref	V	5
CAO pin voltage	Vcao	-0.3 to Veoh-ca	V	
PFC-EO pin voltage	Vpfc-eo	-0.3 to Veoh-pfc	V	
PFC-ON pin voltage	Vpfc-on	-0.3 to 7	V	
RT pin current	I _{rt}	50	μA	
IAC pin current	I _{iac}	1	mA	
PFC-CS pin voltage	Vi-cs	-1.5 to 0.3	V	
VREF pin current	I _{o-ref}	-20	mA	
VREF pin voltage	Vref	-0.3 to Vref	V	
Operating junction temperature	T _{j-opr}	-40 to +125	°C	6
Storage temperature	T _{stg}	-55 to +150	°C	

- Notes:
1. Rated voltages are with reference to the GND (SGND, PGND) pin.
 2. For rated currents, inflow to the IC is indicated by (+), and outflow by (-).
 3. Shows the transient current when driving a capacitive load.
 4. Group1 is the rated voltage for the following pins:
PFC-OUT, PWM-OUT
 5. Group2 is the rated voltage for the following pins:
PFC-FB, PWM-CS, PWM-COMP, IAC, PFC-SS, PWM-SS, RT
 6. HA16158P (DILP): $\theta_{ja} = 120^{\circ}\text{C/W}$
HA16158FP (SOP): $\theta_{ja} = 120^{\circ}\text{C/W}$
This value is based on actual measurements on a 10% wiring density glass epoxy circuit board (40 mm × 40 mm × 1.6 mm).

Electrical Characteristics

(Ta = 25°C, Vcc = 12 V, RT = 200 kΩ)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Supply	Start threshold	VH	15.0	16.0	17.0	V	
	Shutdown threshold	VL	9.4	10.0	10.6	V	
	UVLO hysteresis	dV _{UVL}	5.2	6.0	6.8	V	
	Start-up current	I _s	160	220	280	μA	V _{cc} = 14.8V
	I _s temperature stability	dI _s /dT _a	—	-0.3	—	%/°C	*1
	Operating current	I _{cc}	5.5	7.0	8.5	mA	I _{AC} = 0A, CL = 0F
	Shunt zenner voltage	V _z	25.5	27.5	29.5	V	I _{cc} = 14mA
	V _z temperature stability	dV _z /dT _a	—	-4	—	mV/°C	I _{cc} = 14mA *1
	Latch current	I _{LATCH}	180	250	320	μA	V _{cc} = 9V
VREF	Output voltage	V _{ref}	4.9	5.0	5.1	V	I _{source} = 1mA
	Line regulation	V _{ref-line}	—	5	20	mV	I _{source} = 1mA, V _{cc} = 12V to 23V
	Load regulation	V _{ref-load}	—	5	20	mV	I _{source} = 1mA to 20mA
	Temperature stability	dV _{ref}	—	80	—	ppm/°C	T _a = -40 to 125°C *1
Oscillator	Initial accuracy	f _{pwm}	117	130	143	kHz	Measured pin: PWM-OUT
		f _{pfc}	58.5	65	71.5	kHz	Measured pin: PFC-OUT
	f _{pwm} temperature stability	df _{pwm} /dT _a	—	±0.1	—	%/°C	T _a = -40 to 125°C *1
	f _{pwm} voltage stability	f _{pwm(line)}	-1.5	+0.5	+1.5	%	V _{CC} = 12V to 18V
	Ramp peak voltage	V _{ramp-H}	—	3.6	4.0	V	PFC *1
	Ramp valley voltage	V _{ramp-L}	—	0.65	—	V	PFC *1
	CT peak voltage	V _{ct-H}	—	3.2	—	V	PWM *1
	CT valley voltage	V _{ct-L}	1.50	1.60	—	V	PWM *1
RT voltage	V _{rt}	0.85	1.00	1.15	V	Measured pin: RT	
Supervisor	PFC on voltage	V _{on-pfc}	1.4	1.5	1.6	V	
	PFC off voltage	V _{off-pfc}	1.1	1.2	1.3	V	
	PFC on-off hysteresis	dV _{on-off}	0.2	0.3	0.4	V	
	Input current	I _{pfc-on}	—	0.1	1.0	μA	PFC-ON = 2V
	PFC OVP set voltage	V _{ovps-pfc}	2.65	2.80	2.95	V	Input pin: PFC-FB
	PFC OVP reset voltage	V _{ovpr-pfc}	2.45	2.60	2.75	V	Input pin: PFC-FB
	PFC OVP hysteresis	dV _{ovp}	0.10	0.20	0.30	V	
	B+ good voltage	V _{b-good}	2.25	2.40	2.55	V	Measured pin: PFC-FB
	B+ fail voltage	V _{b-fail}	1.4	1.5	1.6	V	Measured pin: PFC-FB
OVP latch	Latch threshold voltage	V _{latch}	3.76	4.00	4.24	V	Input pin: PWM-SS
	Latch reset voltage	V _{cc-res}	6.1	7.1	8.1	V	
Power saving for PWM	Power saving on voltage	V _{on-save}	1.53	1.70	1.87	V	Measured pin: PWM-COMP
	Minimum frequency at light load	f _{pwm-min}	—	2	—	kHz	PWM-COMP = 1.5V Measured pin: PWM-OUT *1

Note: 1. Reference values for design.

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Electrical Characteristics (cont.)

(Ta = 25°C, Vcc = 12 V, RT = 200 kΩ)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Soft start for PWM	Soft start time	tss-pwm	—	4.2	—	ms	PWM-SS = 0V to Vct-h *1
	Source current	lss-pwm	-20.0	-25.0	-30.0	μA	Measured pin: PWM-SS
	High voltage	Vh-ss	3.25	3.5	3.75	V	Measured pin: PWM-SS
Soft start for PFC	Soft start time	tss-pfc	—	5.7	—	ms	PFC-SS = Vref to Vramp-I *1
	Source current	lss-pfc	+20.0	+25.0	+30.0	μA	Measured pin: PFC-SS
PWM current sense	Delay to output	td-cs	—	210	300	ns	PWM-EO = 5V, PWM-CS = 0 to 2V
PFC current limit	Threshold voltage	VLM1	-0.45	-0.50	-0.55	V	PFC-ON = 2V
	Threshold voltage	VLM2	-0.22	-0.25	-0.28	V	PFC-ON = 4V
	Delay to output	td-LM	—	280	500	ns	PFC-CS = 0 to -1V
PFC-VAMP	Feedback voltage	Vfb-pfc	2.45	2.50	2.55	V	PFC-EO = 2.5V
	Input bias current	lfb-pfc	-0.3	0	0.3	μA	Measured pin: PFC-FB
	Open loop gain	Av-pfc	—	65	—	dB	*1
	High voltage	Veoh-pfc	5.0	5.7	6.4	V	PFC-FB = 2.3V, PFC-EO: Open
	Low voltage	Veol-pfc	—	0.1	0.3	V	PFC-FB = 2.7V, PFC-EO: Open
	Source current	lsrc-pfc	—	-90	—	μA	PFC-FB = 1.0V, PFC-EO: 2.5V *1
	Sink current	lsnk-pfc	—	90	—	μA	PFC-FB = 4.0V, PFC-EO: 2.5V *1
	Transconductance	Gm-pfcv	150	200	250	μA/V	PFC-FB = 2.5V, PFC-EO: 2.5V
PFC-OUT	Minimum duty cycle	Dmin-pfc	—	—	0	%	CAO = 4.0V
	Maximum duty cycle	Dmax-pfc	90	95	98	%	CAO = 0V
	Rise time	tr-pfc	—	30	100	ns	CL = 1000pF
	Fall time	tf-pfc	—	30	100	ns	CL = 1000pF
	Peak current	lpk-pfc	—	1.0	—	A	CL = 0.01μF *1
	Low voltage	Vol1-pfc	—	0.05	0.2	V	Iout = 20mA
		Vol2-pfc	—	0.5	2.0	V	Iout = 200mA
		Vol3-pfc	—	0.03	0.7	V	Iout = 10mA, VCC = 5V
	High voltage	Voh1-pfc	11.5	11.9	—	V	Iout = -20mA
Voh2-pfc		10.0	11.0	—	V	Iout = -200mA	
PWM-OUT	Minimum duty cycle	Dmin-pwm	—	—	0	%	PWM-COMP = 0V
	Maximum duty cycle	Dmax-pwm	42	45	49	%	PWM-COMP = Vref
	Rise time	tr-pwm	—	30	100	ns	CL = 1000pF
	Fall time	tf-pwm	—	30	100	ns	CL = 1000pF
	Peak current	lpk-pwm	—	1.0	—	A	CL = 0.01μF *1
	Low voltage	Vol1-pwm	—	0.05	0.2	V	Iout = 20mA
		Vol2-pwm	—	0.5	2.0	V	Iout = 200mA
		Vol3-pwm	—	0.03	0.7	V	Iout = 10mA, VCC = 5V
	High voltage	Voh1-pwm	11.5	11.9	—	V	Iout = -20mA
Voh2-pwm		10.0	11.0	—	V	Iout = -200mA	

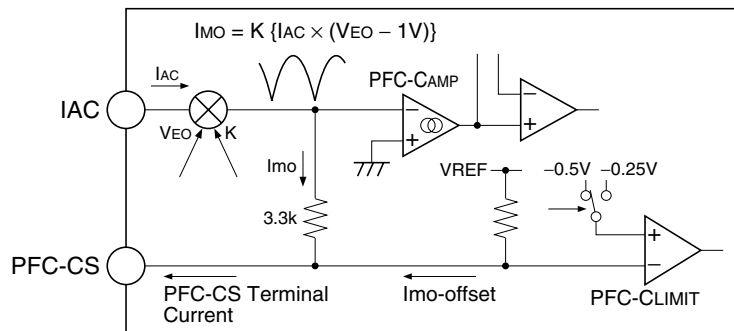
Note: 1. Reference values for design.

Electrical Characteristics (cont.)

(Ta = 25°C, Vcc = 12 V, RT = 200 kΩ)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
PFC-CAMP	Input offset voltage	Vio-ca	—	±7	—	mV	*1
	Open loop gain	Av-ca	—	65	—	dB	*1
	High voltage	Veoh-ca	5.0	5.7	6.4	V	
	Low voltage	Veol-ca	—	0.1	0.3	V	
	Source current	Isrc-ca	—	-90	—	μA	CAO = 2.5V *1
	Sink current	Isnk-ca	—	90	—	μA	CAO = 2.5V *1
	Transconductance	Gm-pfcc	150	200	250	μA/V	*1
IAC/Multiplier	IAC pin voltage	Viac	0.7	1.0	1.3	V	IAC = 100μA
	Terminal offset current	Imo-offset1	-67	-90	-113	μA	IAC = 0A, PFC-ON = 2V
		Imo-offset2	-60	-80	-100	μA	IAC = 0A, PFC-ON = 4V
	Output current (PFC-ON = 2.0V)	Imo1	—	-20	—	μA	PFC-EO = 2V, IAC = 100μA *1,2
		Imo2	—	-60	—	μA	PFC-EO = 4V, IAC = 100μA *1,2
	Output current (PFC-ON = 4.0V)	Imo3	—	-5	—	μA	PFC-EO = 2V, IAC = 100μA *1,2
Imo4		—	-15	—	μA	PFC-EO = 4V, IAC = 100μA *1,2	
PFC-CS resistance	Rmo	—	3.3	—	kΩ	*1	
Gain selector	Threshold voltage for K = 0.05	VK-H	3.60	3.80	4.00	V	Measured pin: PFC-ON
	Threshold voltage for K = 0.25	VK-L	3.20	3.40	3.60	V	Measured pin: PFC-ON
	VK hysteresis	dVK	0.30	0.40	0.50	V	*1

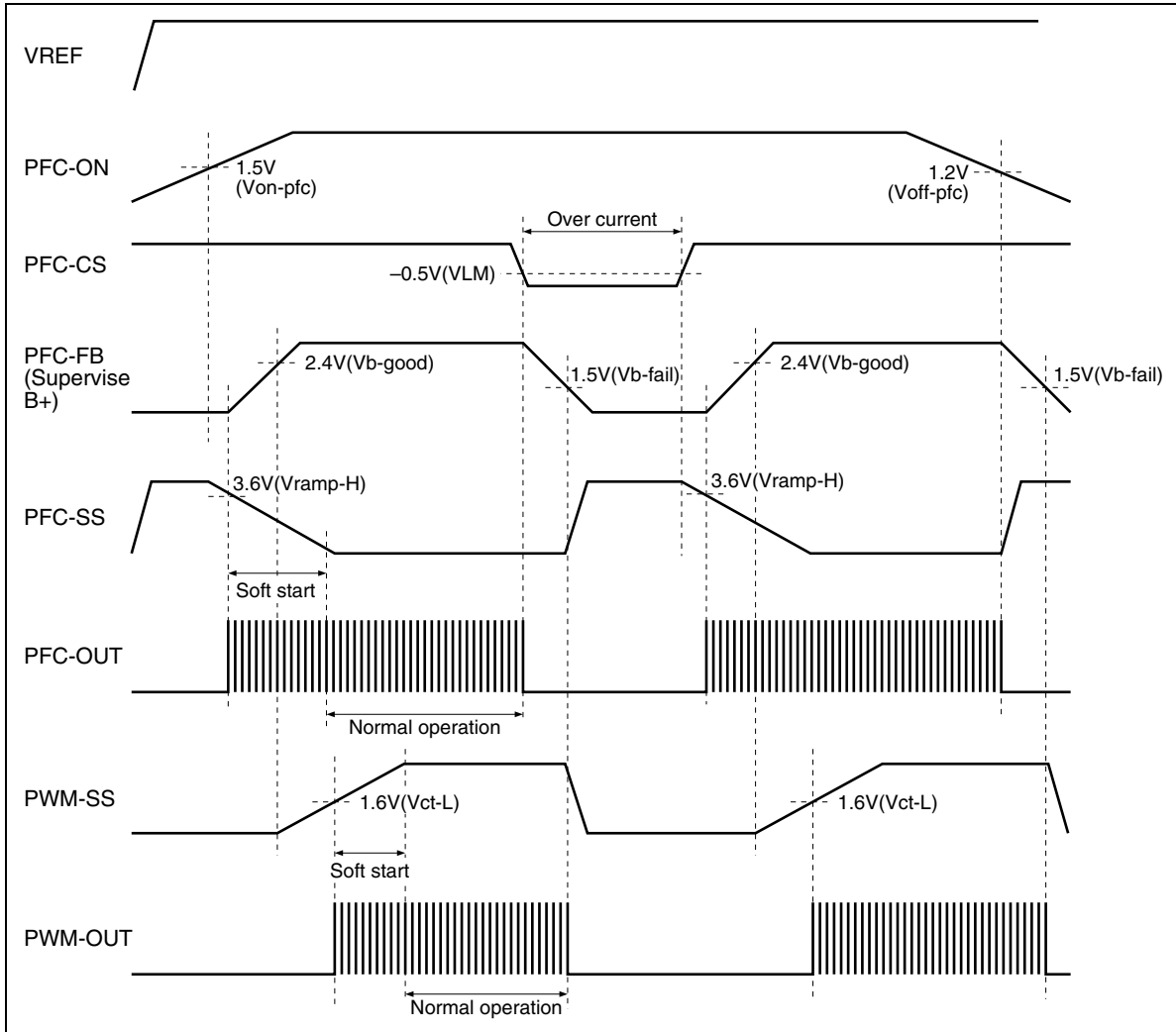
- Notes: 1. Reference values for design.
 2. Imo1 to Imo4 are defined as:
 $I_{mo} = (\text{PFC-CS pin current}) - (I_{mo\text{-offset}})$



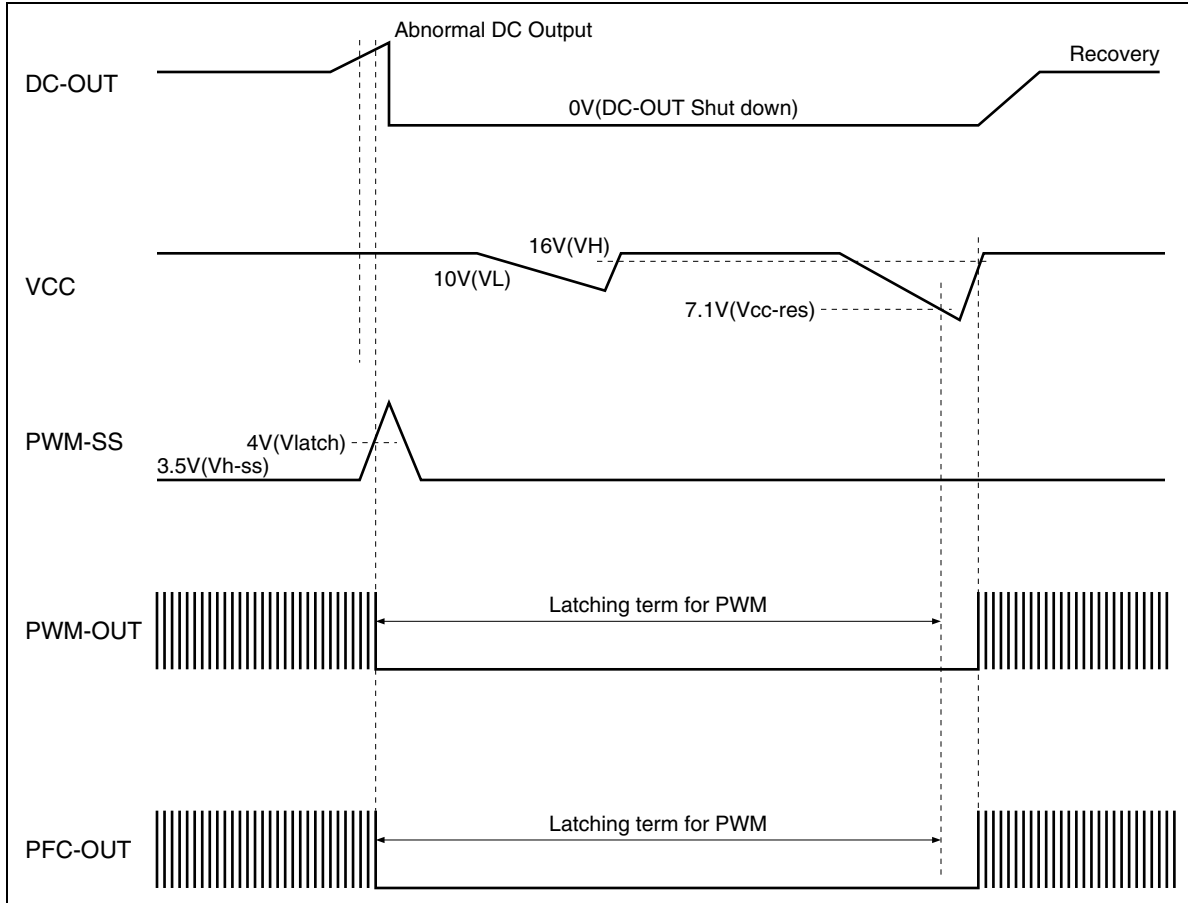
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Timing Diagram

1. Start-up Timing

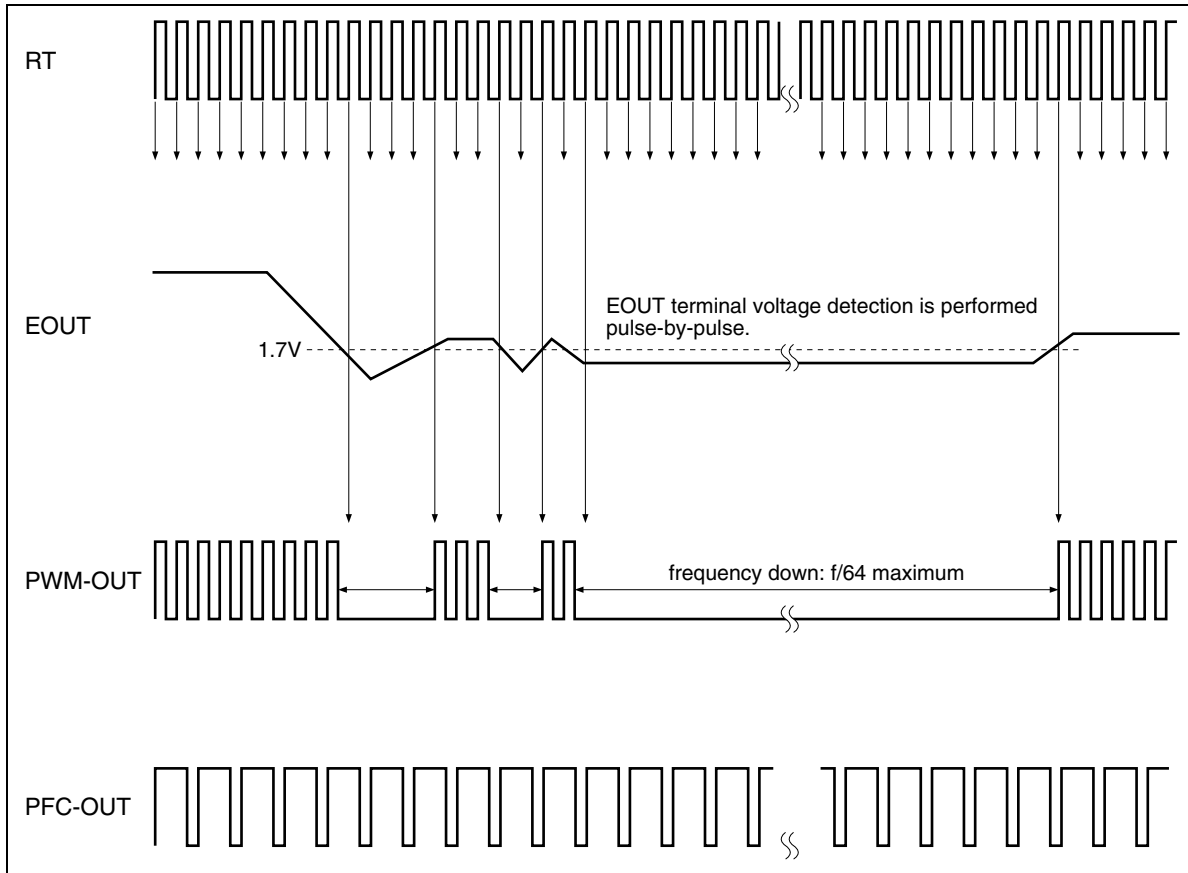


2. PWM OVP Latch



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3. PWM Power Saving



Functional Description

1. UVL Circuit

The UVL circuit monitors the Vcc voltage and halts operation of the IC in the event of a low voltage. The voltage for detecting Vcc has a hysteresis characteristic, with 16.0 V as the start threshold and 10.0 V as the shutdown threshold.

When the IC has been halted by the UVL circuit, control is performed to fix driver circuit output low and halt VREF output and the oscillator.

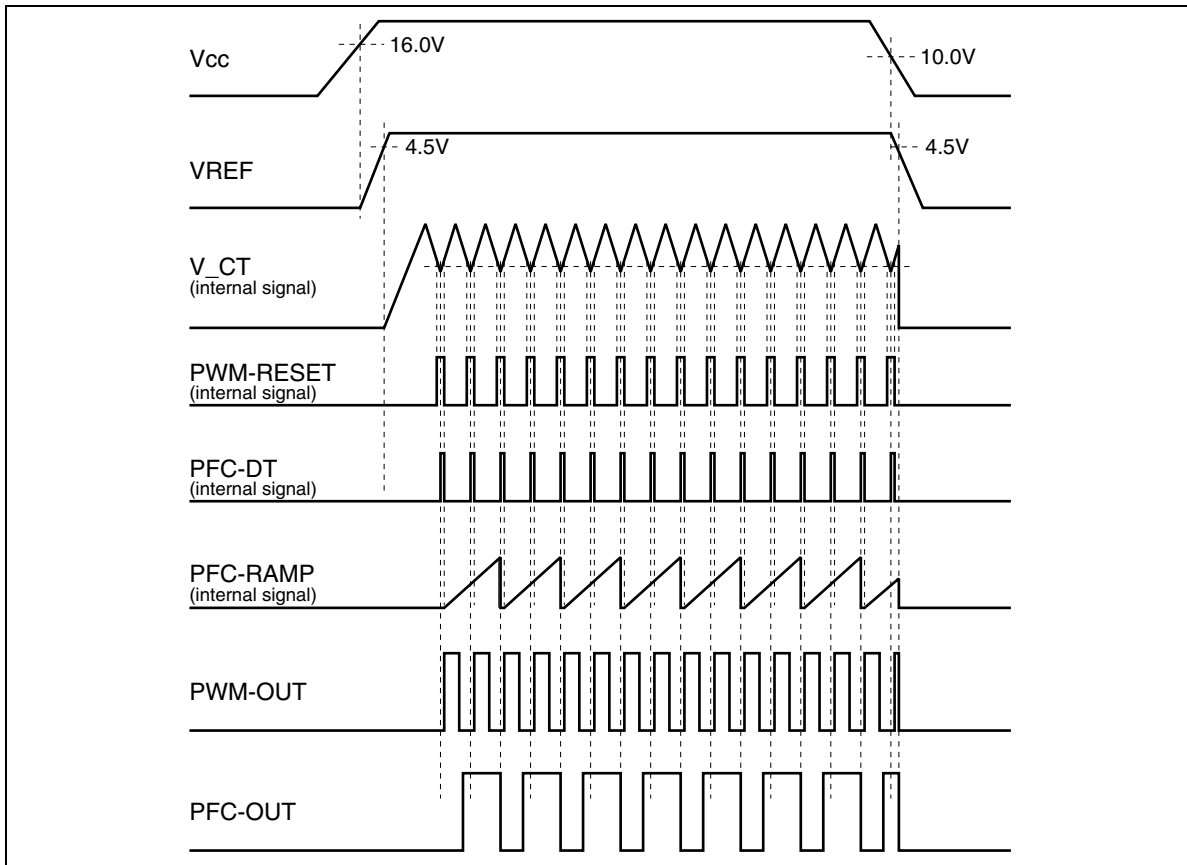


Figure 1

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2. Soft Start Circuit (for PWM Control)

This function gradually increases the pulse width of the PWM-OUT pin from a 0% duty cycle at start-up to prevent a sudden increase in the pulse width that may cause problems such as transient stress on external parts or overshoot of the secondary-side output voltage.

The soft start time can easily be set with a single external capacitance.

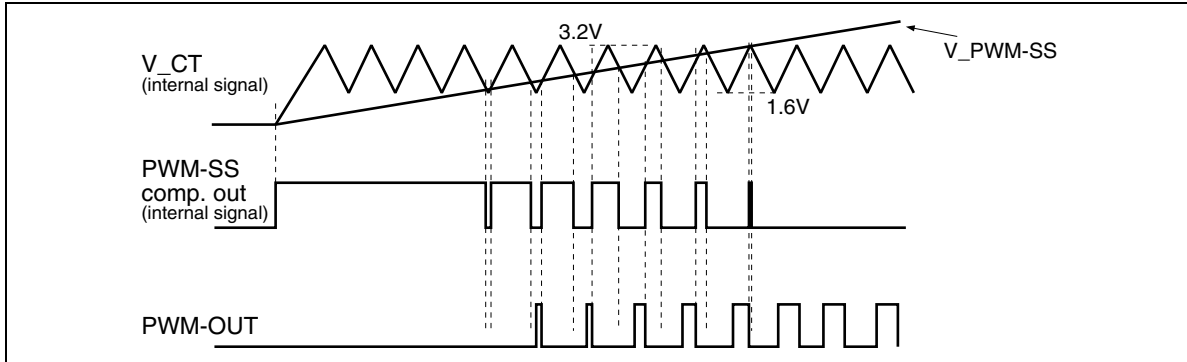


Figure 2

Soft start time t_{ss-pwm} is determined by PWM-SS pin connection capacitance C_{ss-pwm} and an internal constant, and can be estimated using the equation shown below.

Soft start time t_{ss-pwm} is the time until the PWM-SS pin voltage reaches upper-end voltage 3.2 V of the IC-internal CT voltage waveform after VREF starts up following UVLO release.

Soft start time t_{ss-pwm} when C_{ss-pwm} is 3.3 nF is given by the following equation.

$$t_{ss-pwm} = \frac{C_{ss-pwm} \times V_{ct-H}}{I_{ss-pwm}} = \frac{33 \text{ [nF]} \times 3.2 \text{ [V]}}{25 \text{ [\mu A]}} \\ \approx 4.2 \text{ [ms]}$$

* I_{ss-pwm} : PWM-SS pin source current, 25 μA typ.

3. Soft Start Circuit (for PFC Control)

This function gradually increases the pulse width of the PFC-OUT pin from a 0% duty cycle at start-up to prevent a sudden increase in the pulse width that may cause problems such as transient stress on external parts or overshoot of the PFC output voltage (B+ voltage).

The soft start time can easily be set with a single external capacitance.

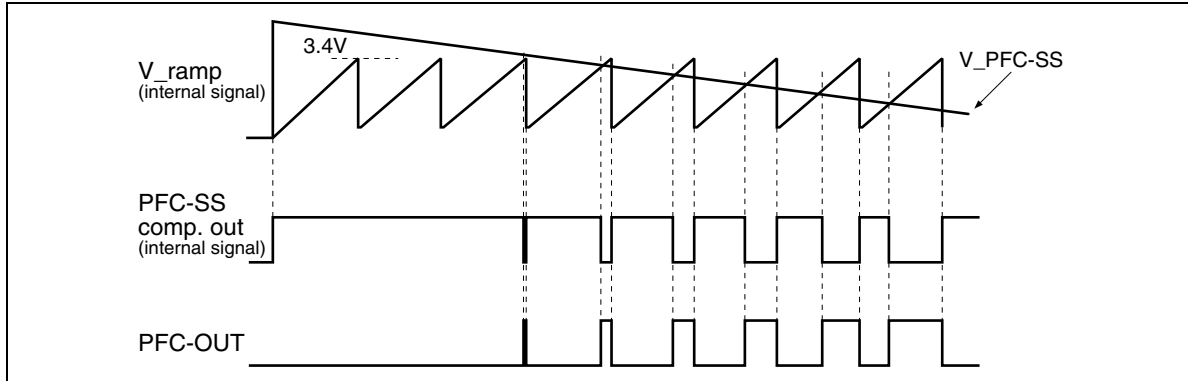


Figure 3

Soft start time t_{ss-pfc} is determined by PFC-SS pin connection capacitance C_{ss-pfc} and an internal constant, and can be estimated using the equation shown below.

Soft start time t_{ss-pfc} is the time until the PFC-SS pin voltage reaches lower-end voltage 0.65 V of the IC-internal RAMP voltage waveform after VREF starts up following UVLO release.

Soft start time t_{ss-pfc} when C_{ss-pfc} is 3.3 nF is given by the following equation.

$$t_{ss-pfc} = \frac{C_{ss-pfc} \times (V_{REF} - V_{ramp-L})}{I_{ss-pwm}} = \frac{33 \text{ [nF]} \times (5 - 0.65)}{25 \text{ [\mu A]}}$$

$$\approx 5.7 \text{ [ms]}$$

* I_{ss-pfc} : PFC-SS pin sink current, 25 μA typ.

In addition, when you do not use a soft start function, please ground this terminal.

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4. PFC On/Off Function

On/off control of the PFC function can be performed using the PFC-ON pin.

If an AC voltage that has undergone primary rectification and has been divided by an external resistance is input, it is possible to halt PFC operation in the event of a low input voltage. On/off control is also possible by using a logic signal.

This IC also incorporates a function that automatically detects a 100 V system or 200 V system AC voltage at the PFC-ON pin, and switches multiplier gain and the PFC-CS comparison voltage.

These functions simplify the design of a power supply compatible with worldwide input.

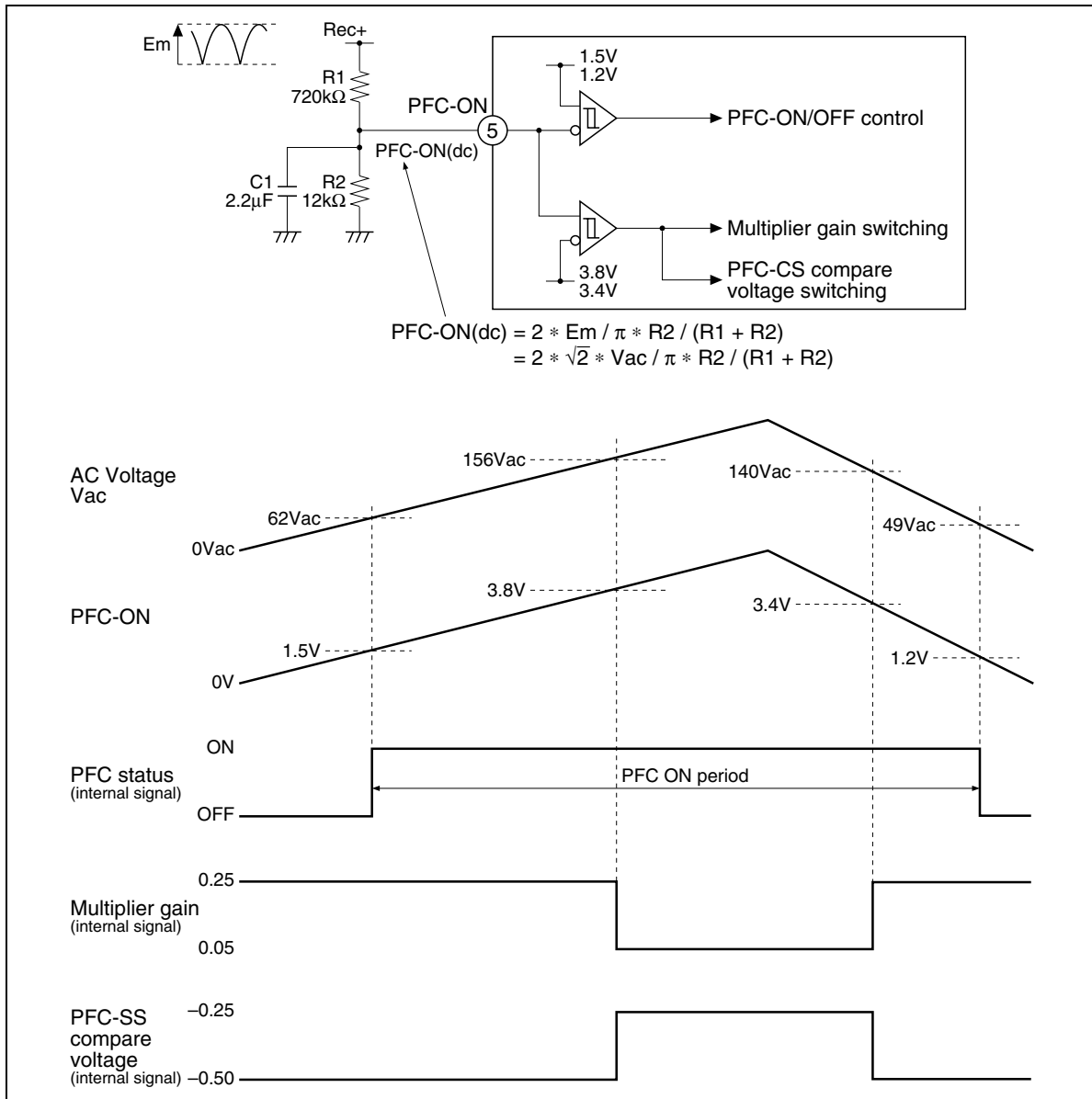


Figure 4

5. Power Saving in Standby State (for PWM Control)

When the output load is light, as in the standby state, the operating frequency of the PWM control section is automatically decreased in order to reduce switching loss.

Standby detection is performed by monitoring the PWM-COMP voltage, and the operating frequency is decreased to a maximum of 1/64 of the reference frequency determined by an external timing resistance.

As standby detection is performed on a reference frequency pulse-by-pulse basis, the frequency varies gently according to the output load.

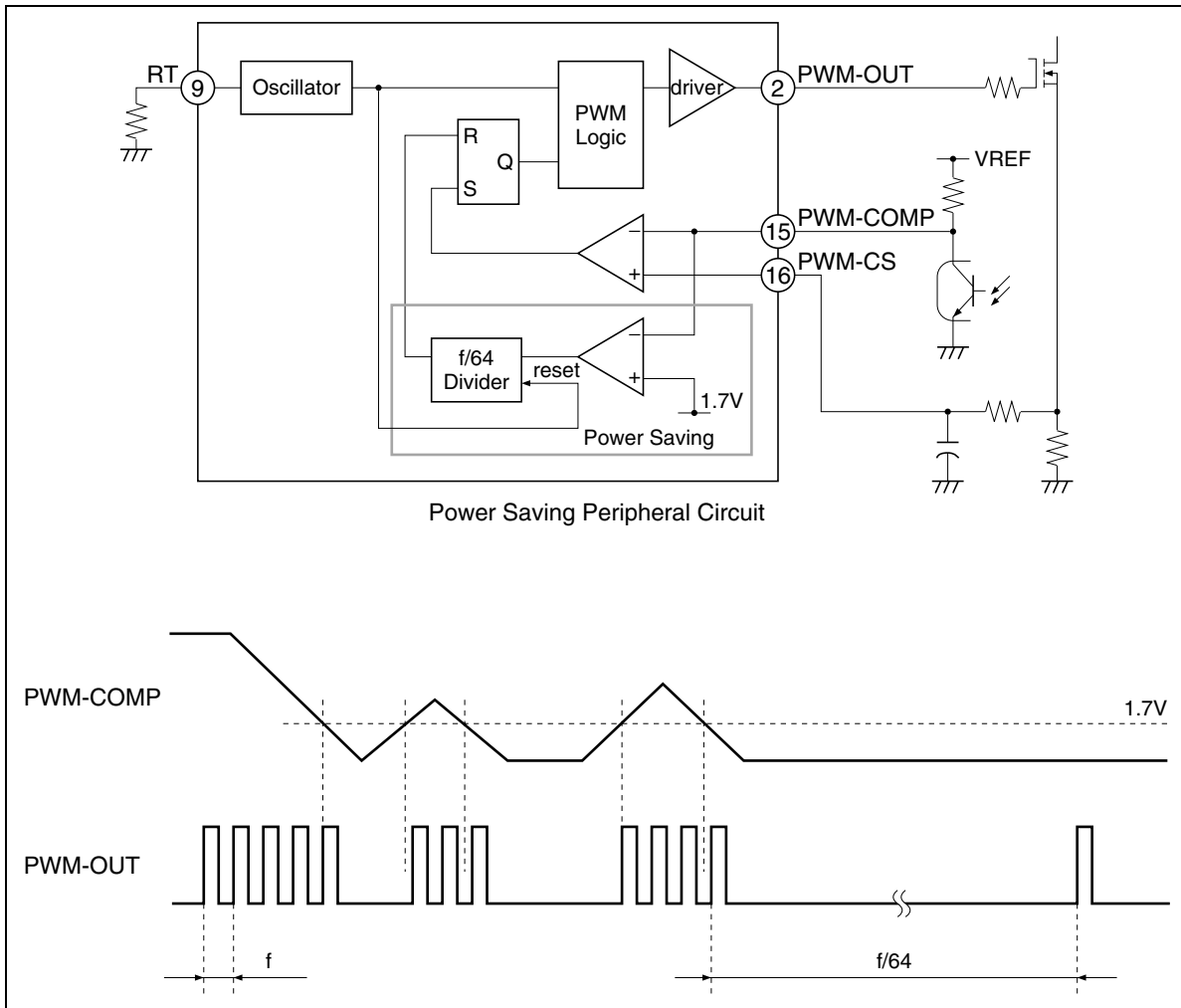


Figure 5

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6. Overvoltage Latch Protection (for PWM Control)

This is a protection function that halts PWM-OUT and PFC-OUT if the secondary-side PWM output voltage is abnormally high.

Overvoltage signal input is shared with the PWM-SS pin. When this pin is pulled up to 4.0 V or higher, the control circuit identifies an overvoltage error and halts PWM-OUT and PFC-OUT.

The power supply is turned off, and the latch is released when the VCC voltage falls to 7.1 V or below.

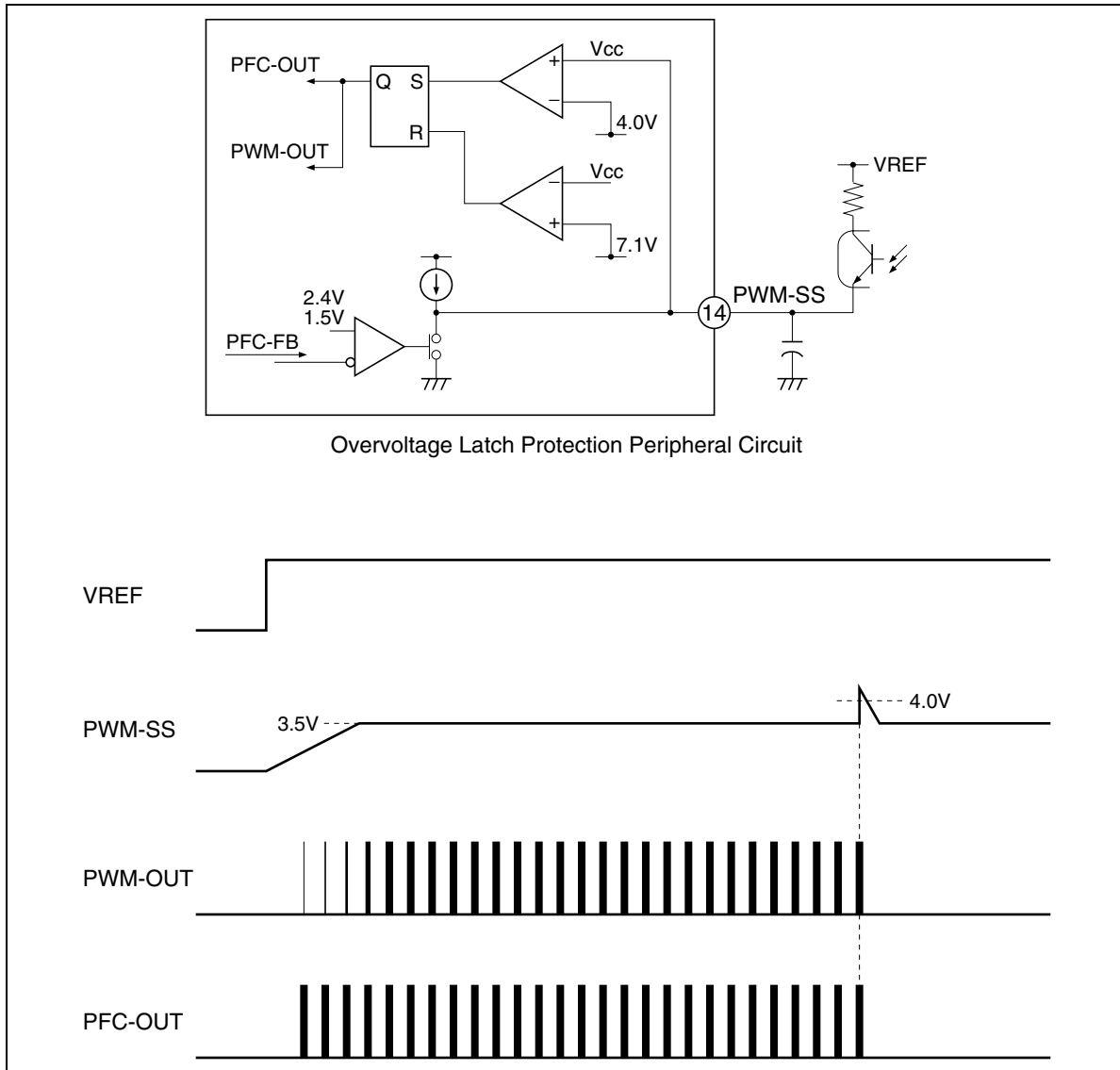


Figure 6

7. Operating Frequency

The operating frequency is adjusted by timing resistance RT.

Adjustment examples are shown in the graph below. The operating frequency fpwm in the PWM section is determined by the RT. The operating frequency fpfc in the PFC section is half the value of fpwm.

The operating frequency in the PWM section can be estimated using the approximate equation shown below.

RT = 200 kΩ:

$$fpwm \approx \frac{2.60 \times 10^{10}}{RT} = 130 \text{ [kHz]}$$

$$fpfc = \frac{fpwm}{2} = 65 \text{ [kHz]}$$

This is only an approximate equation, and the higher the frequency, the greater will be the degree of error of the approximate equation due to the effects of the delay time in the internal circuit, etc.

When the operating frequency is adjusted, it is essential to confirm operation using the actual system.

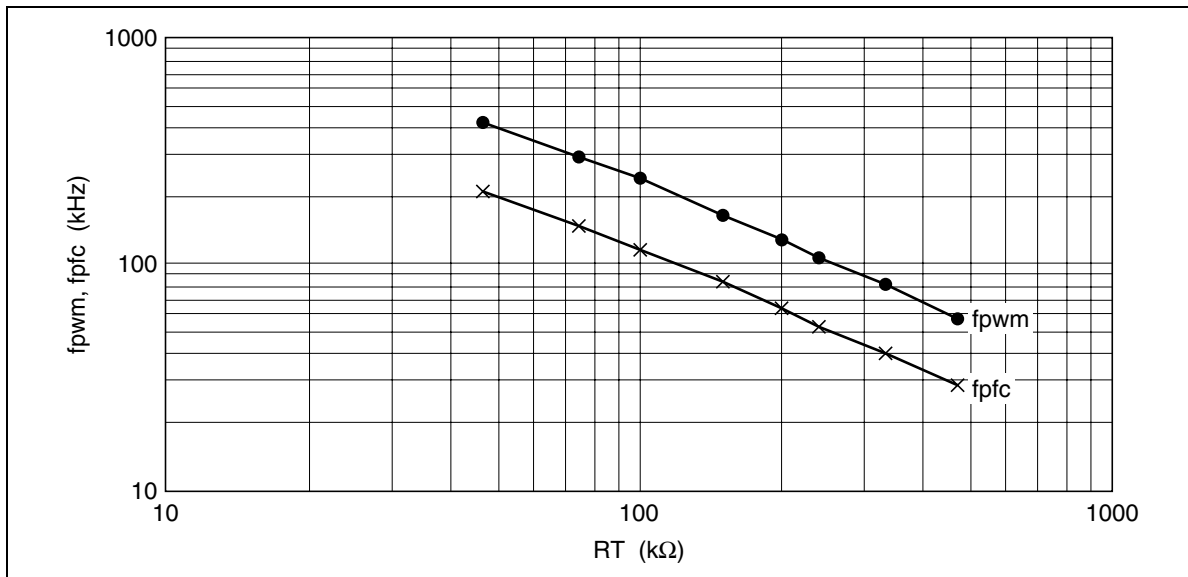
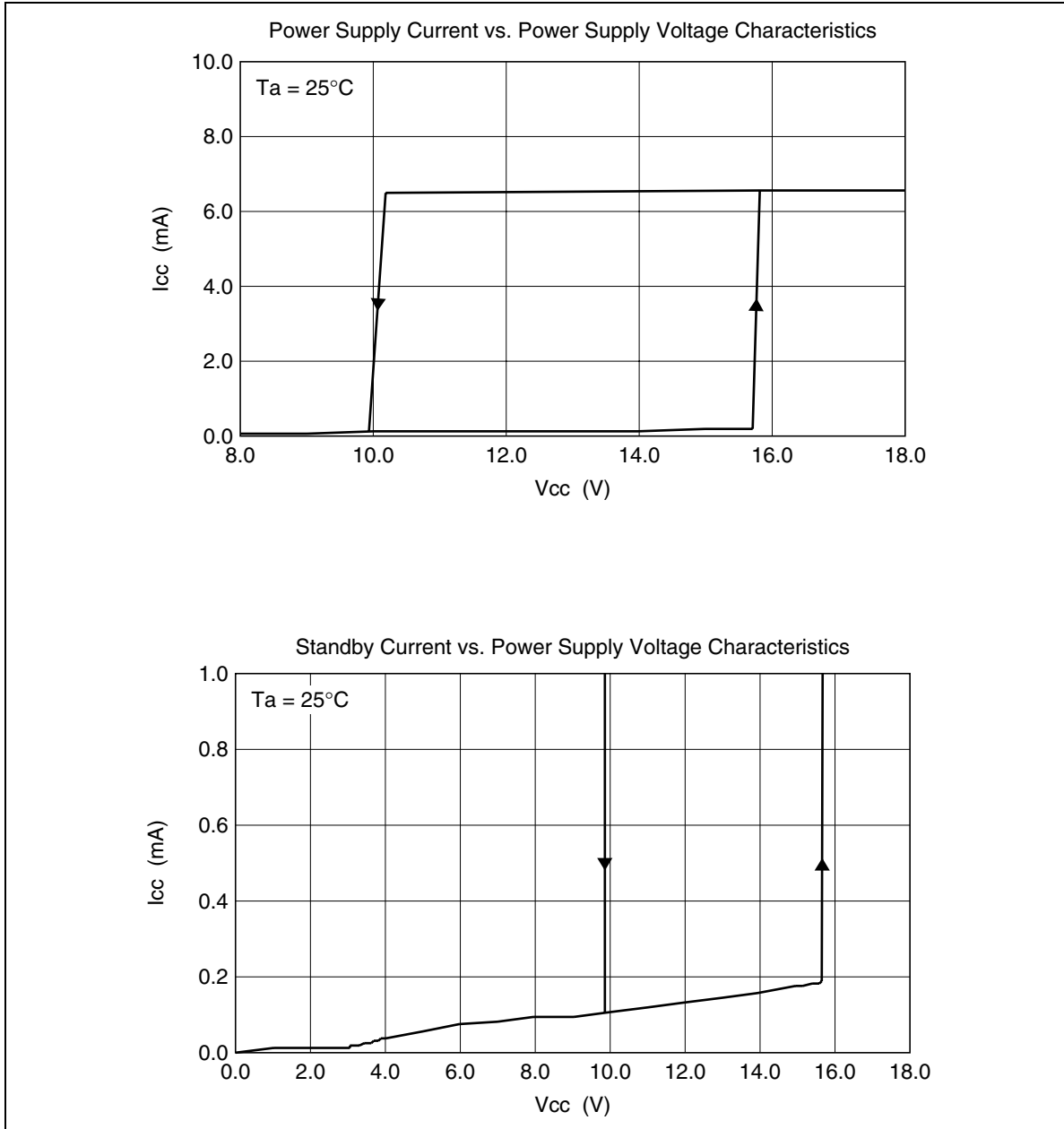
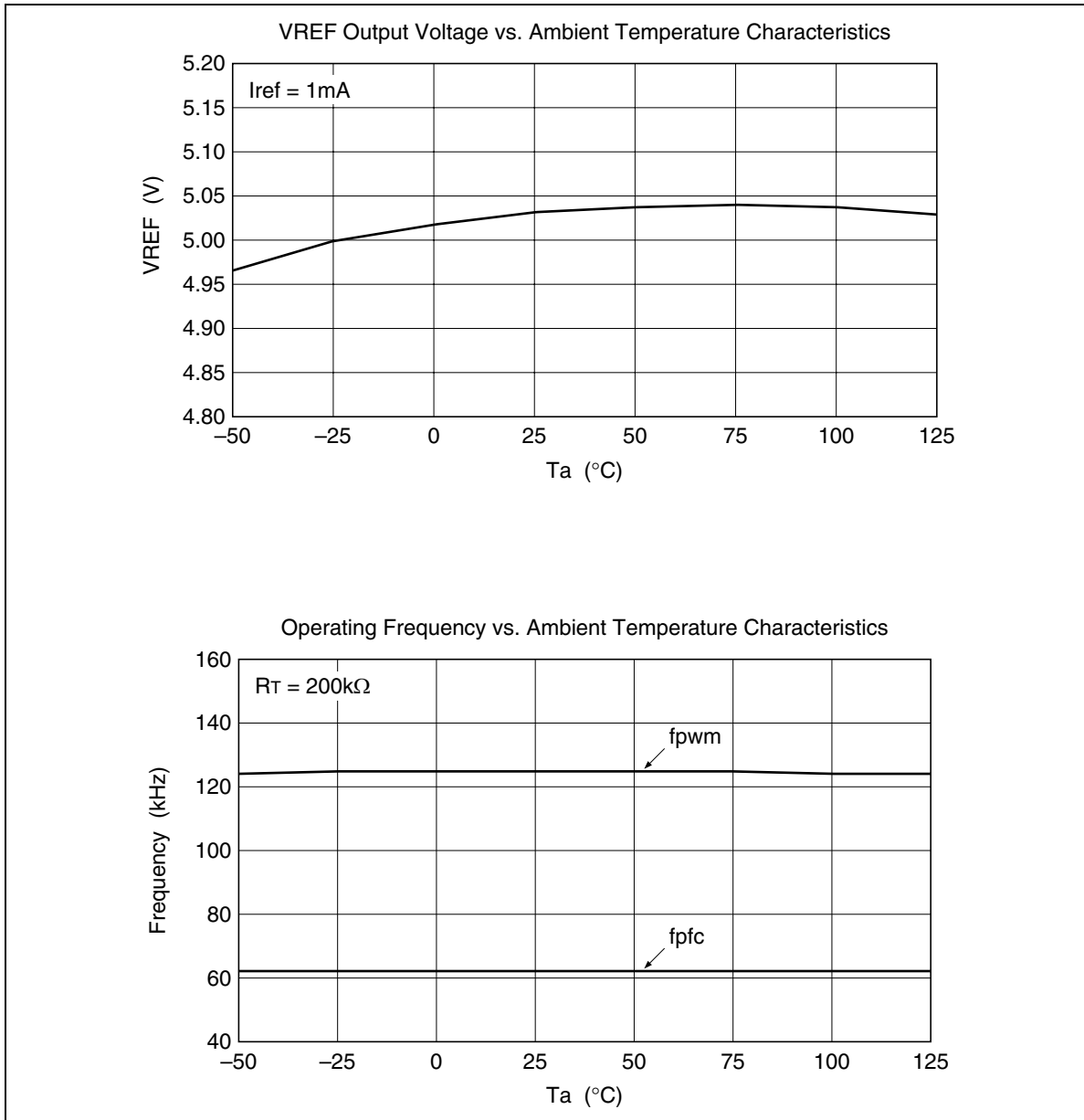


Figure 7

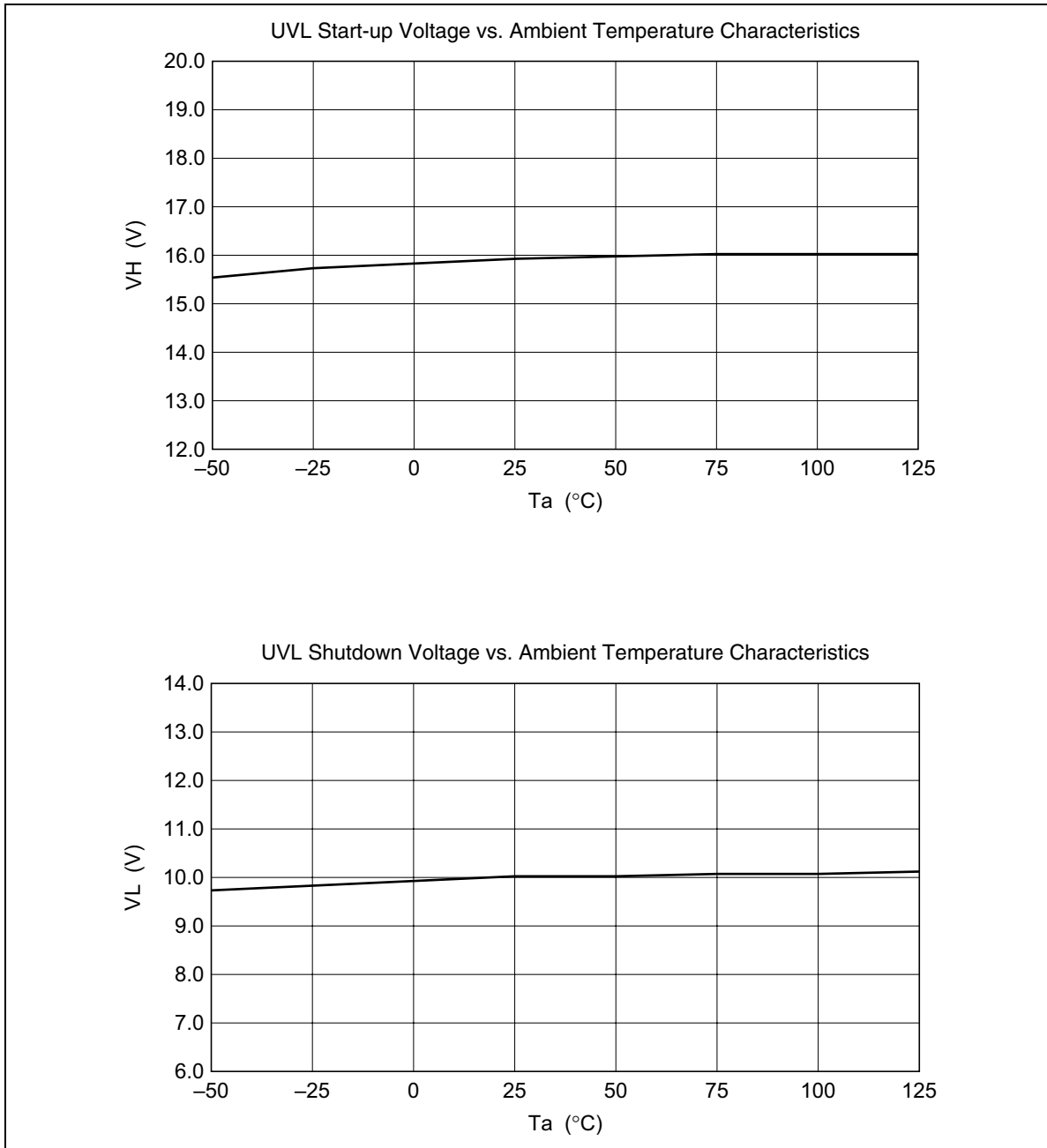
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Characteristic Curves

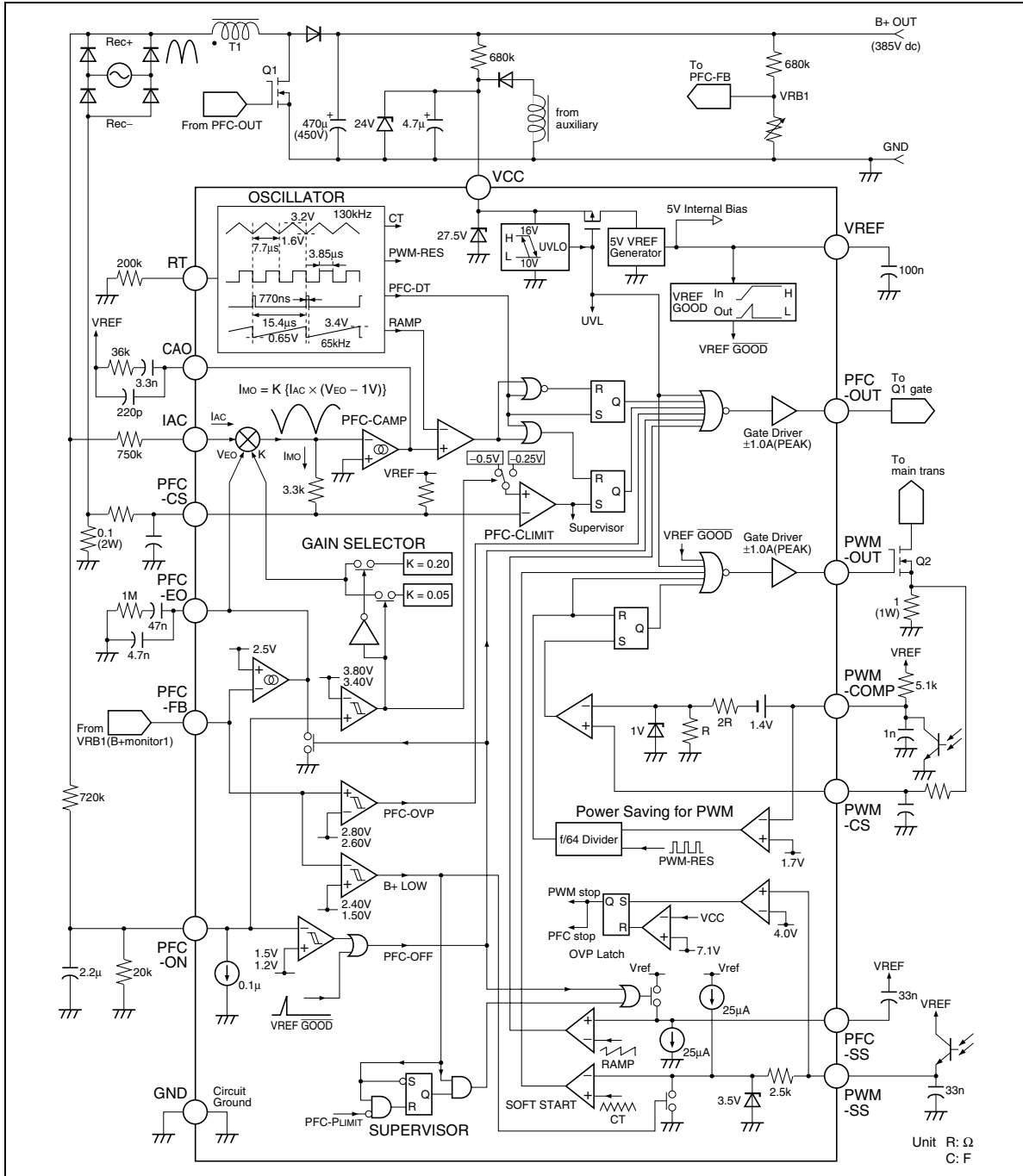




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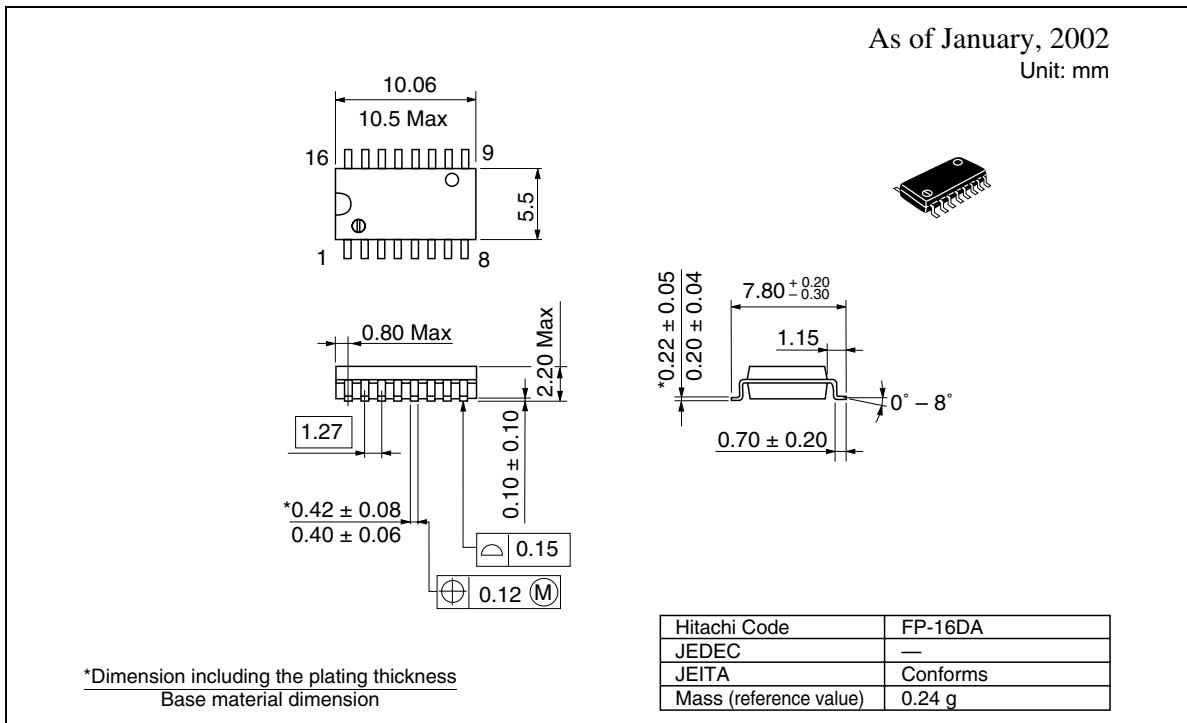
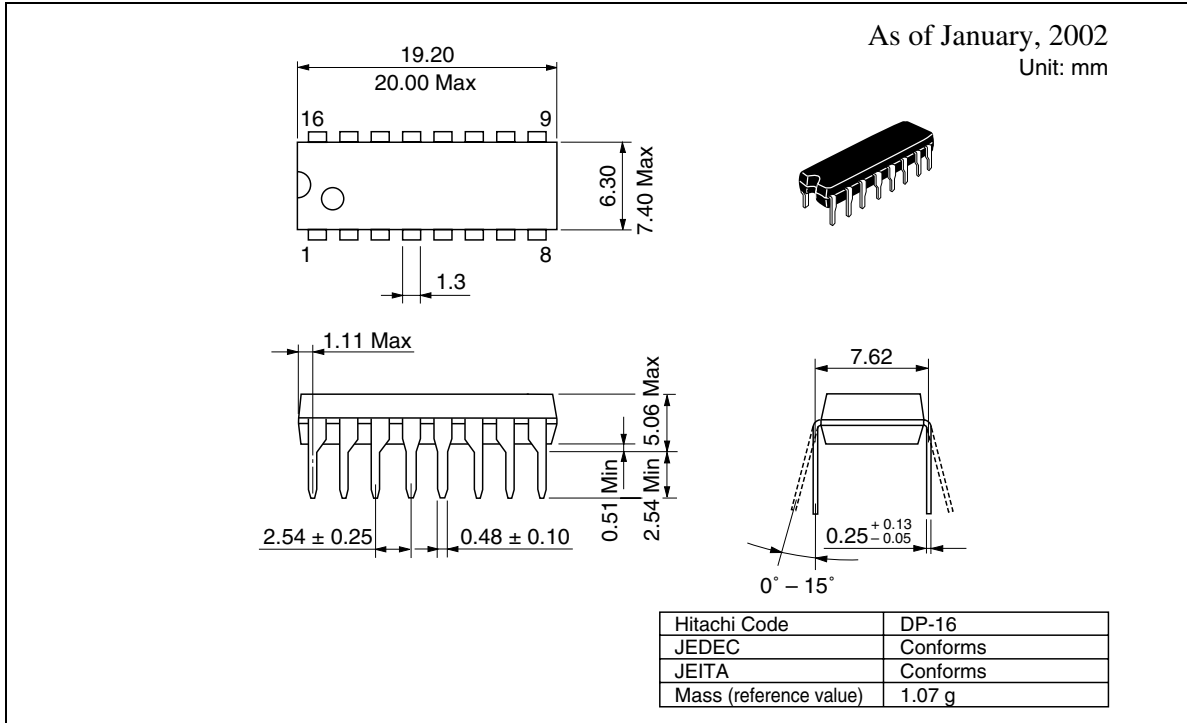


Application Circuit Example



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Package Dimensions



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