FUJITSU MICROELECTRONICS
DATA SHEET

DS04–27267–1E

ASSP for Power Management Applications of LCD Panel

4ch System Power Management IC for LCD Panel

MB39C313

■ DESCRIPTION

The MB39C313 is a 4ch system power management IC. It consists of 2-ch DC/DC Converter and 2-ch Charge pump. The DC/DC converter has excellent line regulation with the feed-forward method. Moreover, SW FET and phase compensator (Buck) is included, so that BOM can be reduced. It is most suitable for large size LCD panel power supply.

■ FEATURES

- Power supply voltage range: 8 V to 14 V
- For Buck Converter included SW FET (Vlogic): output 1.8 V to 3.3 V 1.5 A Max
- For Boost Converter included SW FET (Vs): output 18.1 V Max 1.5 A Max (at 12 V input and 15 V output)
- Negative Charge Pump with output voltage feedback (VGL): 50 mA Max
- Positive Charge Pump with output voltage feedback (VGH): 50 mA Max
- Error Amp threshold voltage: 1.213 V ± 1.5 % (Vlogic), 1.146 V ± 0.9 % (Vs),0 V ± 36 mV (VGL), 1.213 V ± 2.1 % (VGH)
- Built-in soft-start circuit independent of loads
- Excellent line regulation by the feed-forward method (Vlogic, Vs)
- Built-in phase compensator parts (Vlogic)
- Built-in sequence comparator for rising
- Built-in short circuit protection (Vlogic)
- Built-in over voltage protection (Vs)
- Built-in over current protection (Vlogic, Vs)
- Built-in over temperature protection
- Frequency setting by input pin: 500 kHz / 750 kHz
- Package: TSSOP-28 Exposed PAD

■ APPLICATIONS

TFT LCD panels for LCD TV sets and monitors.

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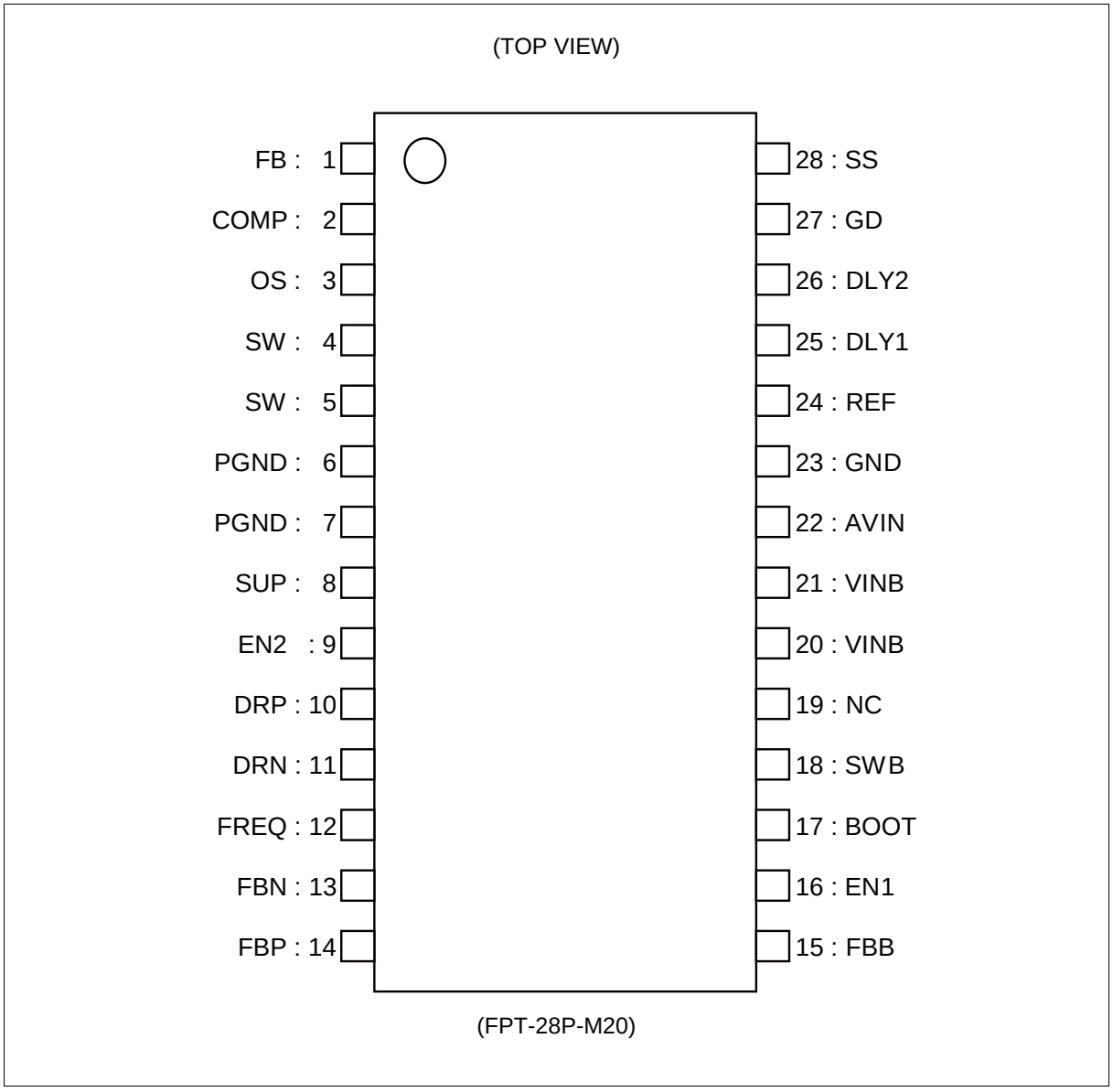
■ PIN ASSIGNMENT

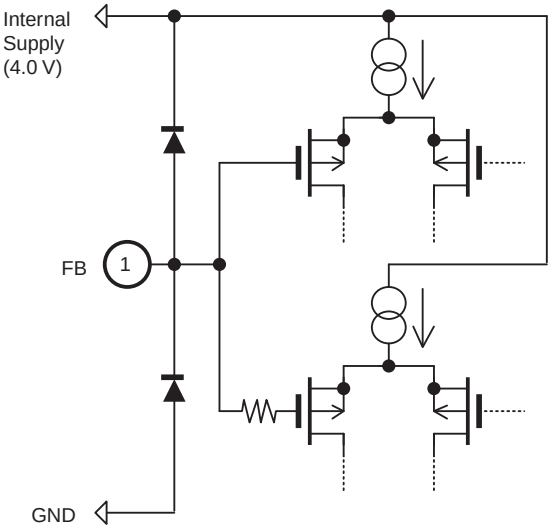


■ PIN DESCRIPTIONS

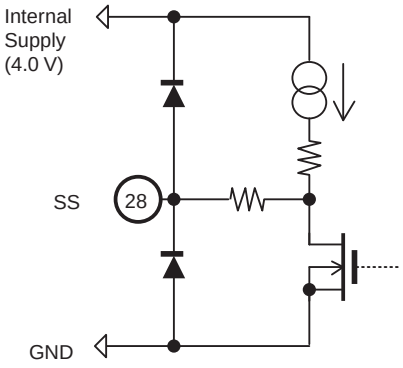
Block	Pin No.	Pin name	I/O	Descriptions
Vlogic (Buck Converter)	15	FBB	I	Vlogic Error Amp input pin
	17	BOOT	—	Boot strap capacitor connection pin
	18	SWB	O	Vlogic inductor connection pin
Vs (Boost Converter)	1	FB	I	Vs Error Amp input pin
	2	COMP	O	Vs Error Amp output pin
	28	SS	—	Vs Soft-start capacitor connection pin
	4	SW	I	Vs Inductor connection pin
	5	SW		
	3	OS	O	Vs Synchronous rectifier FET output pin
	27	GD	O	Vs External SW drive output pin (NMOS open drain output)
VGL (Negative Charge Pump)	11	DRN	O	VGL external flying capacitor connection pin
	13	FBN	I	VGL Error Amp input pin
VGH (Positive Charge Pump)	10	DRP	O	VGL external flying capacitor connection pin
	14	FBP	I	VGH Error Amp input pin
Control	16	EN1	I	Vlogic, VGL control pin
	9	EN2	I	Vs, VGH control pin
	12	FREQ	I	Frequency set pin “L”: 500 kHz,“H”: 750 kHz
	25	DLY1	—	VGL start time setting capacitor connection pin
	26	DLY2	—	Vs, VGH start time setting capacitor connection pin
Power	22	AVIN	—	Power supply pin
	20	VINB	—	Vlogic Power supply pin
	21	VINB		
	8	SUP	—	VGH Power supply pin
	24	REF	O	Reference voltage output pin
	6	PGND	—	Drive block ground pin
	7	PGND		
	23	GND	—	Ground pin
	19	NC	—	Non connection pin

■ I/O PIN EQUIVALENT CIRCUIT DIAGRAM

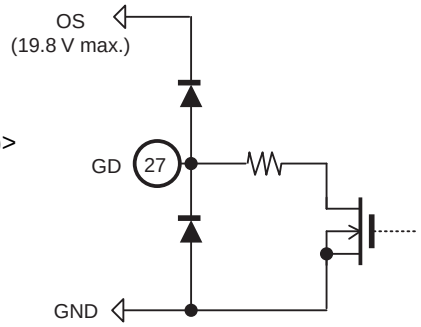
<Error Amplifier (Boost Converter)>



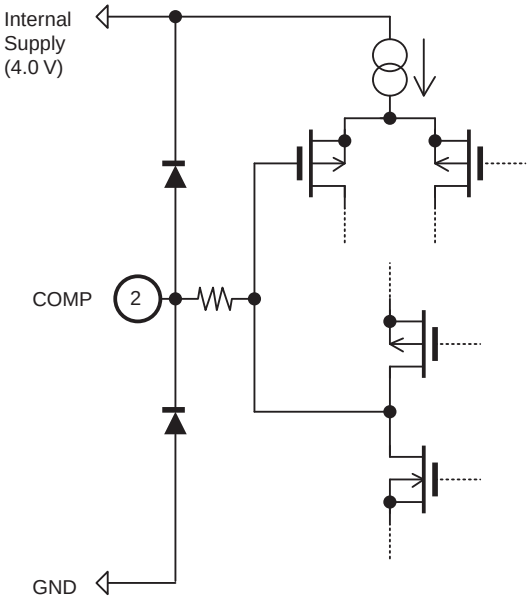
<Soft-start (Boost Converter)>



<Power-good (Boost Converter)>



<Error Amplifier Output for Compensation (Boost Converter)>



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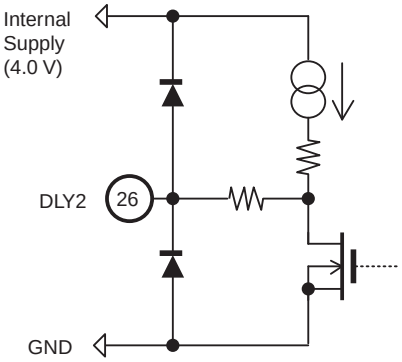

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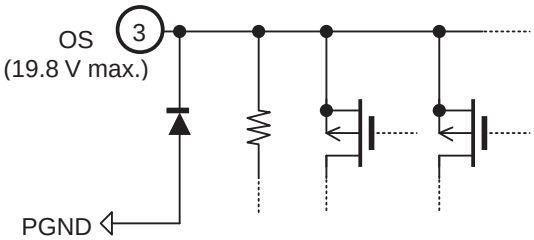

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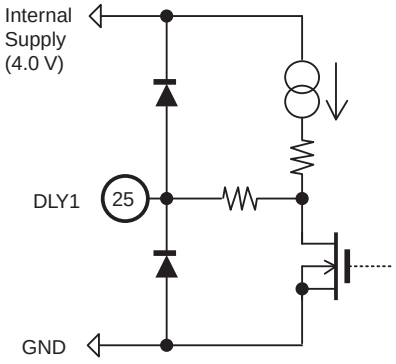

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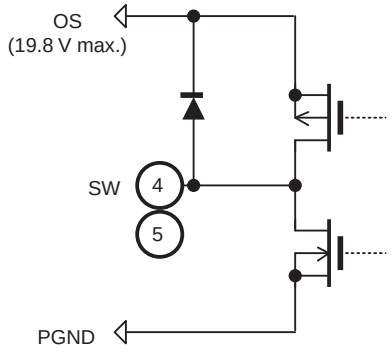

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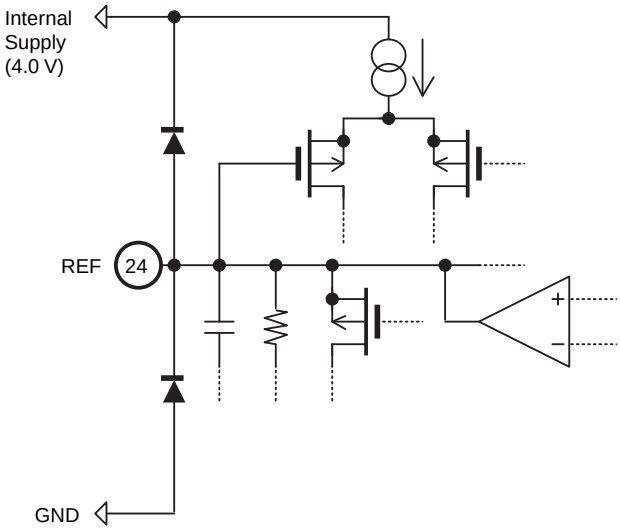

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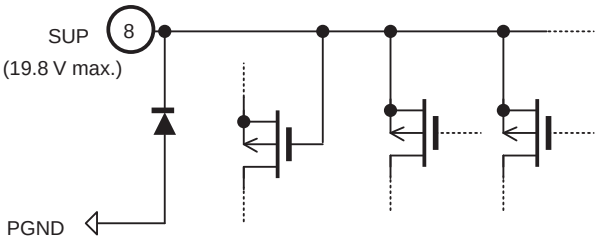

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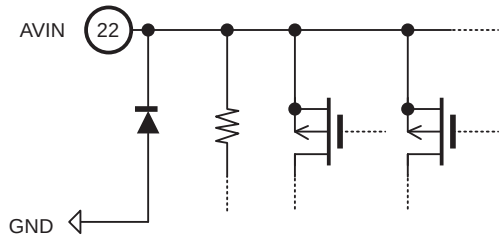

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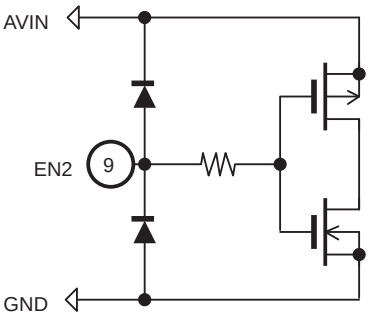
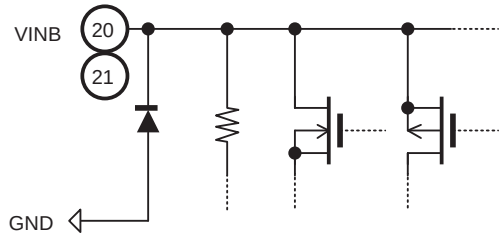


<Power supply (Buck Converter)>



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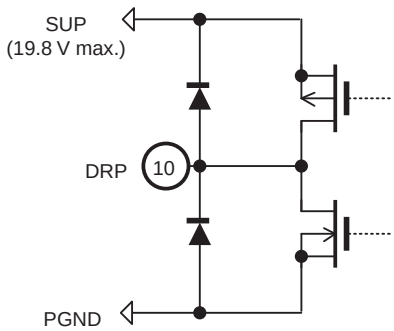

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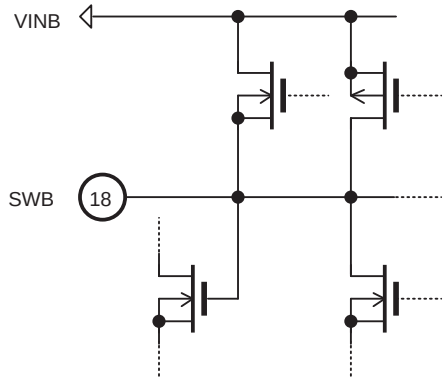

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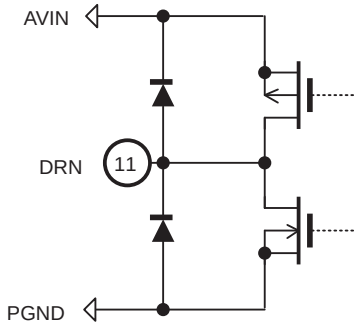
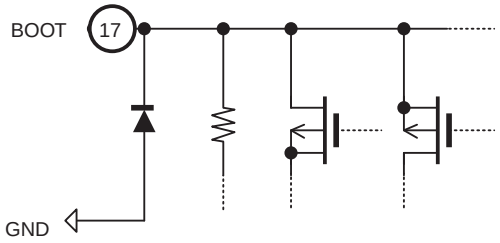
<Switching Output (Negative Charge Pump)>



<Boot Strap (Buck Converter)>



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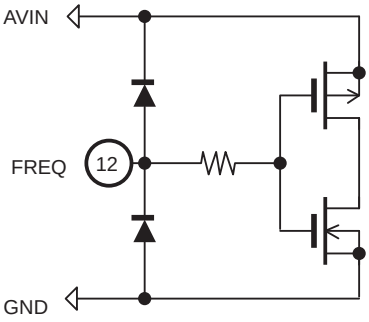

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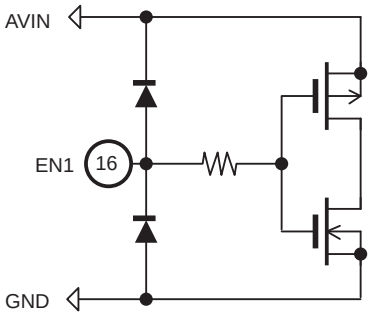
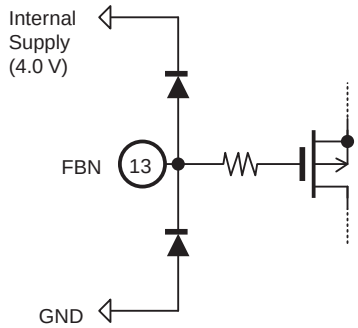


<Error Amplifier (Negative Charge Pump)>



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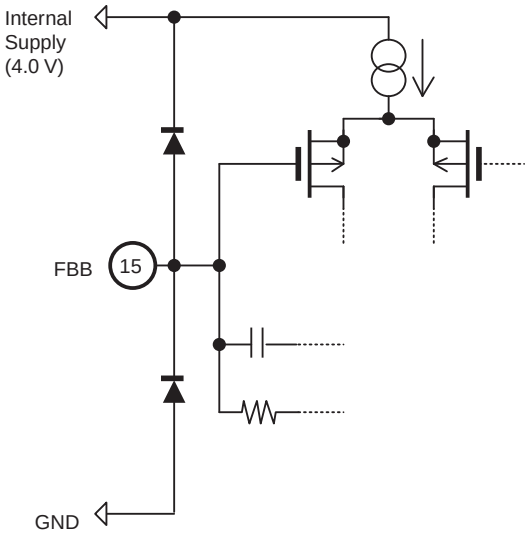

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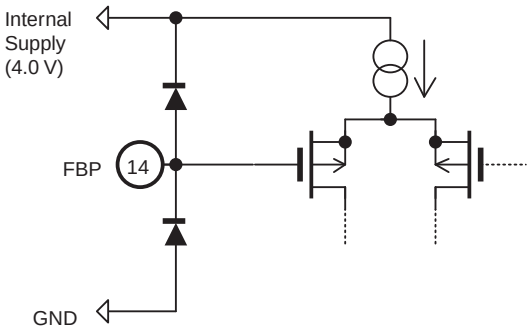
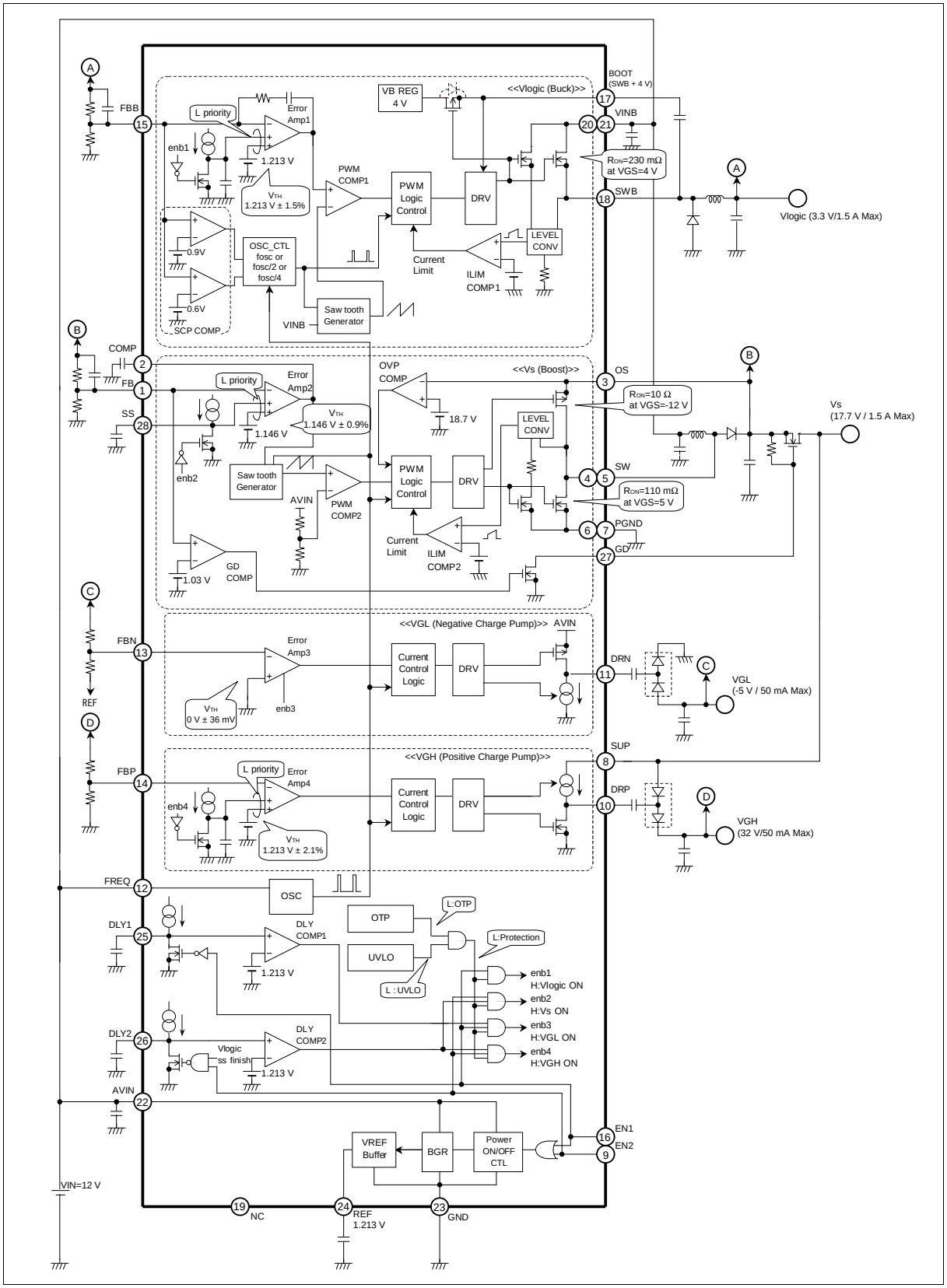


■ BLOCK DIAGRAM



■ FUNCTIONAL DESCRIPTIONS

V_{LOGIC} : Buck Converter

The Buck converter is a fixed frequency PWM control asynchronous converter with integrated NMOS power switch. It features voltage mode control with input feed forward to improve line regulation performance. The converter is internally compensated and is designed to work with ceramic output capacitor. The main switch of the converter is a 3.2 A rated power NMOS with gate drive circuit reference to SWB pin (source terminal of the NMOS power FET). The gate drive circuit is powered from an internal 4 V regulator and is bootstrapped from SWB pin via an external capacitor to achieve driving capability beyond the supply rail.

Soft Start (Buck Converter)

The Buck converter has build in soft start control to limit the inrush current at start up. The soft start cycle start after EN1 is asserted and the duration is internally set to 1 ms. During the soft start cycle, the second non-inverting input of the error amplifier, refer to the block diagram, ramps up from 0 V.

Thus, the Buck converter output ramps up in a control manner. The soft start cycle ends when the voltage on the second non-inverting input of the error amplifier rises above the reference voltage of 1.213 V.

Short Circuit Protection (Buck Converter)

The Buck converter is protected from short circuit fault by internal cycle-to-cycle current limit. In addition, the switching frequency is reduced to limit the power dissipation during the fault condition.

The switching frequency reduction depends on the voltage on FBB pin. When the voltage of FBB pin is below 0.9 V and 0.6 V, the switching frequency reduces to 1/2 and 1/4 of the normal value respectively.

The switching frequency becomes normal automatically if the normal situation was resumed.

V_S : Boost Converter

The Boost converter features fixed frequency pulse width modulated (PWM) control with integrated NMOS power switch. The switching frequency can be set to either 500 kHz or 750 kHz via the FREQ pin. The converter operates as an asynchronous Boost converter with external Schottky diode. The use of voltage mode control with input feed forward improves line regulation performance. In addition, the converter is designed with external frequency compensation that allows flexibility on selecting external component values.

A PMOS switch with on resistance of 10 Ω connects between SW and OS pin so that it operates in parallel with the external Schottky diode. At high loading current, most of the inductor current flows through the external Schottky diode. At light load, the PMOS switch provides a conduction path that allows the inductor current flow in reverse direction. As a result, the converter stays in continuous conduction mode for most of the load current range and allows the use of simple frequency compensation scheme.

Soft Start (Boost Converter)

A build in soft start circuit with an external capacitor connects to SS pin provides soft start function for the Boost converter to prevent high inrush current during start up. The SS pin provides a constant charging current so that soft start time is adjustable by changing the capacitance value of an external capacitor. During start up, the output voltage of the Boost converter is controlled by the SS pin until the voltage on SS pin is higher than the voltage on FB pin and the soft start cycle ends.

Over Voltage Protection (Boost Converter)

The Boost converter has build in over voltage protection to prevent MB39C313 from being damaged due to excessive voltage stress under fault conditions such as FB pin is left floating or short to ground.

The protection circuitry monitors the Boost converter output via OS pin and shut down the NMOS power FET that connects to SW pin when the voltage on OS pin is higher than 18.7 V. As a result, the inductor current start to fall and the output of the Boost converter follows. The Boost converter resumes normal operation when the voltage at OS pin falls below the protection threshold.

Gate Drive Pin (GD)

GD pin is an open drain output that triggers (pulls “Low”) after DLY2 expires and the voltage at FB pin rise above 1.03 V (90 % of FB reference voltage, 1.146 V). 1.03 V at FB pin translates to 90 % of the regulation point of the Boost converter. GD pin remains “Low” until the input voltage or voltage on EN2 is cycled to ground.

V_{GL} : Negative Charge Pump

The negative charge pump uses fixed switching frequency regulated architecture. The output voltage is set externally by a resistor divider. The regulation is done by controlling the pump current in the driver. Refer to the system block diagram, the charge pump use external diodes, pumping capacitor and output filter capacitor. Since the input of the charge pump and the driver is connected to the supply pin (VIN), the maximum negative output voltage is -VIN + V_{loss}. V_{loss} includes voltage drop in external diodes and gate driver. Additional charge pump stage can be added to generate larger negative voltage.

V_{GH} : Positive Charge Pump

The positive charge pump uses fixed switching frequency regulated architecture. The output voltage is set externally by a resistor divider. The regulation is done by controlling the pump current in the driver.

Refer to the system block diagram, the charge pump use external diodes, pumping capacitor and output filter capacitor. The input of the charge pump is connected to the V_S (Boost converter output) and the pump capacitor is charged to V_S during charging phase. As the supply to the driver (SUP pin) can be either the V_S (Boost converter output) or the VIN (supply PIN) of MB39C313, the maximum output voltage is V_{SUP} + V_S. Additional charge pump stage can be added to increase the maximum output voltage.

Common Block

Under Voltage Lockout

MB39C313 will shutdown when the supply voltage below 6 V to prevent improper operation of the device.

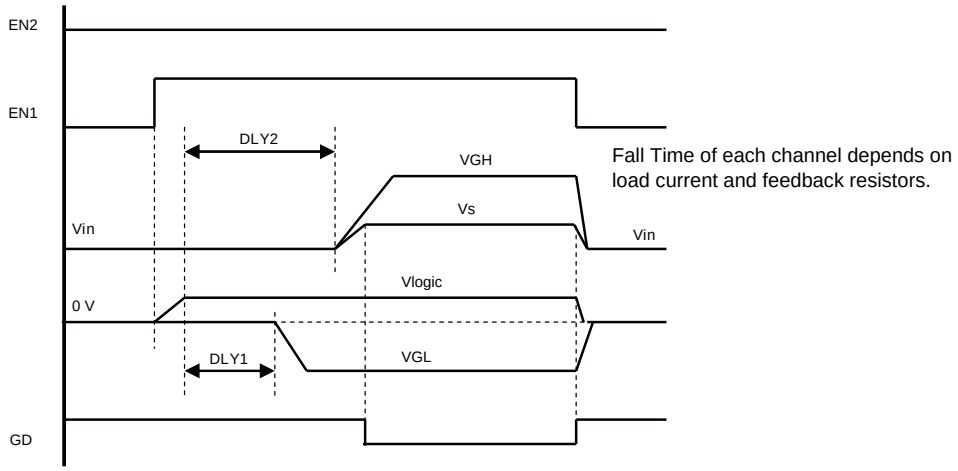
Over Temperature Protection

When the junction temperature rises above 150 °C, most of the active circuitries are shutdown to prevent damage from excessive power dissipation beyond safety limits.

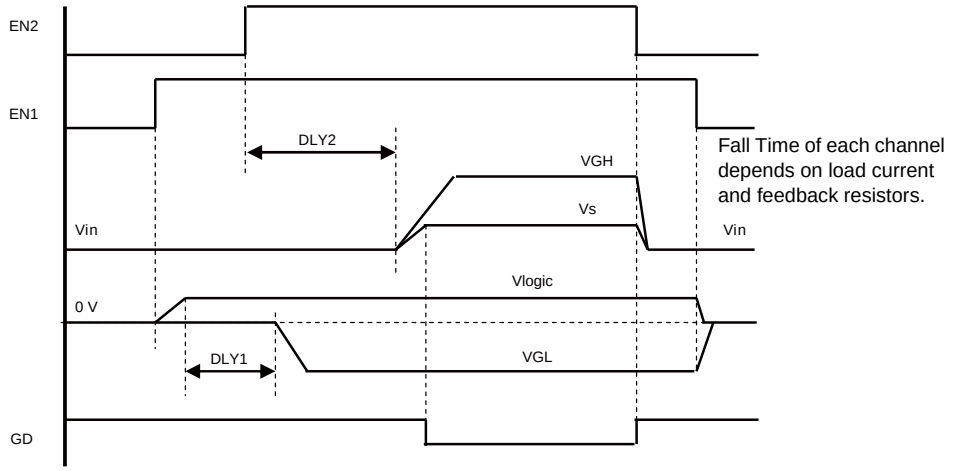
Power Up Sequencing (EN1, EN2, DLY1, DLY2)

EN1 and EN2 pin control the power up sequence of MB39C313. The timing of the sequencing events is controlled by the capacitance on DLY1 and DLY2 pins. By pulling EN1 high, the Buck converter enables first. Then, the Negative Charge Pump is enabled after some delay time, DLY1. Pulling EN2 high, the Boost converter and Positive Charge Pump are enabled at the same time with some time delay, DLY2. If EN2 pin is pulled high when the Buck converter is already operating, the time delay DLY2 starts at the EN2 rising edge, Figure1. Setting such delay time can be particularly useful if EN2 is already connected to input voltage (VIN). If EN2 is pulled high before the Buck converter is operating, the time delay DLY2 starts after the Buck converter is fully on, Figure2.

- Figure 1. Power-On sequence with EN2 is always high



- Figure 2. Power-On sequence with EN1 and EN2 enabled separately



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power supply voltage	V_{DD}	AVIN,VINB pin	– 0.3	+ 17	V
	V_{BOOT}	BOOT pin	– 0.3	+ 19.8	V
	V_{SUP}	SUP pin	– 0.3	+ 19.8	V
Input voltage	V_{FB}	FB, FBB, FBN, FBP pin	– 0.3	+ 7	V
	V_{OS}	OS pin	– 0.3	+ 19.8	V
	V_{GD}	GD pin	– 0.3	+ 19.8	V
	V_{EN}	EN1,EN2 pin	– 0.3	+ 17	V
	V_{FREQ}	FREQ pin	– 0.3	+ 17	V
SW Voltage	V_{SWB}	SWB pin	– 0.7	+ 17	V
	V_{SW}	SW pin	– 0.3	+ 19.8	V
SW peak current	I_{SWB}	SWB pin AC	—	3.9	A
	I_{SW}	SW pin AC	—	4.2	A
Power dissipation	P_D	Ta ≤ + 25 °C	—	3.44*	W
Storage temperature	T_{STG}	—	– 55	+125	°C

* : When mounted on a 100mm × 100 mm: 4 layer.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATION CONDITIONS

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power supply voltage	V_{DD}	AVIN, VINB pin	8	12	14	V
	V_{BOOT}	BOOT pin	13	17	18	V
	V_{SUP}	SUP pin	8.0	12.0	18.1	V
REF pin output current	I_{REF}	REF pin	– 50	—	0	µA
Input voltage	V_{FB}	FB, FBB,FBN, FBP pin	0	—	5.5	V
	V_{OS}	OS pin	0	—	18.1	V
	V_{GD}	GD pin	0	—	18.1	V
	V_{EN}	EN1,EN2 pin	0	—	14	V
	V_{FREQ}	FREQ pin	0	—	14	V
Output voltage	V_O	Vlogic: Buck Converter	1.8	—	3.3	V
	V_O	Vs: Boost Converter	—	—	18.1	V
Output current	I_O	Vlogic: Buck Converter DC	—	—	1.5	A
	I_O	Vs: Boost Converter DC VIN = 12 V, Vs = 15 V, L = 10 µH	—	—	1.5	A
	I_{SWB}	SWB pin DC	– 1.5	—	—	A
	I_{SW}	SW pin DC	—	—	1.5	A
	I_{GD}	GD pin	—	—	1	mA
	I_{OS}	OS pin	– 100	—	+100	mA
	I_{DRN}	DRN pin	– 100	—	+100	mA
	I_{DRP}	DRP pin	– 100	—	+100	mA
SW inductor	L_{SWB}	SWB pin	10	—	15	µH
	L_{SW}	SW pin	6.8	10.0	22.0	µH
BOOT pin capacitor	C_{BOOT}	BOOT pin	0.01	0.10	1.00	µF
REF pin capacitor	C_{REF}	REF pin	0.10	0.22	1.00	µF
DRP, DRN pin capacitor	C_{DR}	DRP, DRN pin	0.10	0.47	1.00	µF
SS pin capacitor	C_{SS}	SS pin	—	0.022	1.000	µF
DLY pin capacitor	C_{DLY}	DLY1, DLY2 pin	—	0.01	1.00	µF
Vlogic output filter capacitor	Cout	Vlogic: Buck Converter	—	20	—	µF
Vs output filter capacitor	Cout	Vs: Boost Converter	—	66	—	µF
Operating ambient temperature	Ta	—	– 30	+ 25	+ 85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

(Ta = + 25 °C, AVIN = VINB = SUP = 12 V)

Parameter		Symbol	Pin No.	Condition	Value			Unit
					Min	Typ	Max	
Reference Voltage Block [VREF]	Output voltage	V_{REF}	24	REF = 0 mA	1.203	1.213	1.223	V
Bias Voltage Block [VB]	Output voltage	V_B	17	BOOT = -1 mA, BOOT pin	3.5	4.0	4.5	V
Under Voltage Lockout Protection Circuit Block [UVLO]	Threshold voltage	V_{TLH}	22	AVIN = ↘	5.6	6.0	6.4	V
	Hysteresis width	V_H	22		—	0.2*	—	V
Over Temperature Protection Block [OTP]	Stop temperature	T_{OTPH}	—	T junction	—	+ 150*	—	°C
	Hysteresis width	T_{OTPHYS}	—		—	+ 15*	—	°C
Oscillator Block [OSC]	Output frequency	f_{OSC}	4, 5, 10, 11, 18	FREQ = “H”	600	750	900	KHz
		f_{OSC}	4, 5, 10, 11, 18	FREQ = “L”	400	500	600	KHz
	Input voltage	V_{IH}	12	f_{OSC} = 750 KHz set	1.7	—	—	V
		V_{IL}	12	f_{OSC} = 500 KHz set	—	—	0.4	V
Sequence Control Block [SEQ CTL]	Threshold voltage	V_{TH}	25, 26	DLY1, DLY2 pin	1.123	1.180	1.239	V
	Charging current	I_{DLY}	25, 26	DLY1, DLY2 = 0 V	3.8	5.5	7.1	µA
Control Block [CTL]	Input voltage	V_{IH}	9,16	EN1, EN2 ON	2	—	—	V
		V_{IL}	9,16	EN1, EN2 OFF	—	—	0.8	V
General	Stand by current	I_{CCS}	22	EN1, EN2 = 0 V, AVIN pin	—	0	1	µA
		I_{CCS}	20, 21	EN1, EN2 = 0 V, VINB pin	—	0	1	µA
		I_{CCS}	8	EN1, EN2 = 0 V, SUP pin	—	0	1	µA
	Power supply current	I_{CC}	22	EN1, EN2 = AVIN, AVIN pin	—	1	2	mA
		I_{CC}	20, 21	EN1, EN2 = AVIN, VINB pin	—	0.2	0.5	mA
		I_{CC}	8	EN1, EN2 = AVIN, SUP pin	—	0.2	2.0	mA

(Continued)

Parameter		Symbol	Pin No.	Condition	Value			Unit
					Min	Typ	Max	
Vlogic [Buck Converter]	Threshold voltage	V_{TH}	15	FBB pin	1.195	1.213	1.231	V
	Input bias current	I_B	15	FBB = 0 V	-100	0	+100	nA
	SW NMOS-Tr On resistor	R_{ON}	18, 20, 21	SWB = -500 mA VGS = 4 V	—	230*	—	mΩ
	SW NMOS-Tr Leak current	I_{LEAK}	18, 20, 21	EN1 = 0 V SWB = 0 V	-10	—	—	µA
	Over current protect	I_{LIM}	18	SWB pin	2.5	3.2	3.9	A
	Short circuit protect threshold voltage	V_{TH}	15	$f_{OSC} \times 1/2$	0.855	0.900	0.945	V
		V_{TH}	15	$f_{OSC} \times 1/4$	0.57	0.60	0.63	V
	Soft-start time	tss	15	FBB pin	0.69	1.00	1.50	ms

(Continued)

Parameter		Symbol	Pin No.	Condition	Value			Unit
					Min	Typ	Max	
Vs [Boost Converter]	Threshold voltage	V_{TH}	1	FB pin	1.136	1.146	1.156	V
	Input bias current	I_B	1	FB = 0 V	-100	0	+100	nA
	SW NMOS-Tr On resistor	R_{ON}	4,5	SW = 500 mA VGS = 5 V	—	110*	—	mΩ
	SW PMOS-Tr On resistor	R_{ON}	3,4,5	OS = -200 mA VGS = 12 V	—	10	16	Ω
	SW NMOS-Tr Leak current	I_{LEAK}	4,5	EN2 = 0 V OS = 15 V SW = 0 V	—	—	10	µA
	SW PMOS-Tr Leak current	I_{LEAK}	3	EN2 = 0 V SW = 15 V	—	—	10	µA
	Over current protect	I_{LIM}	4,5	SW pin	2.8	3.5	4.2	A
	Over voltage protect	V_{OVP}	3	OS = ⌟↑	18.5	18.7	18.9	V
	Soft-start charging current	Iss	28	SS = 0 V	10	15	20	µA
	GD Thresh old voltage	V_{TH}	1	FB = ⌟↑	1.01	1.03	1.05	V
	GD “L” level output voltage	V_{OL}	27	GD = 500 µA	—	—	0.3	V
	GD output leak current	I_{LEAK}	27	GD = 17 V	—	—	1	µA
VGL [Negative Charge Pump]	Threshold voltage	V_{TH}	13		-36	0	+36	mV
	Input bias current	I_B	13	FBP = 0 V	-100	0	+100	nA
	On resistor	R_{ON}	11	IDRVN = -20 mA	—	4.4	6.6	Ω
	I/O voltage difference	Vdrop	11	DRN = 50 mA FBP = nominal-5%	—	130	190	mV
		Vdrop	11	DRN = 100 mA FBP = nominal-5%	—	270	420	mV

(Continued)

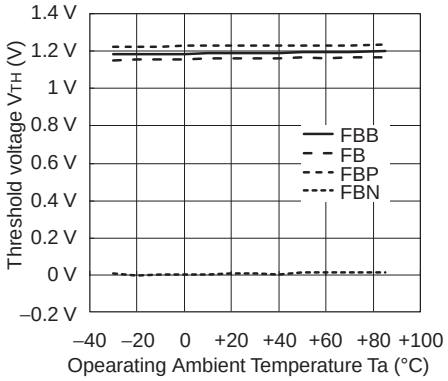
(Continued)

Parameter		Symbol	Pin No.	Condition	Value			Unit
					Min	Typ	Max	
VGH [Positive Charge Pump]	Threshold voltage	V_{TH}	14		1.187	1.213	1.238	V
	Input bias current	I_B	14	FBP = 0 V	-100	0	+100	nA
	On resistor	R_{ON}	10	Iout = 20 mA	—	1.10	1.65	Ω
	I/O voltage difference	Vdrop	10	Vdrop = SUP-DRP DRP = -50 mA FBP = nominal-5%	—	400	680	mV
		Vdrop	10	Vdrop = SUP-DRP DRP = -100 mA FBP = nominal-5%	—	850	1600	mV

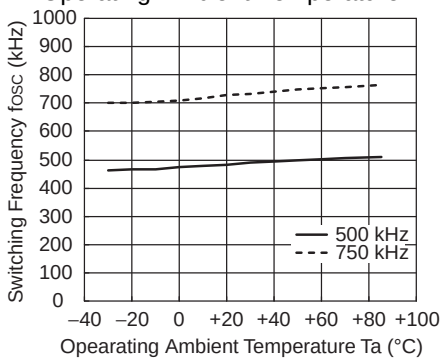
* : This parameter isn't be specified. This should be used as a reference to support designing the circuit

■ TYPICAL CHARACTERISTICS

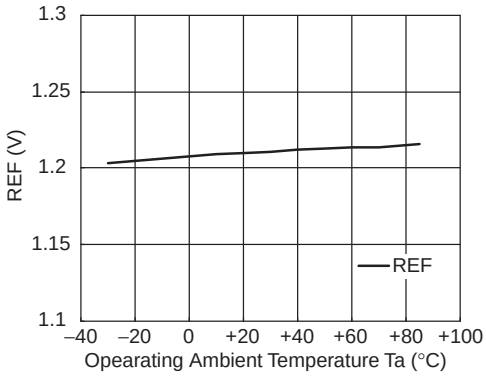
Threshold voltage vs.
Operating Ambient Temperature



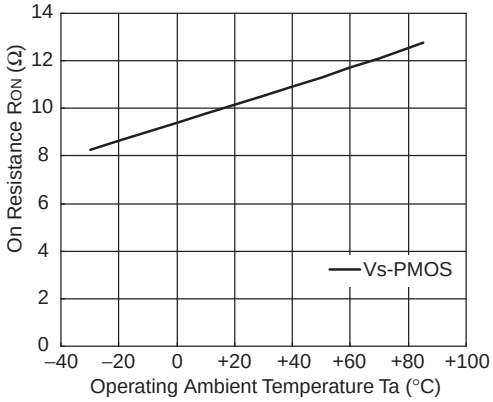
Switching Frequency vs.
Operating Ambient Temperature



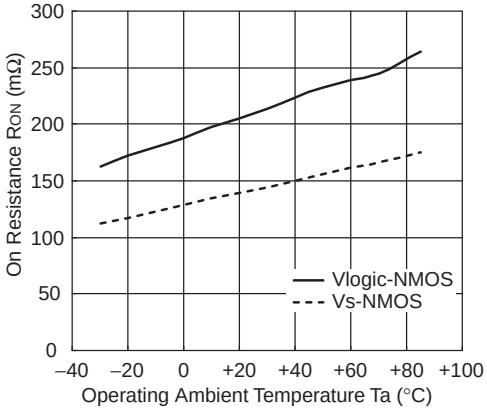
REF vs.
Operating Ambient Temperature



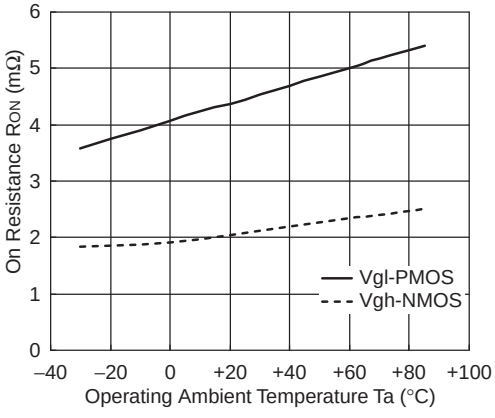
RON Resistance vs.
Operating Ambient Temperature



RON Resistance vs.
Operating Ambient Temperature



RON Resistance vs.
Operating Ambient Temperature



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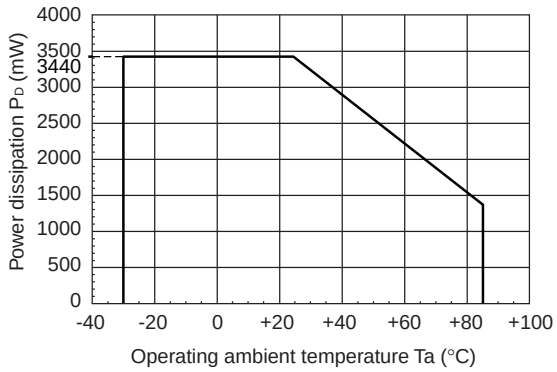
Power dissipation vs. Operating ambient temperature



■ SET UP

1. Setting Control Pin

Pin	Channels	Standby	Operating
EN1	V_{LOGIC}: Buck converter	L	H
	V_{GL}: Negative Charge Pump		
EN2	V_S: Boost converter	L	H
	V_{GH}: Positive Charge Pump		

2. Setting Switching Frequency

Pin	Setting	Internal oscillator frequency
FREQ	H	750 kHz
	L	500 kHz

3. Protection Circuitry

3.1) IC

Under voltage lock out: AVIN ≤ 6 V, all channels shut down

3.2) V_{LOGIC} : Buck Converter

Short circuit protection: FBB pin < 0.9 V, protection circuit active
Over current protection: output current ≥ 3.2 A, protection circuit active

3.3) V_S : Boost Converter

Over voltage protection: V_S ≥ 18.7 V, protection circuit active
Over current protection: SW pin current ≥ 3.5 A, protection circuit active

3.3) V_{GL} : Negative Charge Pump

No protection circuits

3.4) V_{GH} : Positive Charge Pump

No protection circuits

4. Others

4.1) DLY1 / DLY2 delay time setting

With time delay (t_{delay}): DLY1 / DLY2 = open

Without time delay (t_{delay}): for each DLY1 / DLY2,

$$C_{delay} = \frac{5.5\ \mu A \times t_{delay}}{V_{REF}}$$

Where:
t_{delay} = delay time,
C_{delay} = Capacitor value connected to DLY-pin,
V_{REF} = 1.213 V

4.2) V_{LOGIC} : Buck converter

Output voltage setting :

$$VO1 = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

Where:
V_{REF} = 1.213 V, R2 ≤ 1.2 kΩ

Feed-forward capacitance :

$$C_{ff1} = \frac{1}{2 \times \pi \times R1 \times f_{z1}}$$

Where :
f_{z1} = a zero in transfer function

Soft start:
Internal preset
The soft start cycle start after EN1 is asserted and the duration is internally set to 1 ms.

4.3) V_S: Boost converter

Output voltage setting:

$$VO2 = 1.146 \times \left(1 + \frac{R3}{R4}\right)$$

Feed-forward capacitance:

$$C_{ff2} = \frac{1}{2 \times \pi \times R3 \times f_{z2}}$$

Where :
f_{z2} = a zero in transfer function

Soft start:
set by external capacitor connected to SS pin
(Soft start active when SS pin voltage < FB voltage)

GD pin:
GD goes L if FB > 1.03 V after delay time DLY2
GD gives Hi-Z if FB ≤ 1.03 V after delay time DLY2

4.4) V_{GL} : Negative Charge Pump

Output voltage setting:

$$VO3 = (-V_{REF}) \times \frac{R5}{R6}, \text{ where } V_{REF} = 1.213\ V$$

4.5) V_{GH} : Positive Charge Pump

Output voltage setting:

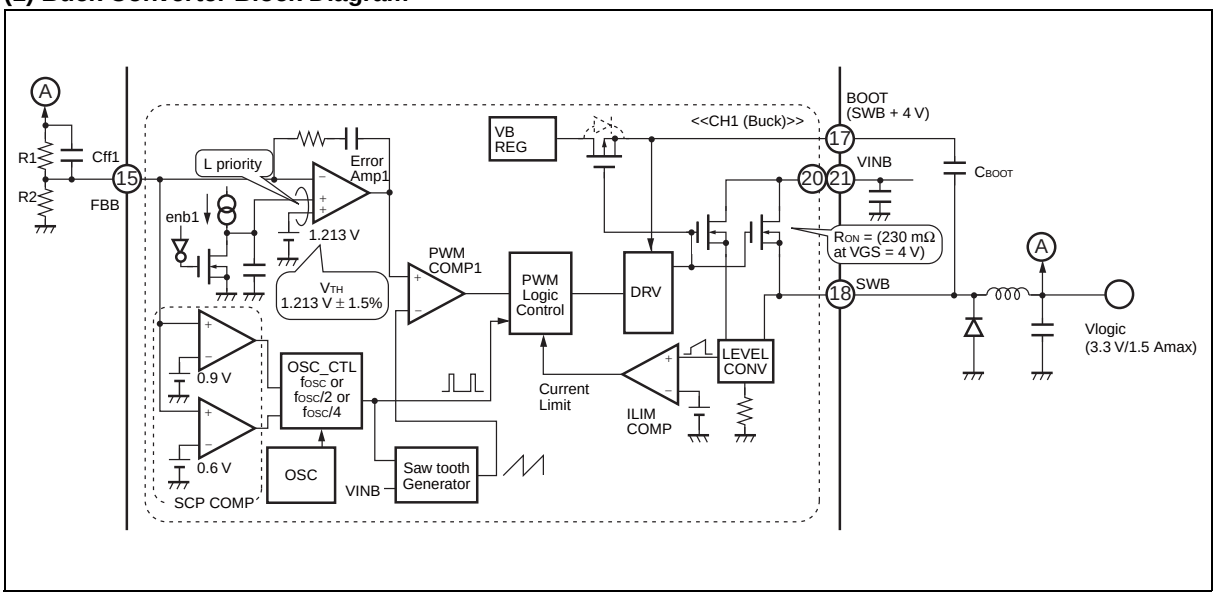
$$VO4 = V_{REF} \times \left(1 + \frac{R7}{R8}\right), \text{ where } V_{REF} = 1.213\ V$$

Note : refer to “■ APPLICATION MANUAL” for corresponding resistor.

■ APPLCATION MANUAL

1. Buck Converter Design

(1) Buck Converter Block Diagram



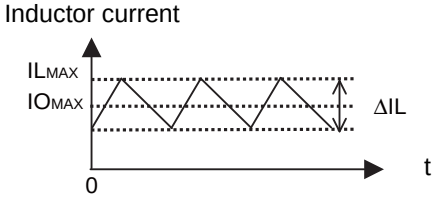
(2) Inductor Selection

The inductor can range from 10 µH to 15 µH. The current flow through the inductor must below the saturation current rating of the inductor. The maximum current flowing through the inductor can be found from the following formula:

$$I_{LMAX} \geq I_{OMAX} \frac{\Delta IL}{2}$$

$$\Delta IL = \frac{V_{in} \times V_{out}}{L} \times \frac{V_{OUT}}{V_{in} \times f_{OSC}}$$

Where
I_{LMAX} = Maximum current through inductor [A]
I_{OMAX} = Maximum load current [A]
ΔIL = Inductor ripple current peak-to-peak value [A]
V_{in} = Input voltage [V]
V_{out} = Output voltage [V]
f_{OSC} = switching frequency [Hz] (500 kHz or 750 kHz)



(3) Rectifier Diode Selection

Schottky diode should be used to attain high efficiency. The reverse voltage rating of the diode must be higher then the maximum output voltage of the converter. The required averaged rectified forward current of diode is the product of off-time of Buck converter and the maximum switch current at SWB pin.

$$\text{Off-time of Buck converter: } D = 1 - \frac{V_{out}}{V_{in}} = 1 - D$$

$$\text{Maximum output current: } I_{avg} = (1 - D) \times I_{SWLIM} = \left(1 - \frac{V_{in}}{V_{out}}\right) \times I_{SWLIM}$$

A Schottky diode with maximum rectified forward-current of 1.5 A to 2 A should be sufficient for most of applications. The diode forward voltage should be less than 0.7 V in order to prevent damage to IC.

Another requirement for Schottky diode is the power dissipation. The power dissipation can be calculated from the formula below:

$P_D = I_{avg} \times V_F = (1 - D) \times I_{SWLIM} \times V_F$

Where
P_D = Power dissipation of the diode [W]
V_F = Diode forward voltage [V]
I_{SWLIM} = Minimum over current protection of SWB-pin [A] (2.5 A)

(4) Bootstrap Capacitor Selection

Bootstrap capacitor connected to BOOT pin is charged by integrated synchronous diode with 4 V internal supply. Ceramic capacitor is recommended for less leakage current. The minimum bootstrap capacitor can be calculated by following equation:

$$C_{BOOT} \geq \frac{Q_{GATE} + \frac{I_{DRV\,(dynamic)}}{f} + Q_{DRV\,(static)} \frac{I_{CBOOT\,(leak)}}{f}}{V_B - V_f - V_{LS} - V_{min}}$$

Where:
C_{BOOT} = bootstrap capacitor value
Q_{GATE} = gate charge of integrated power transistor
f = switching frequency (500 kHz or 750 kHz)
$I_{DRV(dynamic)}$ = dynamic current of power transistor driver
$Q_{DRV(static)}$ = static current of power transistor driver
$I_{CBOOT(leak)}$ = bootstrap capacitor leakage current
V_B = internal regulated voltage 4 V
V_f = forward voltage drop of bootstrap diode
V_{LS} = voltage drop of low-side diode of Buck converter
V_{min} = minimum voltage between BOOT pin and SWB pin

Practically, bootstrap capacitor is selected more than ten times of its minimum value, such that providing sufficient charge for driver and gate of power transistor. With assumption on power used is dominated by charging the gate capacitor of power transistor, the equation can be simplified:

$C_{BOOT} \geq \frac{Q_{GATE}}{\Delta V}$, where ΔV is the change of boot voltage in switching cycle.

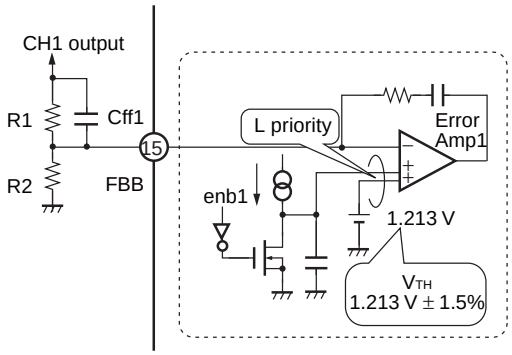
0.1 µF bootstrap capacitor is recommended for Buck converter in MB39C313. The bootstrap capacitor voltage rating is suggested to be high than input voltage.

(5) Output Capacitor Selection

This IC is designed to work best with ceramic output capacitor. Two 10 µF ceramic output capacitors are recommended for most application. More capacitance can be added so as to reduce voltage drop during load transients.

(6) Output Voltage and Feed Forward Capacitor Selection

- Equivalent circuit of Buck converter error amp block



The output voltage of Buck converter can be set by external resistor divider as shown below:

$$V_{LOGIC} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) = 1.213 \times \left(1 + \frac{R1}{R2}\right)$$

R2 is around 1.2 kΩ, and the reference voltage (V_{REF}) = 1.213 V

The lower feedback resistor (R2) should be around 1.2 kΩ to maintain a minimum load current of 1 mA.

If the loading current is less than 1 mA, the output voltage will rise slightly above the nominal voltage in light load or no load condition.

A feed forward capacitor (C_{ff1}) is added parallel to the upper resistor (R1). The C_{ff1} sets a zero in the transfer function. This will improve the load transient response and stabilize the converter loop. The value of C_{ff1} is depending on the inductor and zero frequency (f_{z1}) required.

For 10 µH inductor, set f_{z1} = 8 kHz; for 15 µH inductor, set f_{z1} = 17 kHz.

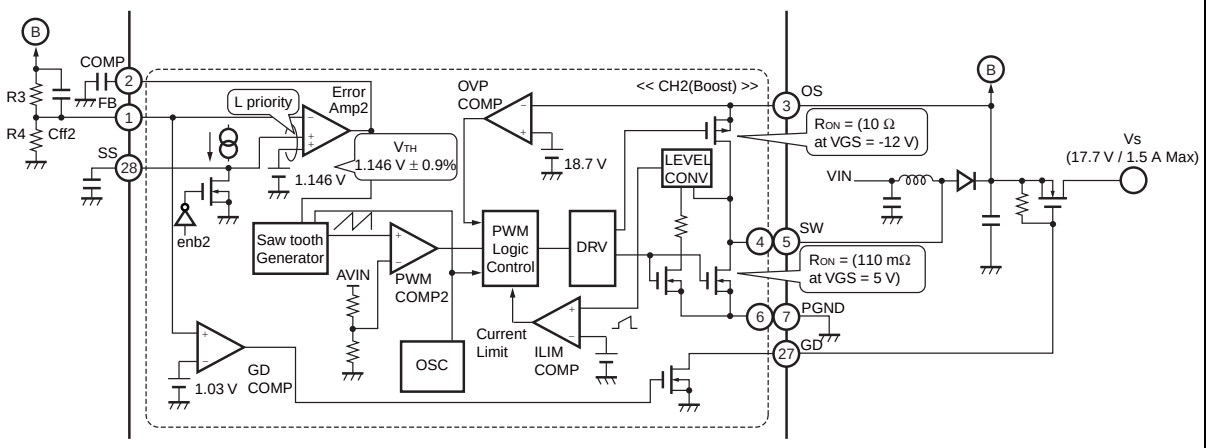
$$C_{ff} = \frac{1}{2 \times \pi \times R1 \times f_z} = \frac{1}{2 \times \pi \times 2\ k\Omega \times 8\ kHz} = 9.9\ nF \fallingdotseq 10\ nF \text{ (Example of 3.3 V output voltage)}$$

A capacitor value close to the calculated value is chosen.

2. Boost Converter Design

(1) Boost Converter Block Diagram

- Figure 3. Boost converter block diagram



It is necessary to verify the maximum output current of this converter whether it meets the application requirements. The efficiency of the Boost converter can be read from the graph or employ a worst-case assumption of 80 %.

$$\text{Duty cycle: } D = 1 - \frac{V_{in} \times \eta}{V_{out}}$$

$$\text{Maximum output current: } I_{avg} = (1 - D) \times I_{SWLIM} \frac{V_{in}}{V_{out}} \times I_{SWLIM}$$

$$\text{Peak switch current: } I_{SWPEAK} = \frac{V_{in} \times D}{2 \times f_{OSC} \times L} + \frac{I_{out}}{1 - D}$$

Where
D = duty cycle
f_{OSC} = switching frequency [Hz] (500 kHz or 750 kHz)
L = inductor value [H]
η = estimated Boost converter efficiency (typically 80 % minimum)
I_{SWLIM} = minimum switch current limit of SW-pin [A] (= 2.8 A)

The selected components, including the embedded switch, the inductor and external Schottky Diode must be able to handle the peak switching current. The estimation should be based on the minimum input voltage, since the switching current will be the highest in this case.

Limited by the power FET maximum switching current, the maximum output current depends on input voltage and output voltage configuration. Refer to “REFERENCE DATA” section for graphical information. For data reading from reference data, margin is suggested to avoid activating current limit.

Inductor Selection

The inductor can range from 6.8 µH to 22 µH. When selecting the inductor, its saturation current must be higher than the peak switch current (I_{SWPEAK}) as shown above. Extra margin is required to cope with high current transients. A more conservative design is to use the maximum SW current limit of 3.5 A as saturation current rating of inductor. Another parameter for choosing inductor is the DC resistance.
Usually, lower the DC resistance can result in higher converter efficiency.

(2) Rectifier Diode Selection

Schottky diode should be used to attain high efficiency. The reverse voltage rating of the diode must be higher than the maximum output voltage of the converter. Similar to Buck converter, the required averaged rectified forward current of the Schottky diode is the product of off-time of Boost converter and the maximum switch current at SW pin.

$$\text{Off-time of Boost converter: } D = 1 - D = \frac{V_{in}}{V_{out}}$$

$$\text{Maximum output current: } I_{avg} = (1 - D) \times I_{SWLIM} \frac{V_{in}}{V_{out}} \times I_{SWLIM}$$

A Schottky diode with maximum rectified forward-current of 2A should be sufficient for most applications. Another requirement for Schottky diode is the power dissipation. The power dissipation can be calculated from the formula below:

$$P_D = I_{avg} \times V_F = (1 - D) \times I_{SWLIM} \times V_F$$

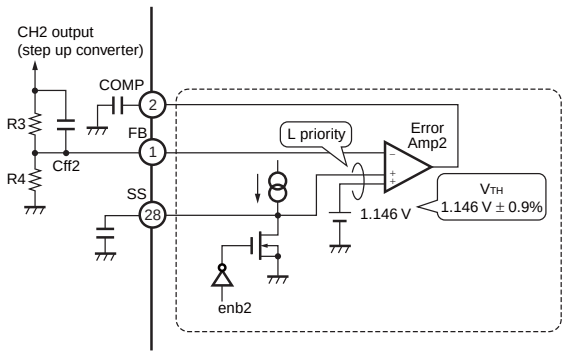
Where
P_D = power dissipation of the diode [W]
V_F = diode forward voltage [V]
I_{SWLIM} = minimum over current protection of SW-pin [A] (2.8 A)

(3) Output Capacitor Selection

Capacitors with low ESR are recommended. Ceramic capacitor which has low ESR is particularly suitable for this purpose. Typically, three 22 µF ceramic capacitors connected in parallel are placed at the converter output. More capacitance can be added so as to reduce voltage drop during heavy load transients.

(4) Output Voltage and Feed Forward Capacitor Selection

- Equivalent circuit of Boost converter error amp block



The Boost converter output voltage of can be set by external resistor divider as shown below:

$$V_S = 1.146 \times \left(1 + \frac{R3}{R4}\right)$$

Note : Output overshot due to large input voltage change may be high enough to trigger OVP under certain condition when output setting is close to 18 V.

A feed forward capacitor (C_{ff2}) is added parallel to the upper resistor (R3). The C_{ff2} sets a zero in the control loop transfer function. This improves the load transient response and stabilizes the converter loop. The value of C_{ff2} is depending on the inductor and zero frequency (f_{z2}) required.

For 6.8 µH and 10 µH inductor, set f_z = 10 kHz; for 22 µH inductor, set f_z = 7 kHz.

$$C_{ff2} = \frac{1}{2 \times \pi \times R3 \times f_{z2}} = \frac{1}{2 \times \pi \times 680\ k\Omega \times 10\ kHz} = 23.4\ pF \fallingdotseq 20\ pF \text{ (Example of 16.5 V output voltage)}$$

A capacitor value close to the calculated value can be used.

(5) Compensation (COMP) Capacitor Selection

The regulator compensation is adjusted by an external component connected to the COMP-pin. This pin is the output of internal trans-conductance error amplifier. By adding a resistor in series will change the internal zero and increases the high-frequency gain. The formula below give the frequency (Fz) at which the resistor increases the high-frequency gain.

$$F_Z = \frac{1}{2 \times \pi \times C_C \times (R_C + 10\ k)}$$

Typically, a 22 nF capacitor is suitable for most applications. If the input voltage is lower, it requires a smaller capacitor value so that it has higher regulator gain.

(6) Soft Start Capacitor Selection

A soft start function is to slow the rate of rising output voltage and minimize the large inrush current at startup. The soft start time is adjustable by connecting external capacitor to SS pin. Soft start capacitor can be estimated by defining the soft start time thought equation below:

$$C = \frac{I_{ss} \times t_{ss}}{V_{FB}},$$

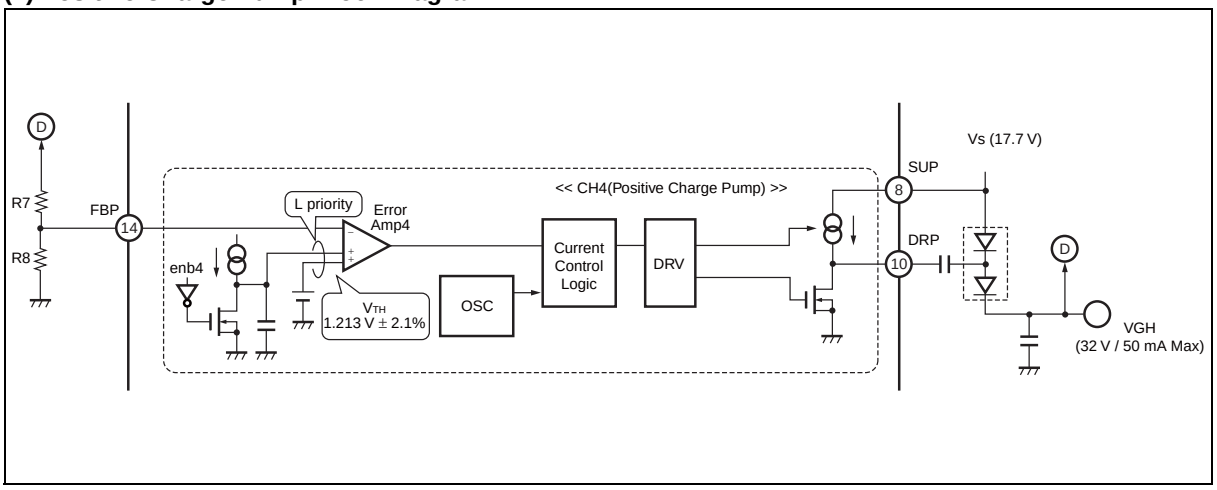
Where:
I_{ss} = soft start charging current;
t_{ss} = soft start time;
V_{FB} = voltage at FB pin.

In general, startup time for power supply is larger than 10 us. The startup time of Boost converter of MB39C313 is defined as 1.5 ms.

$$C = \frac{I_{ss} \times t_{ss}}{V_{FB}} = \frac{15\ \mu A \times 1.5\ ms}{1.146\ V} = 19.6\ nF,$$ therefore, 22 nF soft start capacitor is selected.

3. Positive Charge Pump Design

(1) Positive Charge Pump Block Diagram



(2) Output Voltage Selection

Theoretically, the maximum output voltage is the sum of input voltage and pumping clock voltage of a charge pump. In MB39C313, the maximum output voltage is V_S (Boost converter output voltage) + V_{SUP} – $2V_{diode}$ which is 17.7 V + 17.7 V + 2(0.4 V) = 34.6 V with typical setting. Due to the regulated voltage control, the output voltage can be configured by equation below:

$$V_{GH} = V_{REF} \times \left(1 + \frac{R7}{R8}\right) = 1.213 \times \left(1 + \frac{R7}{R8}\right)$$

Typically, multiple 2 (x2) function for Positive Charge Pump. Its output voltage will be limited by $V_S - 2V_{diode} \le V_{GH} \le V_s + V_{SUP} - 2\ V_{diode}$. For other application that requires higher output voltage, MB39C313 allows adding pumping stage by using SW pin. With multiple 3 (x3) function of Positive Charge Pump, the output voltage should be limited by $2V_S + V_{diode(Vs)} - 2V_{diode} \le V_{GH} \le 2V_S + V_{diode(Vs)} + V_{SUP} - 4V_{diode}$.

(3) Pumping Capacitor and Output Capacitor Selection

Ceramic capacitor is recommended for its non-polarized, more stable over temperature, low leakage and small ESR. Choosing a pumping capacitor should consider the required voltage rating and output current loading. For 32 V output voltage setting, the pumping clock voltage is calculated below.

$\Delta V_{DRP} = V_{GH} - V_S + 2(V_{diode}) = 32\ V - 17.7\ V + 2(0.4\ V) = 15.1\ V$

The minimum pumping capacitor is determined by following equation.

$$C \geq \frac{I_{out}}{f \times \Delta V_{DRP}},$$

Where:
Iout = the output current
f = switching frequency (500 kHz or 750 kHz)
ΔV_{DRP} = pumping clock voltage

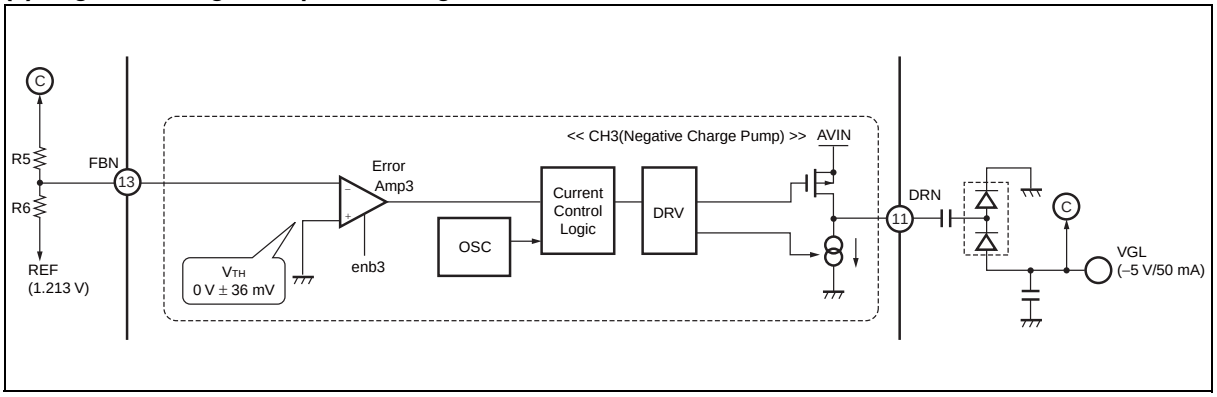
The charge stored on pumping capacitor is transferred to output capacitor cycle-by-cycle. Output capacitor determines output ripple voltage of charge pump. The ripple voltage is estimated by:

$$V_{ripple} = \frac{I_{out}}{2f \times C_{out}} + I_{out} \times ESR_{Cout}$$

Where:
C_{out} = output filtering capacitance
ESR_{Cout} = equivalent series resistance of output filtering capacitor

4. Negative Charge Pump Design

(1) Negative Charge Pump Block Diagram



(2) Output Voltage Selection

Recall from functional description, the maximum negative output voltage is $-V_{DRN} + V_{diode}$ ideally, which is –12 V + 0.4 V = –11.6 V. Similar to Positive Charge Pump, the regulated output voltage can be set by equation below:

$$V_{GL} = -V_{REF} \times \frac{R5}{R6} = -1.213 \times \frac{R5}{R6}$$

(3) Pumping Capacitor and Output Capacitor Selection

Selection of pumping capacitor and output capacitor are similar to Positive Charge Pump design.

For –5 V output, $\Delta V_{DRN} = -V_{GL} - V_{diode} = -5\ V - 0.4\ V = -5.4\ V$. The pumping capacitor and output filtering capacitor can be estimated for required application.

Fast input voltage change at power off causes under-shoot (becomes more negative) at Negative Charge Pump output. This under shoot can be reduced by increasing the output capacitance to pumping capacitance ratio. The power off coupling voltage is VIN – | ΔV_{DRN} |. The coupling effect can be estimated as below:

$$\Delta V_{under\text{-}shot} = (VIN - |\Delta V_{DRN}|) = \times \frac{C_{pump\text{-}cap}}{C_{pump\text{-}cap} + C_{outpu\text{-}cap}}$$

Where:
$\Delta V_{under-shot}$ = under-shot voltage by power off coupling.
ΔV_{DRN} = pumping clock voltage
$C_{pump\text{-}cap}$ = pumping capacitance
$C_{output\text{-}cap}$ = output capacitance

In real application, the power off coupling should be negligible due to large loading gate capacitance on panel.

(4) REF Capacitor Selection

REF pin capacitor is used for defining the low frequency gain of reference voltage buffer. 220 nF capacitor is used for stability and performance. Change of capacitance is NOT recommended.

(5) DLY Capacitor Selection

Refer to “Power Up Sequence” section, power up sequence timing is set by capacitor at DLY1 and DLY2 pins. The delay capacitor can be estimated by following equation.

$$C_{delay} = \frac{5.5\ \mu A \times t_{delay}}{V_{REF}}$$

Where:
t_{delay} = delay time
C_{delay} = capacitor connected to DLY-pin
V_{REF} = 1.213 V

(6) Input capacitor Selection

It is recommended to use low ESR capacitor like ceramic capacitor for the input filtering. For AVIN terminal, a 1 µF capacitance connected from AVIN to ground is needed. For the Buck converter, use minimum of two 22 µF ceramic capacitors connected from VINB pin to ground. For the Boost converter, minimum of one 22 µF ceramic capacitor connected from the inductor terminal to ground is recommended.

5. System Design Consideration

(1) Output Glitches when Very Slow Power up Time

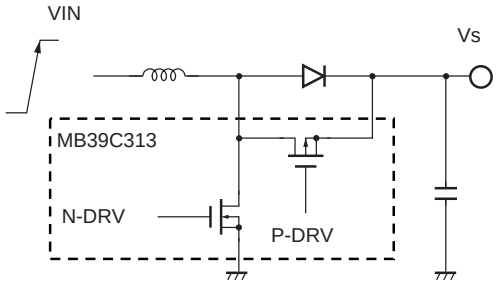
A very slow power up time may cause channel output glitches when input voltage across UVLO voltage. Due to slow rise of input voltage at UVLO threshold, the UVLO is easily triggered with switching noise. This undesired UVLO activation will cause glitches at output when channel is loaded.

The main reason is due to the input voltage drop by sudden current draw when channel startup. For maximum output loading, 0.1 Ω equivalent series resistance of power line is able to cause 0.3 V voltage drop. Consider UVLO hysteresis voltage and its response time with margin. For typical setting (VIN = 12 V, V_{Logic} = 3.3 V/ 1.5 A and other channels without load, 0.1 Ω source resistance), it is suggested less than 167 ms input voltage ramp time to avoid such glitches. Refer to "■ TYPICAL APPLICATION CIRCUIT" for typical application setting.

(2) Voltage Overshot at Boost Converter Output during Power Up

A voltage overshot appears at Boost Converter output when input voltage rise time is too fast. This overshot voltage may damage external parts.

- Figure 4. Simplified Boost Converter of MB39C313.



Refer to Figure 4, consider the node voltage at power up, both gate voltage of P-type and N-type power FET are zero. With sudden voltage change at input, current flow through inductor and charge up the output capacitor towards input voltage. The P-type power FET will be turned off when output capacitor rise to certain voltage. The charging current continues to flow through the Schottky diode, such that capacitor reaches its peak voltage. As the diode blocks the reverse current, the output capacitor voltage can only be discharged by loading elements.

To avoid this overshot voltage at power up, the rise time of input voltage should be controlled base on RLC resonance frequency of application circuit. No load condition can be used to estimate worst case.

The LC resonance frequency is $\frac{1}{2\pi\sqrt{LC}}$

For typical application, L = 6.8 µH, C = 66 µF, the theoretical input rise time should be longer than 133 µs.

Margin is suggested for other parasites.

(3) GD FET Isolation

An isolation switch for Boost Converter output is suggested to break current path for application in disable condition. The isolation switch can be controlled by GD pin. Refer to Figure 3 for its application connection.

(4) PCB Layout Recommendation

PCB layout is significant for power supply design. Poor layout would result in generating unwanted voltage and current spikes. This will not only affect DC output voltage, but also radiate EMI to adjacent equipment. Sufficient grounding and minimize parasitic inductance can reduce DC/DC converter switching spike noise.

The following list of rules should be followed when designing power PCB layout

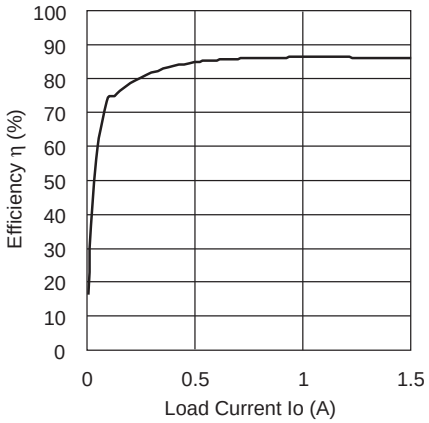
1. Place tracks on the Top Layer and avoid using via or through hole; particularly for nets, such as Input Capacitor (Cin), Inductor (L) and Output Capacitor (Cout).
2. Place the Input Capacitor (Cin) close to the IC, so as to reduce loop current.
3. Place the Schottky diodes close to the SW and SWB respectively, so as to reduce spike noise.
4. Strengthen the ground connection of Input Capacitor (Cin), and Output Capacitor (Cout) with the ground planes. This can be done by placing via holes next to the GND terminals of these components.
5. Place the Schottky Diode and Pumping Capacitor of the two charge pump channels close to IC.
6. The Decoupling Capacitor should be placed near to IC pin of VINB and AVIN. Separate track is required for AVIN and VINB. The GND terminal of AVIN should be placed close to the GND terminal of IC. (Via holes should be placed near to the GND terminals of IC and Capacitors. The connections to internal ground plane should be strengthened at these points.)
7. Feedback paths (i.e. FBB, FB, FBN, FBP) are very sensitive to noise, thus the track should be as short as possible at these terminals. The Output (Vo) feedback line should be placed away from switching components and tracks. Particularly DRN and FBN of the negative charge pump. Use the FREQ pin to separate these two tracks. Similarly, the FBB and SWB can be separated by the EN1 track. Because EN1, EN2 and FREQ are less susceptible to noise.
8. Place wide and short track to connect Boost Converter Output and OS pin.
9. The two ground planes GND and PGND are intersect at the IC thermal pad only.

■ EXAMPLE OF STANDARD OPERATION CHARACTERISTICS

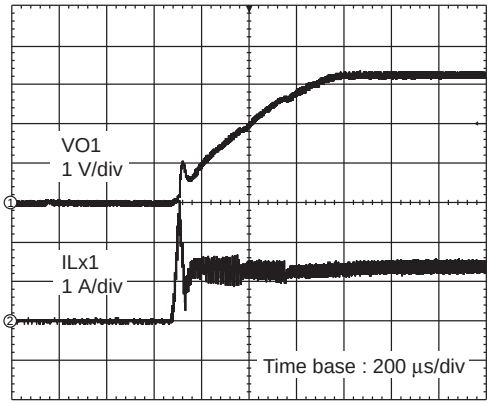
REFERENCE DATA

(1) Buck Converter Characteristic

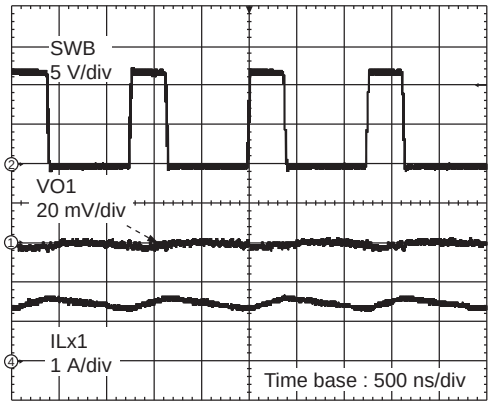
Efficiency vs. Output Current
VIN = 12 V, V_{LOGIC} = 3.3 V, L1 = 10 µH



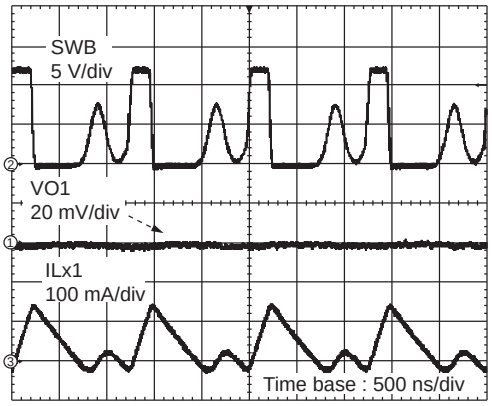
Soft Start
VIN = 12 V, V_{LOGIC} = 3.3 V , I_{LOAD} = 1.2 A



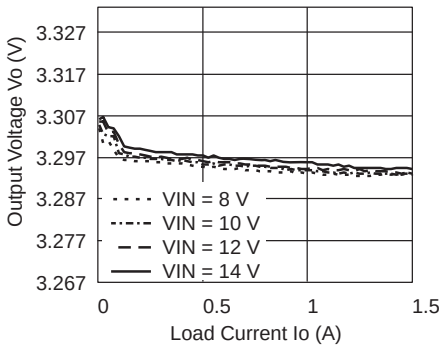
PWM Operation
Continuous Mode
VIN = 12 V, V_{LOGIC} = 3.3 V, I_{LOAD} = 1.5 A



PWM Operation
Discontinuous Mode
VIN = 12 V, V_{LOGIC} = 3.3 V, I_{LOAD} = 45 mA

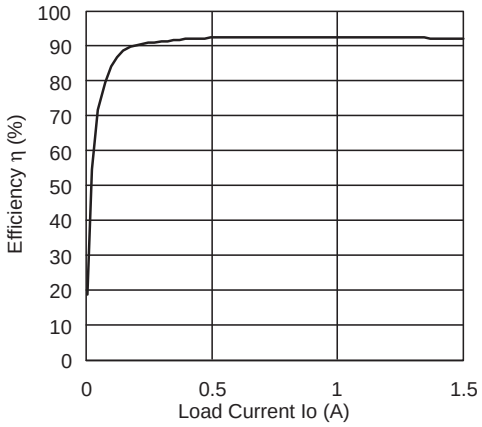


Output Voltage vs. Output Current

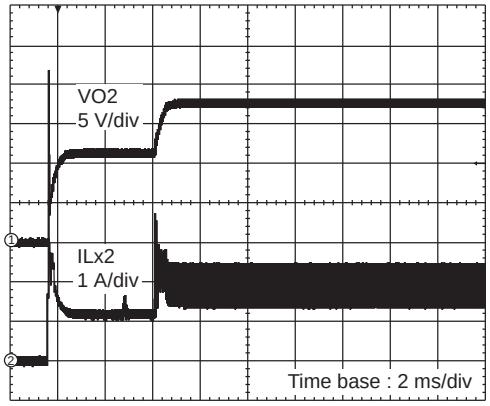


(2) Boost Converter Characteristic

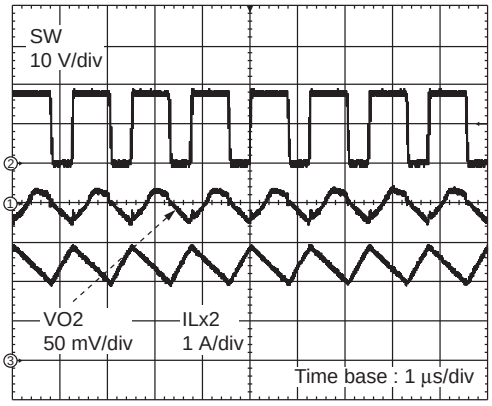
Efficiency vs. Output Current
VIN = 12 V, V_S = 17.7 V, L2 = 6.8 µH



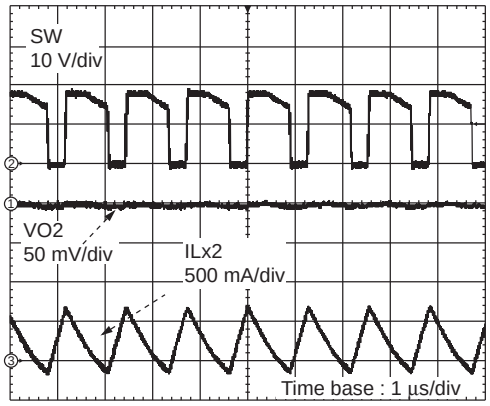
Soft Start
VIN = 12 V, V_S = 17.7 V, I_{LOAD} = 1.2 A, C_{SS} = 22 nF



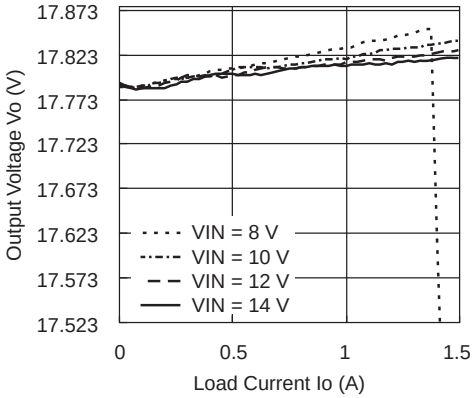
PWM Operation
Continuous Mode
VIN = 12 V, V_S = 17.7 V, I_{LOAD} = 1.5 A



PWM Operation
Discontinuous Mode
VIN = 12 V, V_S = 17.7 V, I_{LOAD} = 10 mA



Output Voltage vs. Output Current

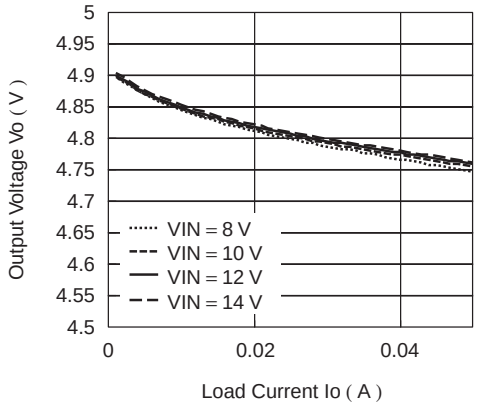


Note : Output current is limited in low input voltage configuration. Refer to "■ APPLICATION MANUAL" for Boost converter design.

(3) Negative Charge Pump Characteristic

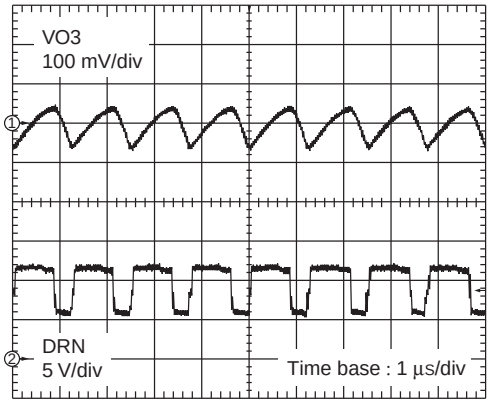
Output Voltage vs. Output Current

V_{GL} = –5 V



Output Ripple Voltage

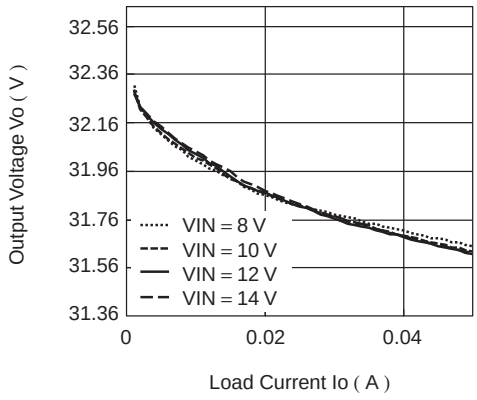
VIN = 12V, V_{GL} = –5V, I_{LOAD} = 50 mA



(4) Positive Charge Pump Characteristic

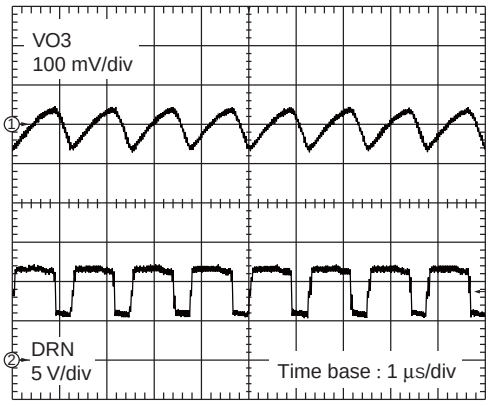
Output Voltage vs. Output Current

V_{SUP} = 17.7 V,
V_{GH} = 32 V, I_{LOAD} = 50 mA



Output Ripple Voltage

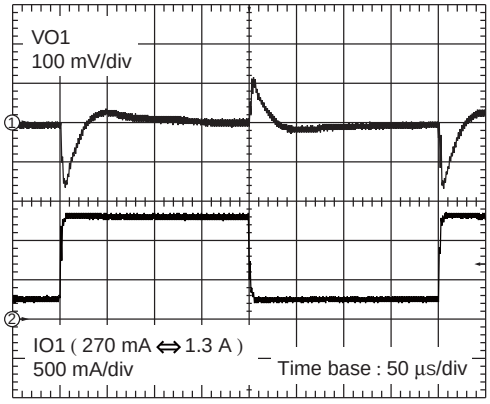
VIN = 12 V, V_{SUP} = 17.7 V,
V_{GH} = 32 V, I_{LOAD} = 50 mA



(5) Converter Load Transient Characteristic

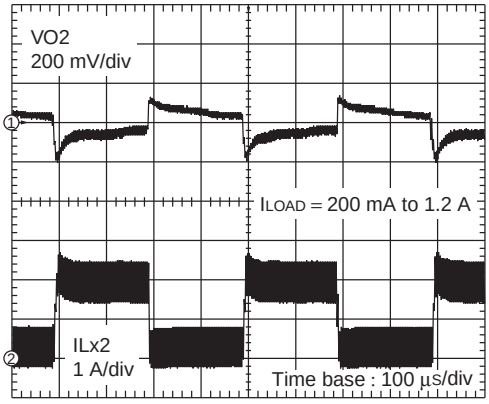
Buck Converter
Load Transient Response

VIN = 12 V, V_{LOGIC} = 3.3 V, Co = 2 x 10 µF,
L1 = 10 µH, FREQ = High



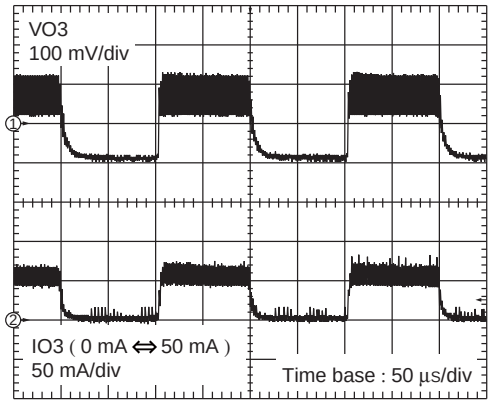
Boost Converter
Load Transient Response

VIN = 12 V, V_S = 17.7 V, Co = 3 x 22 µF,
L2 = 6.8 µH, Ccomp = 22 nF, FREQ = High



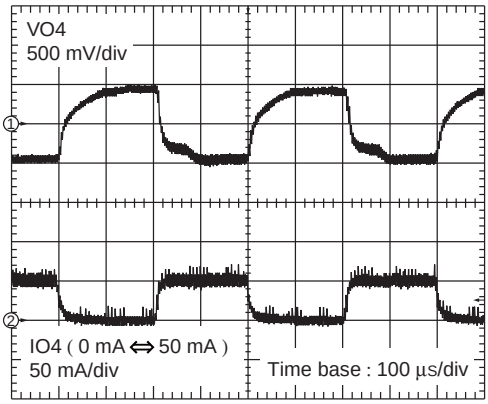
Negative Charge Pump
Load Transient Response

VIN = 12 V, V_{GL} = –5 V, FREQ = High



Positive Charge Pump
Load Transient Response

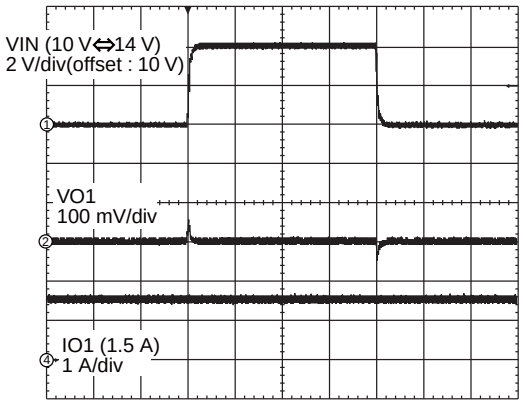
VIN = 12 V, V_{SUP} = 17.7 V,
V_{GH} = 32 V, FREQ = High



(6) Converter Line Transient Characteristic

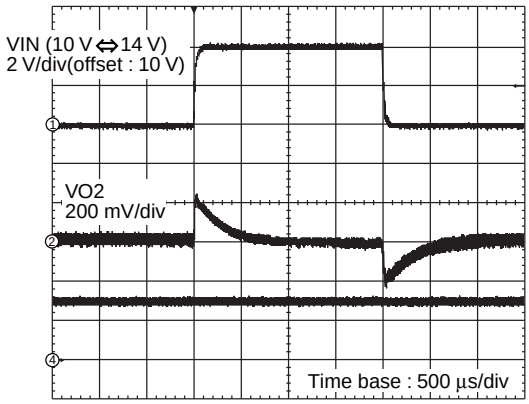
Buck Converter
Line Transient Response

V_{LOGIC} = 3.3 V, I_{LOAD} = 1.5 A, Co = 2 x 10 µF,
L1 = 10 µH, FREQ = High



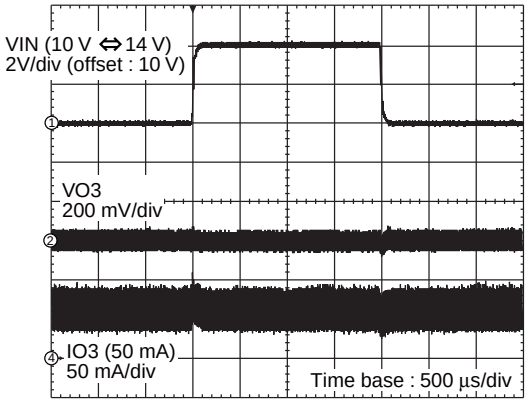
Boost Converter
Line Transient Response

V_S = 17.7 V, I_{LOAD} = 1.5 A, Co = 3 x 22 µF,
L2 = 6.8 µH, Ccomp = 22 nF, FREQ = High



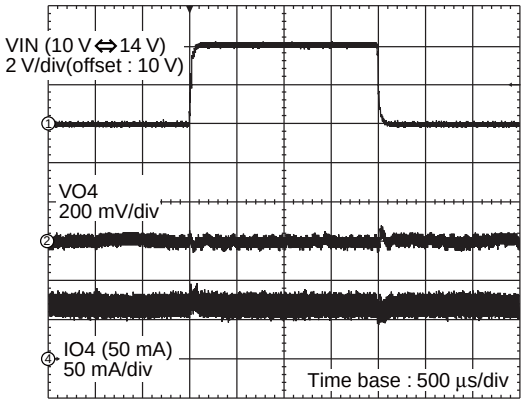
Negative Charge Pump
Line Transient Response

V_{GL} = –5 V, I_{LOAD} = 50 mA, FREQ = High



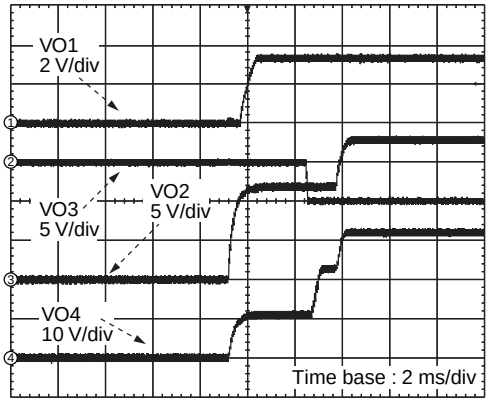
Positive Charge Pump
Line Transient Response

V_{SUP} = 17.7 V, V_{GH} = 32 V
I_{LOAD} = 50 mA, FREQ = High

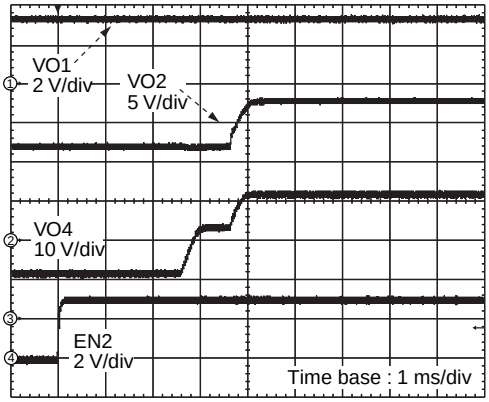


(7) Power-up Sequence

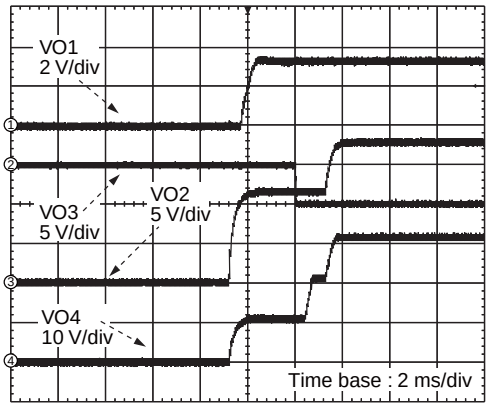
Power-up Sequence
VIN = EN1 = EN2 = 12 V
All channel without load



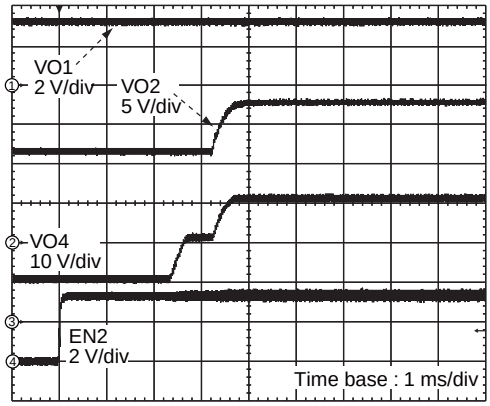
Power-up Sequence
EN2 Enabled Separately
All channel without load



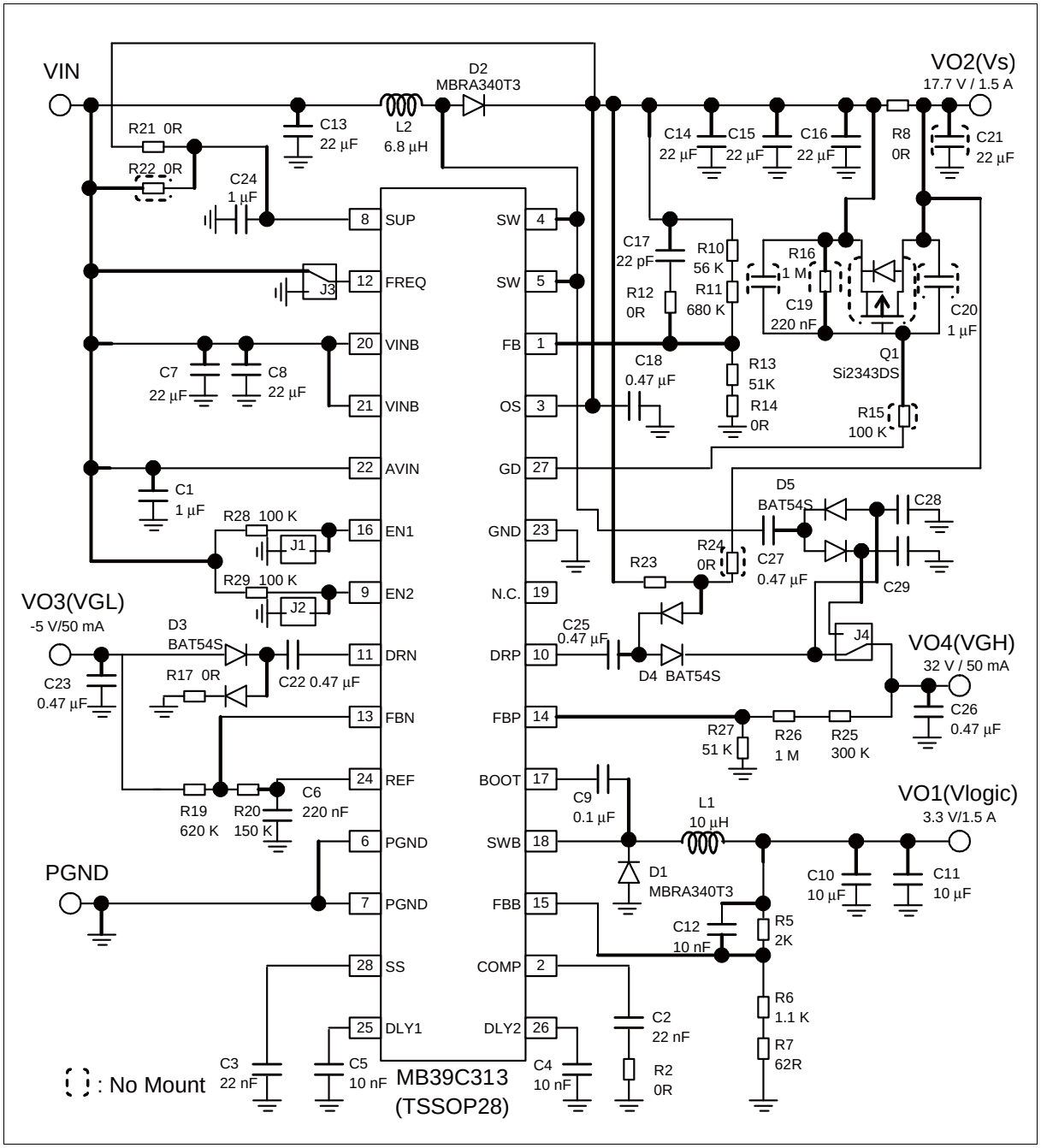
Power-up Sequence
VIN = EN1 = EN2 = 12V
$I_{Load(VLogic)}$ = 1.5 A, $I_{Load(Vs)}$ = 1.5 A
$I_{Load(VGL)}$ = 50 mA, $I_{Load(VGH)}$ = 50 mA



Power-up Sequence
EN2 Enabled Separately
$I_{Load(VLogic)}$ = 1.5 A, $I_{Load(Vs)}$ = 1.5 A
$I_{Load(VGL)}$ = 50 mA, $I_{Load(VGH)}$ = 50 mA



■ TYPICAL APPLICATION CIRCUIT



• **Part List**

Count	Designator	Item Specification	Part Value	Package	Part number	Vendor
1	U1	IC, Bias Power Supply for LCD	MB39C313	TSSOP28P	MB39C313	FML
2	C1, C24	Capacitor, Ceramic, 50 V, X5R, 10%	1 µF	1206	C3216X5R1H105K	TDK
2	C10, C11	Capacitor, Ceramic, 10 V, B, 20%	10 µF	0805	C2012JB1A106K	TDK
6	C7, C8, C13, C14, C15, C16	Capacitor, Ceramic, 25V, B, 20%	22 µF	1210	C3225JB1E226M	TDK
1	C17	Capacitor, Ceramic, 50 V, CH, 5%	22 pF	0603	C1608CH1H220J	TDK
8	C18, C22, C23, C25, C26, C27, C28, C29	Capacitor, Ceramic, 50 V, B, 10%	0.47 µF	1206	C3216JB1H474K	TDK
2	C2, C3	Capacitor, Ceramic, 50 V, B, 10%	22 nF	0603	C1608JB1H223K	TDK
3	C4, C5, C12	Capacitor, Ceramic, 50 V, B, 10%	10 nF	0603	C1608JB1H103K	TDK
1	C6	Capacitor, Ceramic, 25 V, B, 10%	220 nF	0603	C1608JB1E224K	TDK
1	C9	Capacitor, Ceramic, 50 V, B, 10%	0.1 µF	0603	C1608JB1H104K	TDK
2	D1, D2	Diode, Schottky Rectifier, 3 A, 30 V	MBRA340T3	SMA-403D	MBRA340T3	On-Semi
3	D3, D4, D5	Diode, Dual Schottky, 200 mA, 30 V	BAT54S	SOT23	BAT54S	On-Semi
1	L1	Inductor, SMT, 6.5 A, 35 mΩ	10 µH	10x10.2	CDRH104R-100NC	Sumida
1	L2	Inductor, SMT, 4.4 A, 40 mΩ	6.8 µH	7.5x8	PLC-0745-6R8S	NEC
6	R2, R12, R14, R17, R21, R23	Resistor, 1 A, Chip, 0.5%	0R	0603	RK73Z1J	KOA
1	R8	Resistor, 2 A, Chip, 0.5%	0R	0805	RK73Z2J	KOA
1	R10	Resistor, Chip, 1/16 W, 0.5%	56 K	0603	RR0816P-563-D	SSM
1	R11	Resistor, Chip, 1/10 W, 0.5%	680 K	0603	RK73G1JTTD6803D	KOA
2	R13, R27	Resistor, Chip, 1/16 W, 0.5%	51 K	0603	RR0816P-513-D	SSM
1	R19	Resistor, Chip, 1/10 W, 0.5%	620 K	0603	RK73G1JTTD6203D	KOA
1	R20	Resistor, Chip, 1/16 W, 0.5%	150 K	0603	RR0816P-154-D	SSM
1	R26	Resistor, Chip, 1/10 W, 0.5%	1 M	0603	RK73G1JTTD1004D	KOA
2	R28, R29	Resistor, Chip, 1/16 W, 0.5%	100 K	0603	RR0816P-104-D	SSM
1	R5	Resistor, Chip, 1/16W, 0.5%	2 K	0603	RR0816P-202-D	SSM
1	R6	Resistor, Chip, 1/16W, 0.5%	1.1 K	0603	RR0816P-112-D	SSM

(Continued)

(Continued)

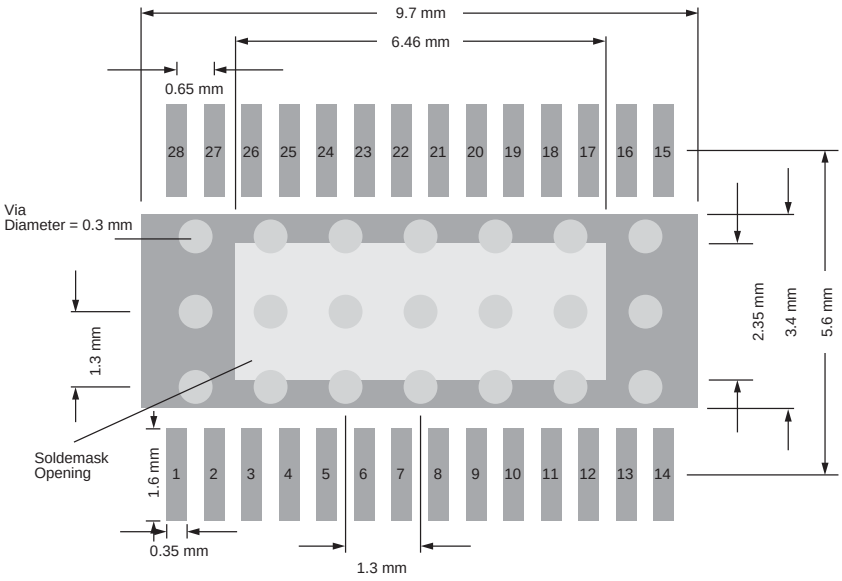
Count	Designator	Item Specification	Part Value	Package	Part number	Vendor
1	R7	Resistor, Chip, 1/16W, 0.5%	62R	0603	RR0816Q-620-D	SSM
2	J1, J2	Jumper	—	HDR1X2	—	—
2	J3, J4	Jumper	—	HDR1X3	—	—
No Mount	C19	—	220 nF	0603	—	—
No Mount	C20	—	1 µF	1206	—	—
No Mount	C21	—	22 µF/25 V	1210	—	—
No Mount	Q1	P-ch MOSFET	SI2343DS	SOT23	Si2343DS	Vishay
No Mount	R15	—	100 K	0603	—	—
No Mount	R16	—	1 M	0603	—	—
No Mount	R22	—	0R	0603	—	—
No Mount	R24	—	0R	0603	—	—

FML : FUJITSU MICROELECTRONICS LIMITED
TDK : TDK Corporation
OnSemi : ON Semiconductor Corporation
Sumida : Sumida Corporation
NEC : NEC Electronics Corporation
KOA : KOA Corporation
SSM : SUSUMU Co. Ltd.
Vishay : Vishay Intertechnology, Inc.

■ LAND PATTERN

The MB39C313 has an exposed thermal pad zone on the bottom side of the IC. This area has to be soldered onto the PCB board to enhance heat dissipation.
The via should be placed in the thermal pad. These via assist heat dissipation towards the bottom layer of the PCB. Via and copper pad size may be adjusted according to PCB constraints.

- Land pattern design example



■ USAGE PRECAUTIONS

1. Never use setting exceeding maximum rated conditions.

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Use the devices within recommended conditions

It is recommended that devices be operated within recommended conditions.
Exceeding the recommended operating condition may adversely affect devices reliability.
Nominal electrical characteristics are warranted within the range of recommended operating conditions otherwise specified on each parameter in the section of electrical characteristics.

3. Design the ground line on printed circuit boards with consideration of common impedance.

4. Take appropriate static electricity measures.

Containers for semiconductor materials should have anti-static protection or be made of conductive material.
After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
Work platforms, tools, and instruments should be properly grounded.
Working personnel should be grounded with resistance of 250 kΩ to 1 MΩ between body and ground.

5. Do not apply negative voltages

The use of negative voltages below -0.3 V may activate parasitic transistors on the device, which can cause abnormal operation.

■ ORDERING INFORMATION

Part number	Package	Remarks
MB39C313PFTH	28-pin plastic TSSOP FPT-28P-M20	Exposed PAD

■ EV BOARD ORDERING INFORMATION

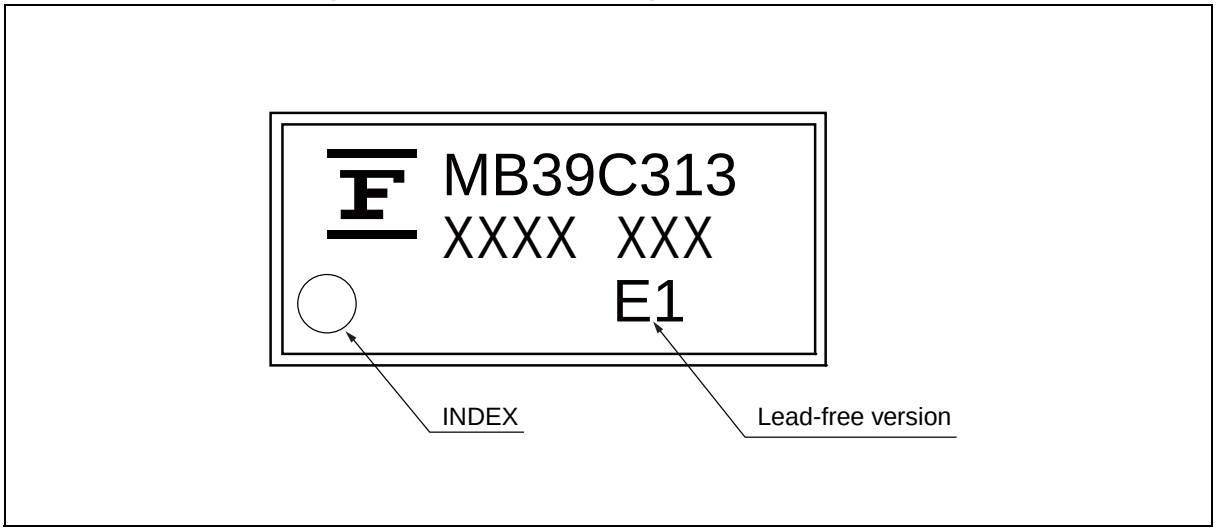
EV Board Part No.	EV Board version No.	Remarks
MB39C313EVB-01	MB39C313EVB-01 Rev.1.2	TSSOP-28

■ RoHS COMPLIANCE INFORMATION OF LEAD (Pb) FREE VERSION

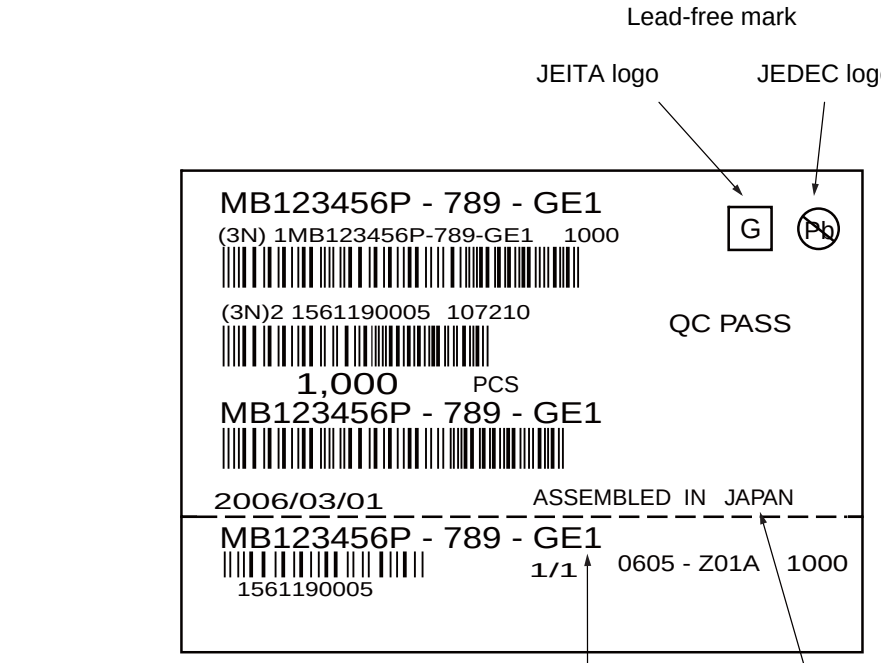
The LSI products of FUJITSU MICROELECTRONICS with “E1” are compliant with RoHS Directive, and has observed the standard of lead, cadmium, mercury, hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenylethers (PBDE).

A product whose part number has trailing characters “E1” is RoHS compliant.

■ MARKING FORMAT (LEAD FREE VERSION)



■ LABELING SAMPLE (LEAD FREE VERSION)



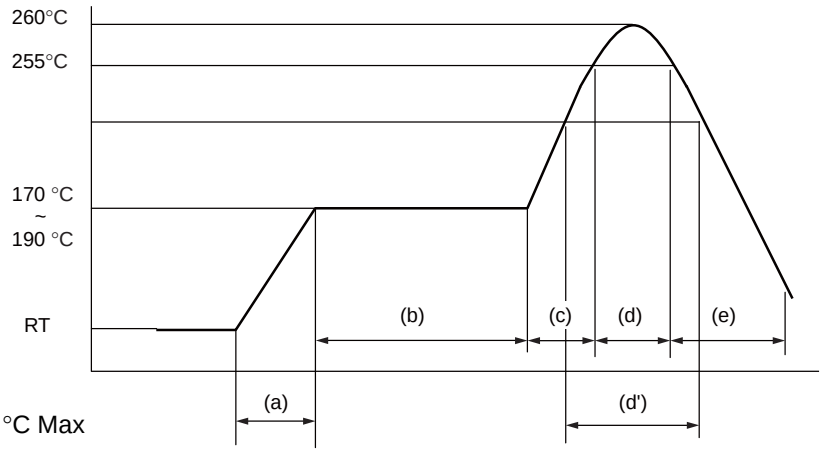
■ MB39C313PFTH RECOMMENDED CONDITIONS OF MOISTURE SENSITIVITY LEVEL

[FUJITSU MICROELECTRONICS Recommended Mounting Conditions]

Item	Condition	
Mounting Method	IR (infrared reflow), warm air reflow	
Mounting times	2 times	
Storage period	Before opening	Please use it within two years after manufacture.
	From opening to the 2nd reflow	Less than 8 days
	When the storage period after opening was exceeded	Please process within 8 days after baking (125 °C ± 3 °C, 24hrs + 2H/-0H) Baking can be performed up to two times.
Storage conditions	5 °C to 30 °C, 70%RH or less (the lowest possible humidity)	

[Parameters for Each Mounting Method]

IR (infrared reflow)



H rank : 260 °C Max

(a) Temperature Increase gradient : Average 1 °C/s to 4 °C/s
(b) Preliminary heating : Temperature 170 °C to 190 °C, 60s to 180s
(c) Temperature Increase gradient : Average 1 °C/s to 4 °C/s
(d) Actual heating : Temperature 260 °C Max; 255 °C or more, 10s or less
(d') : Temperature 230 °C or more, 40s or less
or
Temperature 225 °C or more, 60s or less
or
Temperature 220 °C or more, 80s or less
(e) Cooling : Natural cooling or forced cooling

Note : Temperature : the top of the package body

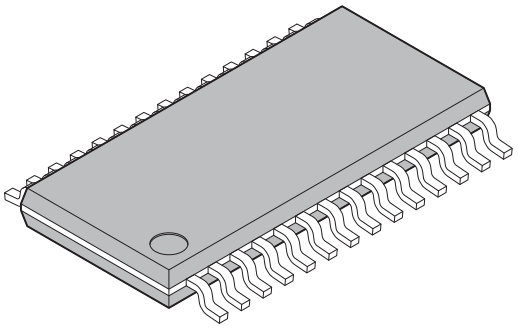
Manual soldering (partial heating method)

Item	Condition	
Storage period	Before opening	Within two years after manufacture.
	Between opening and mounting	Within two years after manufacture. (No need to control moisture during the storage period because of the partial heating method.)
Storage conditions	5 °C to 30 °C, 70%RH or less (the lowest possible humidity)	
Mounting conditions	Temperature at the tip of a soldering iron: 400 °C max Time: Five seconds or below per pin*	

* : Make sure that the tip of a soldering iron does not come in contact with the package body.

■ PACKAGE DIMENSIONS

28-pin plastic TSSOP

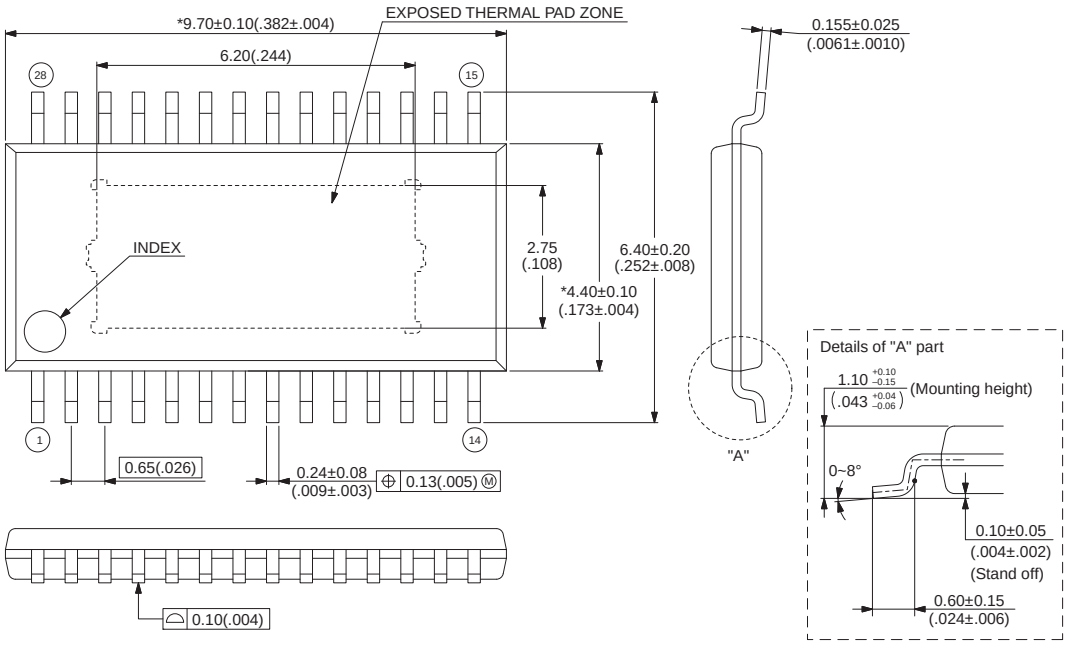


(FPT-28P-M20)

Lead pitch	0.65 mm
Package width × package length	4.40 mm × 9.70 mm
Lead shape	Gullwing
Sealing method	Plastic mold
Mounting height	1.20 mm Max
Weight	0.12 g

28-pin plastic TSSOP
(FPT-28P-M20)

Note 1) Pins width and pins thickness include plating thickness.
Note 2) Pins width do not include tie bar cutting remainder.
Note 3) * : These dimensions do not include resin protrusion.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

■ CONTENTS

MEMO

MEMO

MEMO

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