FUJITSU

HIGH-SPEED CMOS SINGLE CHIP 4-BIT MICROCOMPUTER

T-49-19-44

MB88500H SERIES

TM347-A871: January 1987

HIGH-SPEED CMOS SINGLE-CHIP 4-BIT MICROCOMPUTER

The Fujitsu MB88500H series CMOS single-chip 4-bit microcomputer family is a high-speed version of the conventional MB88500 series. Its architecture and instruction set are same as the MB88500 series, but its minimum instruction execution time is reduced to 1.5 µs min. using an 8 MHz crystal or external clock with a prescaler. (at 4 MHz without prescaler)

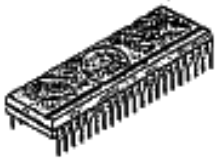
The MB88500H series consists of the MB88501H, MB88503H, and MB88505H. Further all devices have a wide voltage version (3.5V to 6.0V: A-version). The MB88501H and MB88505H contain a 4K by 8-bit mask ROM (program memory) whereas MB88503H contains a 2K by 8-bit mask ROM. Besides the on-chip 256 by 4-bit static RAM (data memory), each devices have 36 I/O lines (including a serial port), an 8-bit timer/counter, and a clock generator.

They are fabricated by the silicon-gate CMOS process, the MB88500H series is packaged in a 42-pin plastic standard, shrink DIP, 48-pin plastic flat package. They operate with a single +5 V power supply and a 4 MHz clock without a prescaler (or 8 MHz clock with prescaler) over the temperature range of -40 °C to +85 °C. (-30 °C to +70 °C for a A-version)

CMOS technology allows the device to operate with low power dissipation (12 mA max. at 2 MHz), and further the standby function enables data retention with lower current (10 µA max. at V_{CC} = 6 V).

For user's development of the MB88500H series based system, Fujitsu provides the MB88400/500 cross-assembler and host-emulator which run on the CP/M-86 or PC-DOS machines (cross-assembler also run on the Intellec series III MDS), and the MB2115 series evaluation board system, and the MB88508H piggyback EPROM evaluation devices which have external 4K/8K x 8-bit EPROM (MBM27C32A or MBM27C64). These development tools enables users to minimize their development time and cost.

MB88501H-P/503H-P/505H-P



42-PIN PLASTIC STANDARD DIP
(DIP-42P-M01)

MB88501H-PSH/503H-PSH/505H-PSH

42-PIN PLASTIC SHRINK DIP
(DIP-42P-M02)

MB88501H-PF/503H-PF/505H-PF

48-PIN PLASTIC FLAT PACK
(FPT-48P-M02)

MB88508H-C/508U-C

42-PIN CERAMIC MODULE
(MDP-42C-P04)

MB88508H-CF/508U-CF

48-PIN CERAMIC MODULE
(MQP-48C-P01)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

FEATURES

- CMOS Single-chip 4-bit Microcomputer

- Program Memory:
  - o MB88501H, MB88505H: 4 K x 8-bit mask ROM
  - o MB88503H : 2 K x 8-bit mask ROM

- Data Memory:
  - o 256 x 4-bit static RAM

- 36 I/O Lines:
  - o K-Port: 4-bit parallel input only
  - o P-Port: 4-bit parallel output only
  - o O-Port: 8-bit parallel output only
  - o R-Port: Four 4-bit parallel or 16 individual input/output
  - o C-Port: Serial I/O, external interrupt input, timer/counter input, and timing output

- Five Selectable Output Port Types for O-, P-, and R-Ports with Mask Option
  - o Standard open-drain
  - o Standard pullup
  - o High-current open-drain
  - o High-current pullup
  - o 12V-interface open-drain (P-Port only)

- On-chip Mask Programmable PLA (Programmable Logic Array) for Data Conversion at O-Port (MB88501H, MB88503H)

- 8-bit Programmable Timer/Counter with Two Clock Modes:
  - o Internal clock (Timer)
  - o External clock (Counter)

- Serial I/O with Serial Buffer:
  - o MB88501H, MB88503H: 4-bit
  - o MB88505H : Software selectable 4-/8-bit

- Three Programmable Clock Modes:
  - o Internal clock
  - o External clock
  - o Software clock

- On-chip Clock Generator with 2 Mask Options:
  - o External crystal/ceramic resonator or external clock drive
  - o External RC-network or external clock drive

- Mask-option Divide-by-two Clock Prescaler for Expanding Clock Range

- Single Level Four Prior Source Maskable Interrupt:
  - o External
  - o Clock
  - o Timer/counter overflow
  - o Serial buffer full/empty

- 8-nesting Levels for Subroutine Calls

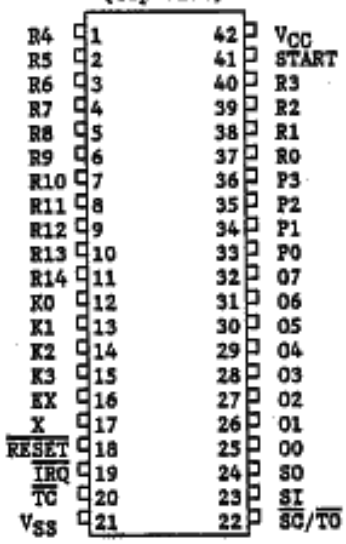
FEATURES (Continued)

- Instruction Set: Upward compatible the MB88500 series instruction set
  - Number of instructions : 76
  - Instruction length/cycle: 1 byte/1 cycle (82%), 2 bytes/2 cycles (17%), 2 byte/3 cycle (1%)
  - Execution time : 1.5 µs min. using 8 MHz clock with prescaler
- On-chip Power-on Reset Circuit
- Mask-option Standby Function:
  - No standby function
  - Software-initiation standby function
- Two mask-option Output States During Standby:
  - Hold
  - High impedance
- Two Software Selectable Oscillator States During Standby:
  - Idle
  - Stop
- Mask-option Standby-off Reset
- Mask-option Watch-dog Timer Function
- Low Power Dissipation:
  - 12 mA at V_{CC} = 5.5 V at fc = 2 MHz max. (Active mode)
  - 10 µA at V_{CC} = 6.0 V at fc = 0 MHz max. (Standby mode)
- Single Power Supply:
  - Standard version: 4.5 V to 5.5 V (Active mode)
    3.5 V to 6.0 V (Standby mode)
  - A-version : 3.5 V to 6.0 V (Active mode)
    3.5 V to 6.0 V (Standby mode)
- Wide Operation Temperature Range:
  - Standard version: T_A= -40 °C to +85 °C
  - A-version : T_A= -30 °C to +70 °C
- Silicon Gate CMOS Technology
- Three Package Types:
  - 42-pin plastic standard DIP: Suffix -P
  - 42-pin plastic shrink DIP: Suffix -PSH
  - 48-pin plastic flat package: Suffix -PF
- Powerful Development Support:
  - CP/M-86, PC-DOS, or Intellec series III MDS cross-assembler (SM07415-A012/SMXXXXX-A010/SM05215-A010)
  - CP/M-86 or PC-DOS host emulator software for monitoring evaluation board and symbolic debugging (SM07415-G022/SMXXXXX-G020)
  - MB2115 series evaluation board (-01, -02, -04 and, -31A) for software debugging
  - MB88508H CMOS piggyback EPROM evaluation devices

T-49-19-44

Fig. 1: PIN ASSIGNMENT

Suffix -P and -PSH
(Top view)



Suffix -PF
(Top View)

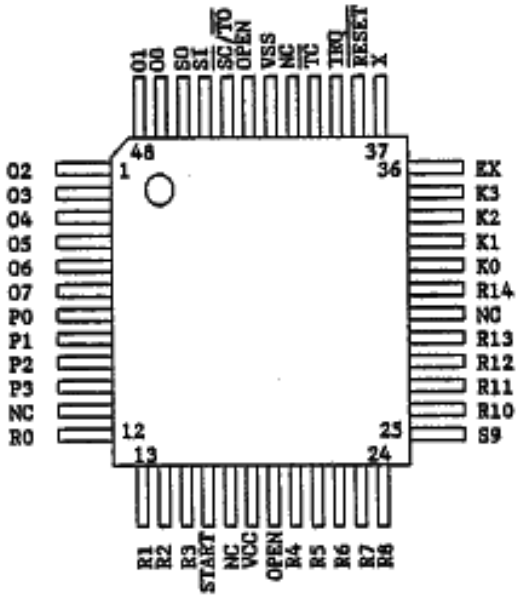
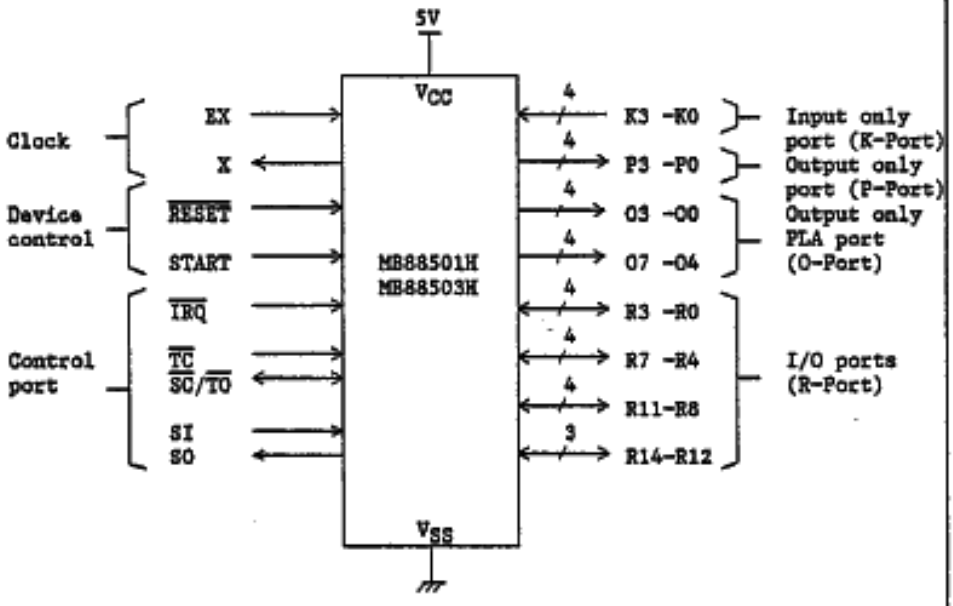


Fig. 2: MB88501H AND MB88503H LOGIC SYMBOL



2

Fig. 3: MB88501H AND MB8503H BLOCK DIAGRAM

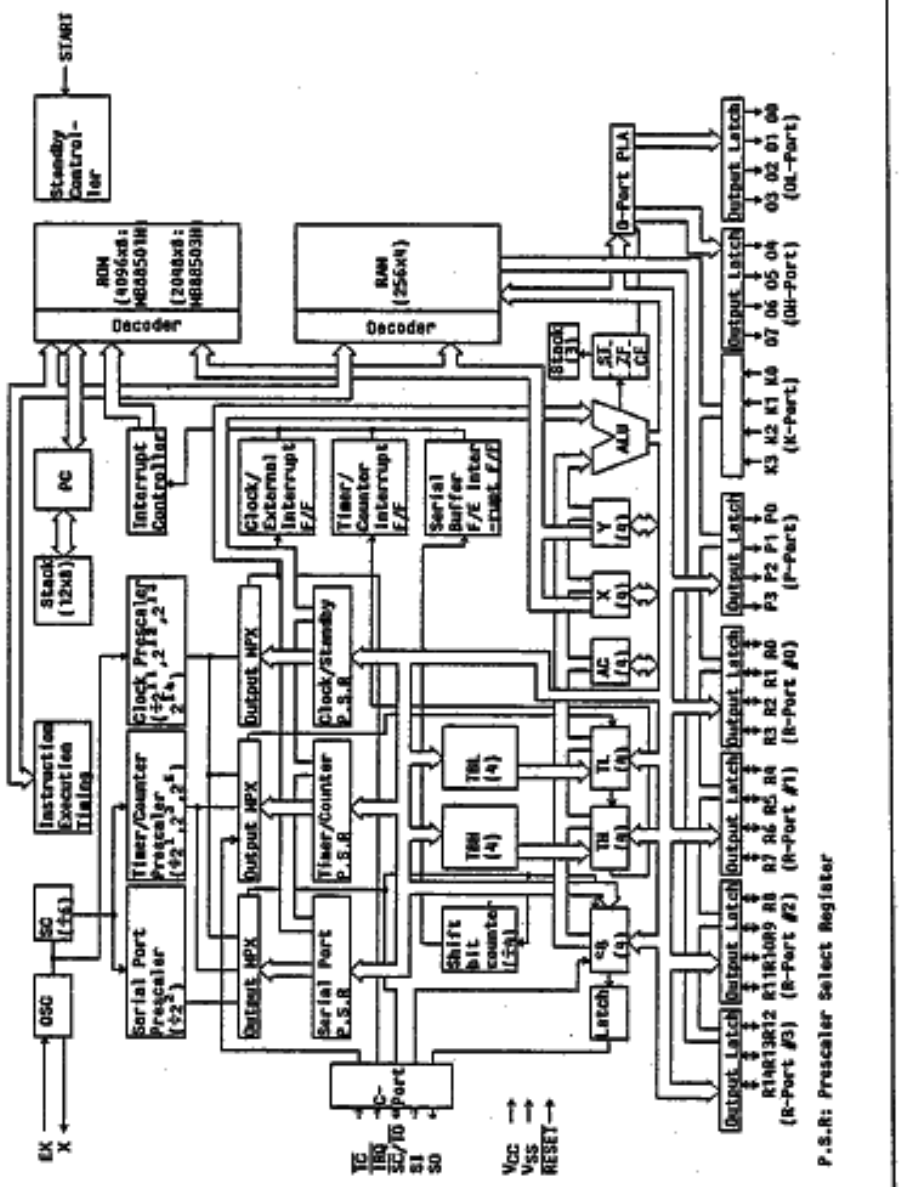


Fig. 4: MB88505H LOGIC SYMBOL

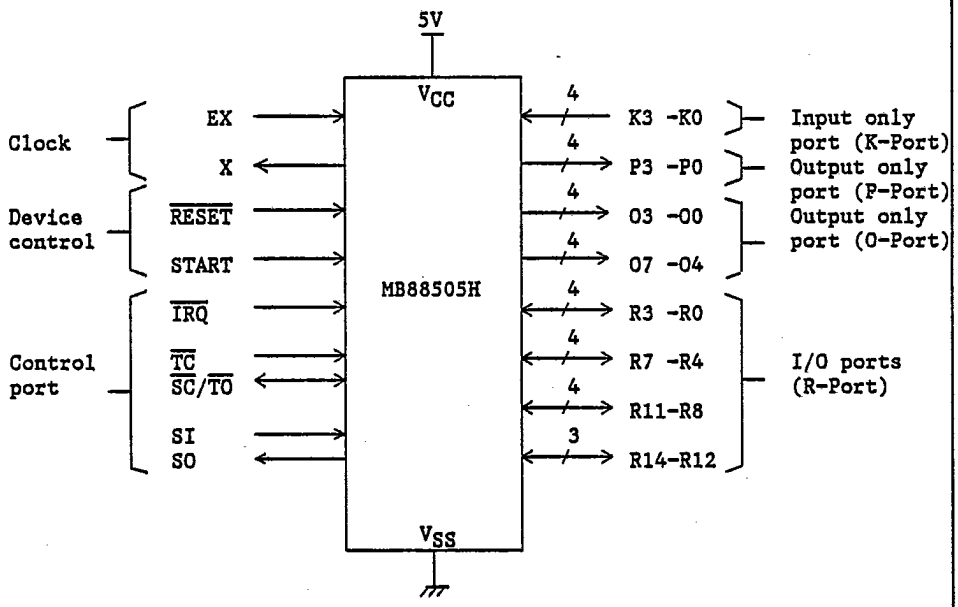
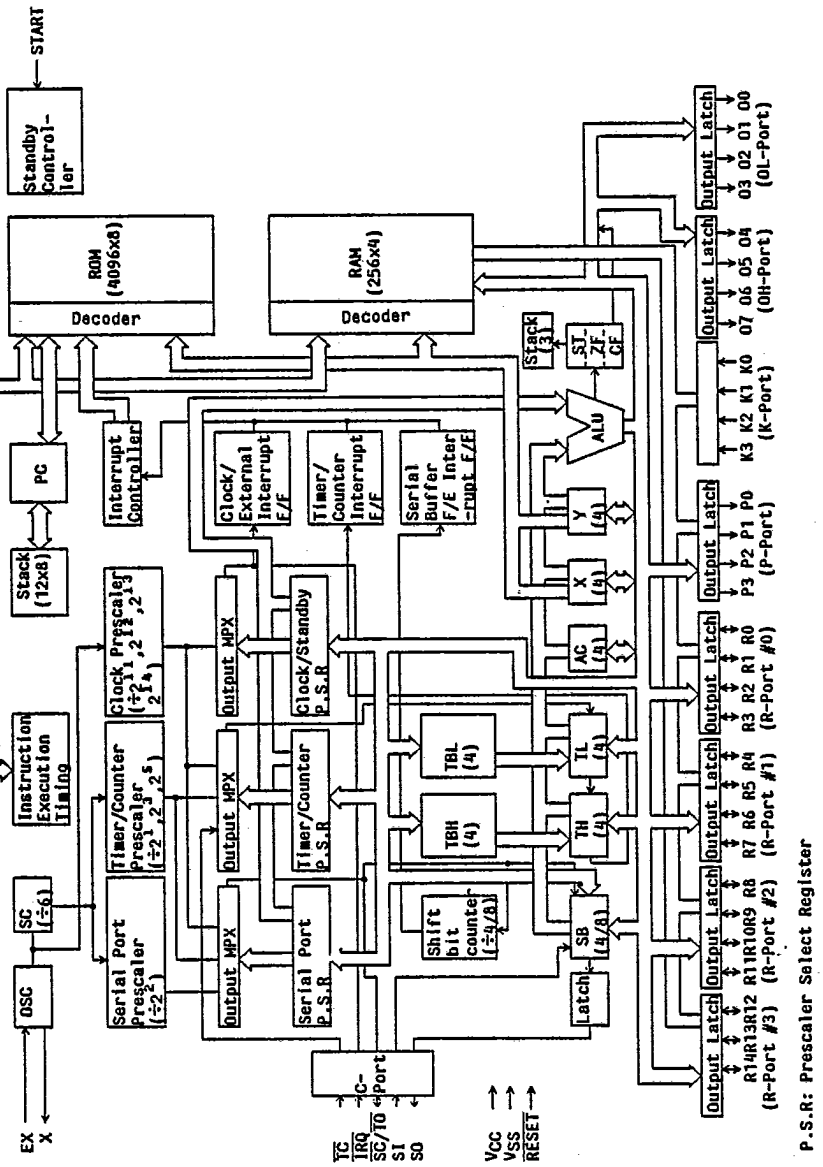


Fig. 5: MB88505H BLOCK DIAGRAM



PIN DESCRIPTION

Fig. 1 and Table 1 show the pin assignment and pin description of the MB88500 series.

Table 1: PIN DESCRIPTION

Symbol	Pin No.	Type	Name & Function
• Power Supply			
V_{CC}	42 (18)	–	+5V DC power supply pin.
V_{SS}	21 (42)	–	Ground pin.
• Clock			
EX	16 (36)	I	**Oscillator Input:** Input to the inverting amplifier that forms the on-chip oscillator. An external crystal/ ceramic resonator or RC-network is connected between the EX and X pins. Either of these two oscillation types can be selected using mask option. When an external oscillator is used, the EX pin receives the external oscillator signal. This pin is a non-hysteresis input when the crystal/ ceramic oscillator is selected, and a hysteresis input when the RC-network oscillator is selected.
X	17 (37)	O	**Oscillator Output:** Output of the inverting amplifier that forms the on-chip oscillator, and input to the internal clock generator. An external crystal/ceramic resonator or RC-network is connected between the EX and X pins. Either of these two oscillator types can be selected using mask option. When an external oscillator is used, the X pin should be left open.
• Device Control			
$\overline{RESET}$	18 (38)	I	**Reset:** This pin function as an external reset input or power-on reset output. External reset input: A reset input to the internal reset circuit. A low level on the $\overline{RESET}$ pin forcedely stops the MCU's operation, and initializes its internal state. After the $\overline{RESET}$ pin returns high, the MCU restarts execution of program from address #0. The $\overline{RESET}$ pulse must be low for at least two instruction cycles while the oscillator is stably running after power-on. This pin is a hysteresis input with an internal pullup resistor. An external capacitor from the $\overline{RESET}$ pin to the VSS pin (and the internal pull-up resistor), whose time constant should be greater than the reset time required (12 clock periods) composes the external reset circuit.

2

T-49-19-44

Table 1: PIN DESCRIPTION (Continued)

Symbol	Pin No.	Type	Name & Function
• Device Control (Continued)			
$\overline{\text{RESET}}$	18 (38)	I/O	Power on reset output: A reset output from the on-chip reset control circuit. Normally this output is high during the active operation except the reset mode. The rising of the VCC voltage after power on outputs a low level on the $\overline{\text{RESET}}$ pin, and them automatically returns high 2^{18} clock periods after the oscillator starts by power on. This pin is a hysteresis input with an internal pullup resistor.
START	41 (16)	I	Start: A standby release input to the internal standby control and status registers that control and monitor the on-chip standby control circuit. A high level on the START pin during the standby mode sets the standby release flag (STF) in the standby status register, resets the standby enable flag (STBE) in the standby control register, and triggers the standby release sequence to return the MCU to the active mode. Before the START pulse is applied, the VCC voltage must return to the active operation range when the battery backup is used. Also, the START pin must be low before the standby mode is initiated. The START pin state (logical level) is reflected in the standby release input (START) flag (STIF) in the standby status register, regardless of during the standby mode or active mode, and besides even when the standby function is not implemented using mask option. Therefore, the START pin state can be sensed by reading the standby status register using IN instruction (with Y=8). This pin is a hysteresis input with an internal pulldown resistor.
• C-Port			
$\overline{\text{IRQ}}$	19 (39)	I	Interrupt Request: A maskable external interrupt input to the on-chip interrupt control circuit. The falling edge of the $\overline{\text{IRQ}}$ pulse sets the external interrupt request flag (IRF) in the interrupt flag register regardless of enabling or disabling the external interrupt. If the external interrupt is enabled in advance by EN instruction, the interrupt sequence starts at once. Otherwise, the IRF flag is internally held as an interrupt source. Also, the $\overline{\text{IRQ}}$ pin state (logical level), which is reflected in the external interrupt input flag (IF) regardless of enabling or disabling the external interrupt, is testable using TSTI instruction. (When $\overline{\text{IRQ}}$ = L, IF = 1; otherwise IF = 0.) This pin is a hysteresis input with an internal pullup resistor.

Table 1: PIN DESCRIPTION (Continued)

Symbol	Pin No.	Type	Name & Function
• C-Port (Continued)			
$\overline{TC}$	20 (40)	I	Timer/Counter: An external count clock input to the on-chip 8-bit timer/counter. The falling edge of the $\overline{TC}$ pulse increments the timer/counter by one bit, when the external count clock (counter) mode is enabled by EN instruction programming the timer/counter prescaler select register using OUT instruction (with Y = B). Also, the TC pin state (logical level), which is reflected in the timer/counter input flag (TCIF) in the timer/counter prescaler select register regardless of enabling or disabling the external count clock (counter mode, is testable by reading the prescaler select register using IN instruction (with Y = B). (When $\overline{TC}$ = L, TCIF = 1; otherwise TCIF = 0.) This pin is inactive as a count clock input when the external count clock mode is not selected or the timer/counter is disabled by DIS instruction or reset. This pin is a hysteresis input with an internal pullup resistor.
$\overline{SC}/\overline{TO}$	22 (44)	I/O	Shift Clock/Timing Output: One of the shift clock input ($\overline{SC}$), shift clock output ($\overline{SC}$), or synchronous timing output ($\overline{TO}$) is enabled using EN instruction.
		I	$\overline{SC}$: 1) Shift clock input to the on-chip serial port: When the external shift clock mode is enabled for the serial port, the falling edge of the external $\overline{SC}$ clock shifts the contents of the internal serial buffer one bit right (from MSB to LSB). This input is inactive when the external clock mode is not selected or the serial port disabled by DIS instruction or reset. This pin is a hysteresis input. 2) Shift clock output from the on-chip serial port: When the internal shift clock mode is enabled, the internal shift clock shifts the contents of the serial buffer one bit right. In this mode, the internal timing signal selected is output onto the $\overline{SC}$ pin for synchronization.
		O	$\overline{TO}$: Synchronous timing output: When the timing output is enabled, the internal timing signal (which is generated by the on-chip state counter outputs, $\phi 1$ and $\phi 2$) is output onto the $\overline{TO}$ pin. By DIS instruction or reset, the $\overline{TO}$ pin is disabled and stops issuing the timing output. This pin is a hysteresis input with an internal pullup resistor

2

Table 1: PIN DESCRIPTION (Continued)

Symbol	Pin No.	Type	Name & Function
• C-Port (Continued)			
SI	23 (45)	I	**Serial Data Input:** Data input to the on-chip serial port. The rising edge of the external ($\overline{SC}$) or internal shifts the data bit on the SI pin into the MSB of the serial buffer register when the serial port is enabled by EN instruction. Also, the SI pin state (logical level) is reflected in the serial data input flag (SIF) in the serial port prescaler select register regardless of enabling or disabling the serial port. Therefore, the SI pin can be sensed by reading the prescaler register using IN instruction (with Y = A).
SO	24 (46)	O	**Serial Data Output:** Data output with latch of the on-chip serial port. The falling edge of the external ($\overline{SC}$) or internal shift clock shifts the LSB data of the serial buffer register to the serial port output latch, regardless of enabling or disabling to serial port. The content of the output latch directly appears on the SO pin. This pin is a CMOS pullup output, and is set high by reset.
• I/O Ports			
K3-K0	15-12 (35-32)	I	**K-Port:** A 4-bit parallel non-latched input only port. K0 is LSB. 4-bit data on K-Port is input into the accumulator by INK instruction. These pins are internally pullup.
P3-P0	36-33 (10- 7)	O	**P-Port:** A 4-bit parallel latched output only port. P0 is LSB. 4-bit data in the accumulator is output to P-Port by OUTP instruction. Refer to Table 5 User mask options for available making option.
O3-O0, O7-O0	28-25 (2,1,48, 47) 32-39 (6-3)	O	**O-Port:** An 8-bit parallel latched output only port with the on-chip mask programmable PLA (Programmable Logic Array) for output data conversion. Depending on user's PLA pattern, this port functions as a dual 4-bit parallel output or an 8-bit parallel PLA output. Dual 4-bit parallel output: By OUTO instruction, 4-bit data in the accumulator is output, without conversion, onto the lower nibble (O3-O0) or upper nibble (O7-O4) of O-Port, depending on whether the carry flag (CF) is "0" or "1".

Table 1: PIN DESCRIPTION (Continued)

Symbol	Pin No.	Type	Name & Function
• I/O Port (Continued)			
O3-O0, O7-O4	28-25, (2,1,48, 47) 32-29 (6-3)	O	8-bit parallel PLA output(MB88501H, MB88503H): By OUTO instruction, 4-bit data in the accumulator and the carry flag (CF) bit are converted into 8-bit data through the PLA array, and the 8-bit data is output to O-Port. Depending on user's PLA pattern, 32 kinds of 8-bit data conversions are possible. For example, it can be encoded into 8-segment data for LED display. Refer to Table 5 User mask options for available making option.
R3 -R0, R7 -R4, R11-R8, R14-R12	40-37, (15-12) 4- 1, (23-20) 8- 5, (27-24) 11- 9 (31,29, 28)	I/O	R-Port: This port functions as three 4-bit parallel input and one 3-bit parallel input (non-latched)/output (latched) ports, or 15 individual input (non-latched)/ output (latched) lines, depending on instructions. Parallel I/O: Each 4-bit and 3-bit port is named R-Port #0 (R3-R0), R-Port #1 (R7-R4), R-Port #2 (R11-R8), and R-Port #3 (R14-R12), and is indirectly addressed by the Y-register (Port #). 4-bit data in the accumulator is output to an addressed port of R-Ports #0 to #3 by OUT instruction. 4-bit data on the addressed port is input into the accumulator by IN instruction. (Before IN instruction, the port to be addressed must be set up to "1" state (input) mode).) Individual I/O: Each line from R14 to R0 is indirectly addressed by the Y-register (Bit #). The addressed line is individually set/reset by SETR/RSTR instruction, and especially each line of R-Port #0 (R3-R0) is directly set/reset by SETD/RSTD instruction. The addressed line is individually testable by TSTR instruction, and each line of R-Port #2 (R11-R8) is directly testable in particular by TSTD instruction. (Before the TSTR and TSTD instructions, the line to be addressed must be set up to "1" (input mode).) Refer to Table 5 User mask options for available making option.

Note: Parenthesis number is applied to suffix -PF

DIFFERENCES BETWEEN MB88500 SERIES AND MB88500H SERIES

Table 2: DIFFERENCES BETWEEN MB88501 AND MB88501H/MB88503H

Device / Item	MB88501	MB88501H	MB88503H
ROM size	· 4K x 8 bits	· 4K x 8 bits	· 2K x 8 bits
RAM size	· 192 x 4 bits	· 256 x 4 bits	· 256 x 4 bits
Oscillator Type	· Crystal/Ceramic OSC or external clock drive · RC-network OSC or external clock drive (Mask option)	· Crystal/Ceramic OSC or external clock drive · RC-network OSC or external clock drive (Mask option)	· Crystal/Ceramic OSC or external clock drive · RC-network OSC or external clock drive (Mask option)
Minimum Instruction Execution Time	· 2.86 µs use 4.19 MHz with prescaler	· 1.5 µs use 8.0 MHz with prescaler	· 1.5 µs use 8.0 MHz with prescaler
PLA	· No · Yes (Mask option)	· No · Yes (Mask option)	· No · Yes (Mask option)
Serial Buffer	· 4 bit	· 4 bit	· 4 bit
Low-voltage Reset Function	· No · Yes (-10°C to +70°C) (Mask option:STD version)	· No	· No
Instruction No.	75	76 (Reset instruction)	76 (Reset instruction)
Members	· MB88501-P/-PSH/-PF A-version are available for each part above.	· MB88501H-P/-PSH/-PF A-version are available for each part above.	· MB88503H-P/-PSH/-PF A-version are available for each part above.

Table 3: DIFFERENCES BETWEEN MB88505/MB88507 AND MB88505H

Item \ Device	MB88505	MB88507	MB88505H
ROM size	· 4K x 8 bits	· 2K x 8 bits	· 4K x 8 bits
RAM size	· 256 x 4 bits	· 256 x 4 bits	· 256 x 4 bits
Oscillator Type	· Crystal/Ceramic OSC or external clock drive · RC-network OSC or external clock drive (Mask option)	· Crystal/Ceramic OSC or external clock drive · RC-network OSC or external clock drive (Mask option)	· Crystal/Ceramic OSC or external clock drive · RC-network OSC or external clock drive (Mask option)
Minimum Instruction Execution Time	· 2.0 µs use 6.0 MHz with prescaler	· 1.5 µs use 8.0 MHz with prescaler	· 1.5 µs use 8.0 MHz with prescaler
PLA	· No	· No	· No
Serial Buffer	· 4 bit · 8 bit (Software selectable)	· 4 bit · 8 bit (Software selectable)	· 4 bit · 8 bit (Software selectable)
Low-voltage Reset Function	· No	· No	· No
Instruction No.	75	75	76 (Reset instruction)
Members	· MB88505-P/-PSH/-PF A-version are available for each part above.	· MB88507-P/-PSH/-PF A-version are available for each part above.	· MB88505H-P/-PSH/-PF A-version are available for each part above.

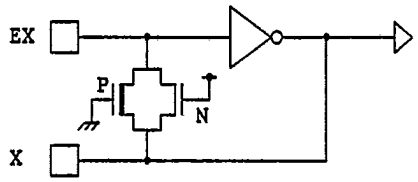
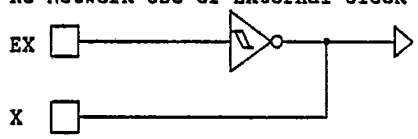
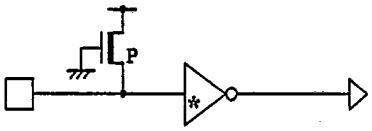
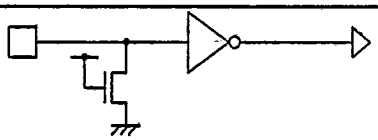
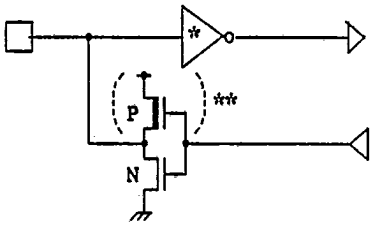
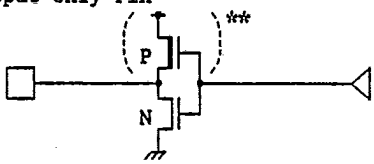
2

T-49-19-44

INPUT/OUTPUT CIRCUITS

All input only pins are internally pulled up, and all output only and input/output pins except O-, P-, and R-Ports have push-pull output buffer (standard pullup). O-, P-, and R-Ports can have push-pull (standard or high-current pullup) or open-drain (standard, high-current, or 12V-interface) buffer using mask option.

Table 4: INPUT/OUTPUT CIRCUITS

Pin	Circuit	Note
EX, X	• Crystal/Ceramic OSC or External Clock* 	• Non-hysteresis inverter • Feedback resistor: Approx. 2 MΩ typ. (at V_{CC}=5V) * When only external clock drive is used, we recommend RC-network OSC.
	• RC-Network OSC or External Clock* 	• Hysteresis inverter • Without feedback resistor * When only external clock drive is used, we recommend RC-network OSC.
$\overline{IRQ}$, $\overline{TC}$, SI, K-Port	• Input Only Pin 	• Input pull-up resistor (P-ch. Tr.): Approx. 300kΩ typ. (at V_{CC}=5V) * Hysteresis inverter for $\overline{IRQ}$, $\overline{TC}$
START		• Input pull-down resistor (N-ch. Tr.):Approx. 300kΩ typ. at (V_{CC}=5V)
$\overline{RESET}$,* $\overline{SC}/\overline{TO}$,* R-Port **	• Input/Output Pin 	• Output pullup resistor (P-ch. Tr.): $\overline{RESET}$: Approx. 300kΩ typ. $\overline{SC}/\overline{TO}$: Approx. 10kΩ typ. (at V_{CC}=5V) * Hysteresis inverter for $\overline{RESET}$, $\overline{SC}/\overline{TO}$ • Output port options for O-, P-, and R-Ports 1: Standard pullup: Pullup resistor (P-ch. Tr.): Approx. 10kΩ typ. (at V_{CC}=5V) 2: High-current pullup: with pullup resistor **3: Standard/high-current/12V interface open-drain: Without P-ch. pullup resistor
SO, P-Port,** O-Port **	• Output Only Pin 	

USER MASK OPTIONS

The MB88500H series has the following mask options, which must be specified by the customer on the attached data release form when devices are ordered.

Table 5: USER MASK OPTIONS

Optional Feature	Symbol	Option	Option No.	Note
Clock	CLK	No	0	f_C=2 MHz to 4 MHz:
		Yes	1	f_C=4 MHz to 8 MHz:
Oscillator Type	OSC	Crystal/ceramic OSC or external clock*	0	* When only external clock drive is used, we recommend RC-network oscillator.
		RC-network OSC or external clock*	1	We recommend no clock prescaler.
Output PLA Data (MB88501)	SPLA	4-bit parallel output	0	MB88505H is fix.
		8-bit parallel output	1	Customer's output PLA data is needed.
Output Port Type	PORT	Standard open-drain	L	Output port circuit option selected must be the same for all O-, P-, and R-Ports.
		Standard pull-up	M	
		High-current open-drain	K	
		High-current pull-up	T	
		12V-interface open-drain	G	P-Port only
Standby Function	STBY	No	0	
		Yes(Software initiation)	1	
Output Port State During Standby	STATE	Hold	0	Output port state option selected must be the same for all O-, P-, and R-Ports.
		High-Z	1	
Standby off Reset Function	SOR	No	0	
		Yes	1	
Output Port Level During reset	RST	High	0	P-Port only
		Low	1	
Watch-dog Timer Function	WDR	No	0	
		Yes	1	

T-49-19-44

NOTES ON OPERATION

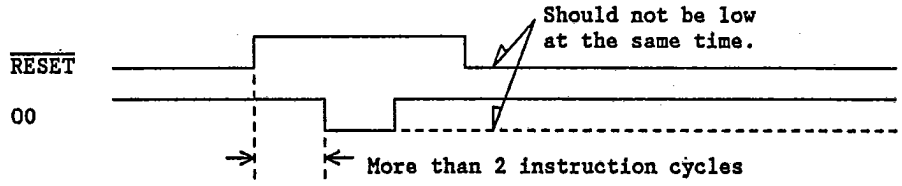
- **Prevention Latch-up**
  Latch-up may occur in CMOS devices when a voltage higher than V_{CC} or lower than V_{SS} is applied to any input or output pin, or when a voltage exceeding the absolute maximum ratings is applied between V_{CC} and V_{SS} pins. If latch-up occurs, the supply current increases greatly, and the device may be thermally destroyed. Therefore, applied voltages should not exceed the maximum ratings.

- **Treatment of Unused Pins**
  Unused input pins should be pulled up or down with external resistors or they may cause some malfunction. (However, the X pin should be open when an external clock oscillator is used.)

- **Special Function of O0 Pin**
  The O0 pin has another function as a test terminal, in addition to its normal function O-Port. If the O0 pin is forced low while the $\overline{\text{RESET}}$ pin is low, the MCU is placed in the test mode. Therefore, the O0 pin should not be forced low while the $\overline{\text{RESET}}$ pin is low (when all output ports are initialized).

  Especially when the open-drain is selected for the output port option, the O0 pin should be externally pulled up because such open-drain outputs are subject to noise disturbance if left floating.

  At least 2 instruction cycles are required to change O0 pin from high to low after releasing reset ($\overline{\text{RESET}}$: Low → High)



- **External Capacitors for Crystal Oscillation**
  Fig. 9 gives an aim of an area where the on-chip oscillator has stable oscillator characteristics and short oscillation stabilization time when an average crystal resonator is used.

  The external capacitor should be adjusted to individual crystal resonators when precise oscillation frequency is required. It is recommended to use crystal with a frequency higher than required oscillation frequency, together with the on-chip divided-by-two prescaler, because crystal resonators with lower oscillation frequency generally tends to have longer stabilization time and wider characteristics variation.

- **Supply Voltage**
  Malfunction may occur even within the recommended operating supply voltage if the supply voltage changes rapidly. Therefore, the supply voltage should be regulated as well as possible. The following conditions are recommended for the power supply:
  (1) V_{CC} ripple (peak-to-peak value) at commercial frequency (50Hz to 60Hz): Less than 10% of typical V_{CC} value.
  (2) V_{CC} transient change rate (such as at switching of power supply): Less than 0.1V/ms.

INSTRUCTION SET DESCRIPTION

The MB88500H series instruction set includes 76 instructions, 83% of which are single-byte and single-cycle, 13% two-byte two-cycle, 1% two byte three-cycle, and 3% three-byte and three-cycle. The MB88500H series instruction set is exactly the same as the MB88500H series instruction set, and is divided into ten functional groups:

- Register-to-register transfer
- Register-to-memory transfer
- Constant transfer
- Arithmetic and logical operations
- Bit manipulation
- Control
- Input/Output
- Branch
- Flag manipulation
- Other

Tables 6 and 7 summarize the MB88500H series instruction set.

Table 6: INSTRUCTION SET SUMMARY

	Mnemonic +operand	Code (Hex.)	Flag/Status ZF	CF	ST	Byte/ Cycle	Operation
Register-to-Register Transfer	TATH	05	·	·	·	1/1	TH←(AC)
	TATL	06	·	·	·	1/1	TL←(AC)
	TAS	07	·	·	·	1/1	SB←(AC)
	TAY	04	·	·	·	1/1	Y←(AC)
	TSA	17	↕	·	·	1/1	4-bit mode: AC←(SB_L), 8-bit mode: AC←(SB_L), X←(SB_H) *4
	TTHA	15	↕	·	·	1/1	AC←(TH)
	TTLA	16	↕	·	·	1/1	AC←(TL)
	TYA	14	↕	·	·	1/1	AC←(Y)
	XX	1B	↕*1	·	·	1/1	(AC)⇄(X)
Register-to-Memory Transfer	L	0D	↕	·	·	1/1	AC←{M(X,Y)}
	LS	2B	↕	·	·	1/1	SB←{M(X,Y)}
	ST	1D	·	·	·	1/1	M(X,Y)←(AC)
	STDC	1A	·	·	↓C	1/1	M(X,Y)←(AC), Y←(Y)-1
	STIC	0A	·	·	↓C	1/1	M(X,Y)←(AC), Y←(Y)+1
	STS	2A	↕	·	·	1/1	M(X,Y)←(SB)
	X	0B	↕*1	·	·	1/1	(AC)⇄{M(X,Y)}
	XD D	50-53*	↕*1	·	·	1/1	(AC)⇄{M(0,D)}; D=0 to 3 (X=0, Y=D)
	XYD D	54-57*	↕*2	·	·	1/1	(Y) ⇄{M(0,D)}; D=4 to 7 (X=0, Y=D)
Constant Transfer	CLA	90	↓	·	·	1/1	AC←0 (Included in LI instruction)
	LI imm	90-9F*	↕	·	·	1/1	AC←imm; imm=0 to 15
	LXI imm	58-5F*	↕	·	·	1/1	X3←0, X2 to X0←imm; imm=0 to 7
	LXID	3D90-3D9F*	↕	·	·	2/2	X←imm; imm=0 to 15
	LRXA imm	3D20-3D3F*	·	·	·	2/3	X ←{ROM(imm | X | Y)}d, d=7-4 AC←{ROM(imm | X | Y)}d, d=3-0 imm=0 to 31
	LYI imm	80-8F*	↕	·	·	1/1	Y ←imm; imm=0 to 15
Arithmetic & Logical Operations	ADC	0E	↕	↕	↓C	1/1	AC←(AC)+{M(X,Y)}+(CF)
	AI imm	3D80-3D8F	↕	↕	↓C	1/1	AC←(AC)+imm; imm=0 to 15
	AND	0F	↕	·	↓Z	1/1	AC←(AC)∩{M(X,Y)}
	C	2E	↕	↕	↓Z	1/1	{M(X,Y)}-(AC)
	CI imm	B0-BF*	↕	↕	↓Z	1/1	imm-(AC); imm=0 to 15
	CYI imm	A0-AF*	·	·	↓Z	1/1	imm-(Y) ; imm=0 to 15

Table 6: INSTRUCTION SET SUMMARY (Continued)

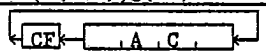
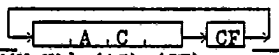
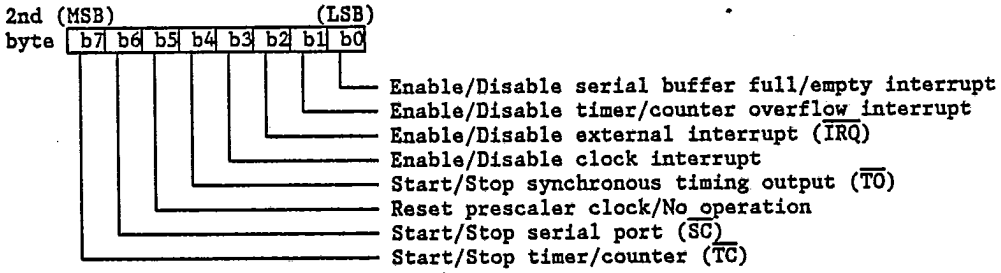
	Mnemonic +Operand	Code (Hex.)	Flag/Status ZF	CF	ST	Byte/ Cycle	Operation
Arithmetic & Logical Operation	DAA	10	·	↕	↓C	1/1	AC←(AC)+6 if (AC)>9 or (CF)=1
	DAS	11	·	↕	↓C	1/1	AC←(AC)+10 if (AC)>9 or (CF)=1
	DCA	3D8F	↕	↕	↓C	1/1	AC←(AC)+15 (Included in AI instruc-
	DCM	19	↕	·	↓C	1/1	M(X,Y)←{M(X,Y)}-1 tion)
	DCY	18	·	·	↓C	1/1	Y←(Y)-1
	EOR	2F	↕	·	↓Z	1/1	AC←{M(X,Y)}⊕(AC)
	ICA	3D81	↕	↕	↓C	1/1	AC←(AC)+1 (Included in AI instruc-
	ICM	09	↕	·	↓C	1/1	M(X,Y)←{M(X,Y)}+1 tion)
	ICX	3DAC	·	·	↓C	2/2	X←(X)+1
	ICY	08	↕	·	↓C	1/1	Y←(Y)+1
	NEG	2D	·	·	↓Z	1/1	AC←(AC)+1
	OR	1F	↕	·	↓Z	1/1	AC←{M(X,Y)}∪(AC)
	ROL	0C	↕	↕	↓C	1/1	
	ROR	1C	↕	↕	↓C	1/1	
	SBC	1E	↕	↕	↓C	1/1	AC←{M(X,Y)}-(AC)-(CF)
Bit Manipulation	RBIT bp	34-37*	·	·	·	1/1	{M(X,Y)}bp←0; bp=0 to 3
	SBIT bp	30-33*	·	·	·	1/1	{M(X,Y)}bp←1; bp=0 to 3
	RBA bp	3DA4 3DA7 *	·	·	·	2/2	(AC)bp←0 ; bp=0 to 3
	SBA bp	3DA0 3DA3 *	·	·	·	2/2	(AC)bp←1 ; bp=0 to 3
	TBA bp	4C-4F*	·	·	↓Z	1/1	(AC)bp-1 ; bp=0 to 3
	TBIT bp	38-3B*	·	·	↓Z	1/1	{M(X,Y)}bp-1; bp=0 to 3
Control	EN imm	3E00-3EFF*	·	·	·	2/2	Enable the internal resources by the operand byte (2nd byte); *3
	DIS imm	3F00-3FFF*	·	·	·	2/2	Disable the internal resources by the operand byte (2nd byte); *3
	RST	3DAD	·	·	·	2/2	System initialization
Input/ Output	IN	13	↕	·	·	1/1	AC←(R)Y ; Y=0 to 3 (Port #) AC←(REG)Y; Y=9 to 15
	INK	12	↕	·	·	1/1	AC←(K)
	OUT	03	·	·	·	1/1	(R)Y←(AC); Y=0 to 3 (Port #) (REG)Y←(R);Y=9 to 15
	OUTO	01	·	·	·	1/1	If CF=0 O3-O0←(AC) If CF=1 O7-O4←(AC)
	OUTP	02	·	·	·	1/1	P←(AC)
	RSTD d	44-47*	·	·	·	1/1	(R)d←0; d=0 to 3 (Bit # of Port #0)
	RSTR	22	·	·	·	1/1	(R)Y←0; Y=0 to 15 (Bit #)
	SETD d	40-43*	·	·	·	1/1	(R)d←1; d=0 to 3 (Bit # of Port #0)
	SETR	20	·	·	·	1/1	(R)Y←1; Y=0 to 15 (Bit #)
	TSTD d	48-4B*	·	·	↓Z	1/1	(R)d-1; d=8 to 11 (Bit #)
	TSTR	24	·	·	↓Z	1/1	(R)Y-1; Y=0 to 15 (Bit #)
Branch	CALL addr	6000-6FFF*	·	·	·	2/2	If ST=1, Subroutine Call for addr; addr=0 to 4095. ST=0, Not Subroutine Call.

Table 6: INSTRUCTION SET SUMMARY (Continued)

	Mnemonic +Operand	Code (Hex.)	Flag/Status ZF	CF	ST	Byte/ Cycle	Operation
Branch	JMP addr	C0-FF*	·	·	·	1/1	If ST=1, Branch to addr; addr=0 to 63 ST=0, No Branch.
	JPXY addr	3D00-3D1F*	·	·	·	2/2	Branch always to addr on page #n;
	JPL addr	7000-7FFF*	·	·	·	2/2	If ST=1, Branch to addr; addr=0 to 4095. ST=0, No Branch.
	RTI	3C	·	·	·	1/1	Return From Interrupt Routine.
	RTS	2C	·	·	·	1/1	Return From Subroutine
Flag Manipulation	RSTC	23	·	↓	·	1/1	CF←0
	SETC	21	·	↑	·	1/1	CF←1
	TSTC	28	·	·	↓CF	1/1	(CF)-1
	TSTI	25	·	·	↓IF	1/1	(IF)-1, (If $\overline{IRQ}$=L, IF=1)
	TSTS	27	·	·	↓SF	1/1	(SF)-1, SF←0
	TSTV	26	·	·	↓VF	1/1	(VF)-1, VF←0
	TSTZ	29	·	·	↓ZF	1/1	(ZF)-1
Other	NOP	00	·	·	·	1/1	No Operation

Notes:

*1: ZF is set or reset depending on contents of AC after instruction execution.
*2: ZF is set or reset depending on contents of Y after instruction execution.
*3: Each bit of the operand (the second byte) functions as follows:



*4: MB88501H and MB88503H: AC←(SB), ZF affected
MB88505H : AC←(SBL), X←(SBH), ZF not affected

Symbols and Abreviations

Symbols	Meaning
←	Is transferred to
⇄	Is exchanged with
+	Arithmetic plus
−	Arithmetic minus
⊕	Logical exclusive or
∩	Logical OR
∪	Logical AND
$\overline{\quad}$ (Overline)	Negation
( )	Contents of parenthesis
↑	Set to "1" always
↓	Set to "0" always
↕	Affected (set or reset) by operation results
↓C	Set to "0" due to carry (not carry flag)
↓CF	Set to "0" due to carry flag
↓IF	Set to "0" due to interrupt flag
↓SF	Set to "0" due to serial buffer full/empty flag
↓VF	Set to "0" due to timer/counter overflow flag
↓Z	Set to "0" due to zero (not zero flag)
↓ZF	Set to "0" due to zero flag
·	Not affected

Abbreviation	Meaning
AC	Accumulator
addr	Jump address
bp	Bit pointer (that is part of the instruction code)
C	Carry
CF	Carry flag
d	Direct line number (that is part of the instruction code)
IF	Interrupt flag
imm	Immediate data
$\overline{\text{IRQ}}$	Interrupt request
K	K-Port (K3 to K0)
LSB	Least significant bit
M(X,Y)	Data memory (RAM) location indirectly addressed by data pointer (X- and Y-registers)
M(0,D)	Data memory (RAM) location directly addressed by "D" bits in the instruction code, in page #0 (X=0)
MSB	Most significant bit
O	O-Port (O7-O0)
PLA	Programmable Logic Array
R	R-Port (#0: R3-R0, #1: R7-R4, #2: R11-R8, #3: R15-R12)
(R)Y; Y=n	① R-Port #n specified by Y-register (Y=0 to 3) ② R-Port bit n specified by Y-register (Y=0 to 15)
(R)d; d=n	R-Port bit n specified by "d" bits in the instruction code
SB	Serial buffer register
SF	Serial buffer full/empty flag
ST	Status flag
TH	Timer/counter high byte
TL	Timer/counter low byte
VF	Timer/counter overflow flag
X	X-register (that indicates page # in data memory RAM)
Xn	The n-th bit X-register
Y	Y-register
Z	Zero
ZF	Zero flag

Table 7: INSTRUCTION CODES SUMMARY

L / H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	OUTO	OUTP	OUT	TAY	TATH	TATL	TAS	ICY	ICM	STIC	X	ROL	L	ADC	AND
1	DAA	DAS	INK	IN	TYA	TTHA	TTLA	TSA	DCY	DCM	STDC	XX	ROR	ST	SBC	OR
2	SETR	SETC	RSTR	RSTC	TSTR	TSTI	TSTV	TSTS	TSTC	TSTZ	STS	LS	RTS	NEG	C	EOR
3	SBIT bp				RBIT bp				TBIT bp				RTI	* EXT	EN imm	DIS imm
4	SETD d				RSTD d				TSTD d				TBA bp			
5	XD D				XYD D				LXI imm							
6	CALL addr															
7	JPL addr															
8	LYI imm															
9	(CLA)	LI imm														
A	CYI imm															
B	CI imm															
C	JMP addr															
D																
E																
F																

NOTE: : 1-byte/1-cycle instruction : 2-bytes/2-cycles instruction

* See the next page

2

Table 7: INSTRUCTION CODES SUMMARY (Continued)
Extended instruction

3DH \ 3DL	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	JPXY addr															
1																
2	LRXA imm															
3																
4	NOT USED															
5																
6	NOT USED															
7																
8		(ICA)	AI imm													(DCA)
9	LXID imm															
A	SBA bp				RBA bp				NOT USED				ICX	RST	NOT USED	
B	NOT USED															
C	NOT USED															
D																
E																
F																

Note: ▱ : 3 byte/3 cycle instruction

PRODUCT LINE-UP AND DEVELOPMENT TOOLS

The MB88500H series consists of the MB88501H, MB88503H and MB88505H. The MB88508H are available as piggyback EPROM evaluation devices for MB88501H and MB88503H. MB88508U is for the MB88505H. Refer to Table 8.

Table 8: MB88500H SERIES PRODUCT LINE-UP & DEVELOPMENT TOOLS

	MB88501H-P/ -PSH/-PF	MB88503H-P/ -PSH/-PF	MB88505H-P/ -PSH/-PF	MB88508H-C/ -CF-101/102	MB88508U-C/ -CF-101/102
ROM Size	4K x 8 bits (On-chip mask ROM)	2K x 8 bis (On-chip mask ROM	4K x 8 bits (On-chip mask ROM)	8K x 8 bits (External EPROM)	
RAM Size (Directly addressed locations)	256 x 4 bits (0-7)				
I/O Port:	Total 36 lines				
-Input only port	4				
-Output only port	12				
-I/O port	15				
-Control port	5 (Including serial I/O)				
Output Port Type	· STD P/U · STD O/D · H/C P/U · H/C O/D · 12V interface O/D (P-Port) (Mask option)			· STD P/U:101 · STD O/D:102	
Output PLA Pattern	33 patterns · Dual 4-bit parallel output · 8-bit PLA output (32 patterns)		· Dual 4-bit parallel output	· Dual 4-bit parallel output	
Stack Depth (Nesting level)	8 levels				
Timer/Counter:	Yes				
-Buffer size	8 bits				
-Clock source	Internal/External				
Serial I/O:	Yes	Yes	Yes	Yes	
-Buffer size	4 bits	4/8 bits	4 bits	4/8 bits	
-Clock source	Internal/External	Internal/ External	Internal/ External	Internal/ External	
-Output latch	Yes	Yes	Yes	Yes	
Clock Generator:	Yes		Yes		
-Oscillator type	· Crystal/External · RC-Network External (Mask option)		· Crystal/External (Fixed)		
-Clock Frequency (With prescaler)	2 MHz-4 MHz (4 MHz-8 MHz)		- 4 MHz-8 MHz	- 1 MHz-6 MHz	
Clock Prescaler (Divid-by-two)	Yes/No (Mask option)		Yes (Fixed)		
Interrupt Function	Yes				
-Nesting level	Single level				
-Interrupt sources	4 sources				

2

PRODUCT LINE-UP AND DEVELOPMENT TOOLS

Table 8: MB88500H SERIES PRODUCT LINE-UP & DEVELOPMENT TOOLS (Countinued)

	MB88501H-P/ -PSH/-PF	MB88503H-P/ -PSH/-PF	MB88505H-P/ -PSH/-PF	MB88508H-C -CF	MB88508U-C -CF
Standby Function: -Initiation method -Oscillator state during standby -Output state during standby -Standby off reset function	· Yes/No (Mask option) · Software · Idle/Stop (Software selectable) · Hold/High-Z (Mask option) · Yes/No (Mask option)			· Yes (Fixed) · Software · Idle/Stop (Software selectable) · Hold:102/High-Z:101 (Mask option) · Yes/No (Mask option)	
Watch Dog Timer Function	· No · Yes (Mask option)			· No (Fixed)	
Number of Instructions	76			78	77
Instruction Length/Cycle	1/1, 2/2, or 2/3			1/1, 2/2, 2/3, or 3/3	
Min. Instruction Execution Time	1.5 µs at 8 MHz (With prescaler)				2.0µs at 6MHz (With prescaler)
Power Supply: -Standard version: -Active -Standby -A-version: -Active -Standby	Single +5V Yes · 4.5V to 5.5V · 3.5V to 6.0V Yes · 3.5V to 6.0V · 3.5V to 6.0V			Single +5V Yes · 4.5V to 5.5V · 3.5V to 6.0V No - -	
Operating Temp. Range: -Standard version -A-version	-40°C to +85°C -30°C to +70°C			-40°C to +85°C -	
Process	CMOS				
Package	DIP-42P SH-DIP-42P QFP-48P			MDIP-42P MQFP-48P	
Development Tools: -Hardware -Software	MB2115-01 : CRT unit (Common) MB2115-02 : Monitor board with keyboard (Common) MB2115-04 : EPROM writer (Common) MB2115-31A : DUE board SM05215-A010: Intellec series III MDS cross-assembler SM07415-A012: CP/M-86 cross-assembler SMXXXXX-XXXX: PC-DOS cross-assembler SM07415-G022: CP/M-86 host emulator SMXXXXX-XXXX: PC-DOS host emulator				

Note STD: Standard
H/C: High-current
P/U: Pull-up
O/D: Open-drain

ELECTRICAL CHARACTERISTICS

- **ABSOLUTE MAXIMUM RATINGS (Standard and A-version)†**

Parameter	Symbol	Rating			Unit	Remarks
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	V_{SS}-0.3		V_{SS}+7.0	V	
	V_{SS}		0		V	
Input Voltage	V_{IN}	V_{SS}-0.3		V_{SS}+7.0	V	Should not exceed V_{CC}+0.3V.
Output Voltage	V_{OUT}	V_{SS}-0.3		V_{SS}+7.0	V	Should not exceed V_{CC}+0.3V.
		V_{SS}-0.3		V_{SS}+15.0	V	P-Port (12V interface open-drain)
Output Low Current	I_{OL}			20	mW	
Total Output Low Current	ΣI_{OL}			80	mW	
Power Dissipation	P_D			600	mW	
Operating Ambient Temperature	T_A	-40		+85	°C	
Storage Temperature	T_{STG}	-55		+150	°C	

† Permanent device damage may occur if the above ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

• **RECOMMENDED OPERATING CONDITIONS (Standard version)**

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	Active operation range
		3.5		6.0	V	Standby operation range
	V_{SS}		0		V	
Input High Voltage	V_{IH}	$0.75 \cdot V_{CC}$		$V_{CC}+0.3$	V	K-Port, SI
	V_{IHS}	$0.8 \cdot V_{CC}$		$V_{CC}+0.3$		EX, START, SC/TO, IRQ, TC, RESET
Input Low Voltage	V_{IL}	$V_{SS}-0.3$		$0.25 \cdot V_{CC}$	V	K-Port, SI
	V_{ILS}	$V_{SS}-0.3$		$0.2 \cdot V_{CC}$	V	EX, START, SC/TO, IRQ, TC, RESET
Operating Ambient Temperature	T_A	-40		+85	°C	

• **RECOMMENDED OPERATING CONDITIONS (A-version)**

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	3.5	5.0	6.0	V	Active operation range
		3.5		6.0	V	Standby operation range
	V_{SS}		0		V	
Input High Voltage	V_{IH}	$0.75 \cdot V_{CC}$		$V_{CC}+0.3$	V	K-Port, SI
	V_{IHS}	$0.8 \cdot V_{CC}$		$V_{CC}+0.3$		EX, START, SC/TO, IRQ, TC, RESET
Input Low Voltage	V_{IL}	$V_{SS}-0.3$		$0.25 \cdot V_{CC}$	V	K-Port, SI
	V_{ILS}	$V_{SS}-0.3$		$0.2 \cdot V_{CC}$	V	EX, START, SC/TO, IRQ, TC, RESET
Operating Ambient Temperature	T_A	-30		+70	°C	

- **DC CHARACTERISTICS (Standard and A-version)**
  (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Condition	Value			Unit
				Min.	Typ.	Max.	
Output High Voltage	V_{OH}	O-, P-, R-Ports (Standard/High-current pull-up), $\overline{SC}/\overline{TO}$, SO	V_{CC}=4.5V I_{OH}=-200μA	2.4			V
			V_{CC}=4.5V I_{OH}=-10μA	4.0			V
Output Low Voltage	V_{OL}	O-, P-, R-Ports (All output options), $\overline{SC}/\overline{TO}$, SO, $\overline{RESET}$	V_{CC}=4.5V I_{OL}=1.8mA			0.4	V
			V_{CC}=4.5V I_{OL}=3.6mA			0.6	V
Input Leakage Current	I_{IH}	START, EX	V_{CC}=5.5V V_{IH}=5.5V			60	mA
	I_{IL}	R-Port(Standard/High-current pull-up), $\overline{SC}/\overline{TO}$	V_{CC}=5.5V V_{IL}=0.4V			-1.8	mA
		$\overline{EX}$, K-Port, $\overline{SI}$, $\overline{RESET}$, $\overline{IRQ}$, $\overline{TC}$	V_{CC}=5.5V V_{IL}=0.4V			-60	μA
Open-Drain Output Leakage Current	I_{LEAK}	O-, P-, R-Ports (Standard/High-current/12V interface open-drain)	V_{CC}=5.5V V_{OH}=5.5V Output in high-Z		0.1	10	μA
Total I/O Leakage Current (High-Z)	ΣI_{IZ}	All pins except V_{CC}, V_{SS}, EX and $\overline{RESET}$	V_{CC}=5.5V(Standby), V_{IN}=0V to 6.0V, High-Z state			±10	μA
Supply Current	I_{CC}	V_{CC}	V_{CC}=5.0V(Typ.), 5.5V(Max.) fc=2MHz(Active), All outputs open		4	12	mA
	I_{CCH}	V_{CC} (With standby function)	V_{CC}=6.0V fc=0(Standby), All outputs open			10	μA
Input Capacitance	C_{IN}	All pins except V_{CC} and V_{SS}	fc=1MHz		10	20	pF

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T-49-19-44

- **AC CHARACTERISTICS (Standard and A-version)**

CLOCK TIMING
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin	Condition	Value Min.	Value Max.	Unit	Remarks
Clock Frequency	f_C	EX, X	Crystal/ceramic or RC-network OSC or external clock drive: Figs. 6 and 7	2	4	MHz	Without prescaler
				4	8		With prescaler
Clock Cycle Time	t_{cyc}	EX, X	Figs. 6 and 7	0.25	0.5	µs	
Input Clock Pulse Width	P_{WCH}, P_{WCL}	EX	External clock drive(with X open): Figs. 6 and 7	100		ns	Without prescaler
				50			With prescaler
Input Clock Rise/Fall Time	t_{cr}, t_{cf}	EX	External clock drive(with X open): Figs. 6 and 7	5	100	ns	

Fig. 6: CLOCK TIMING

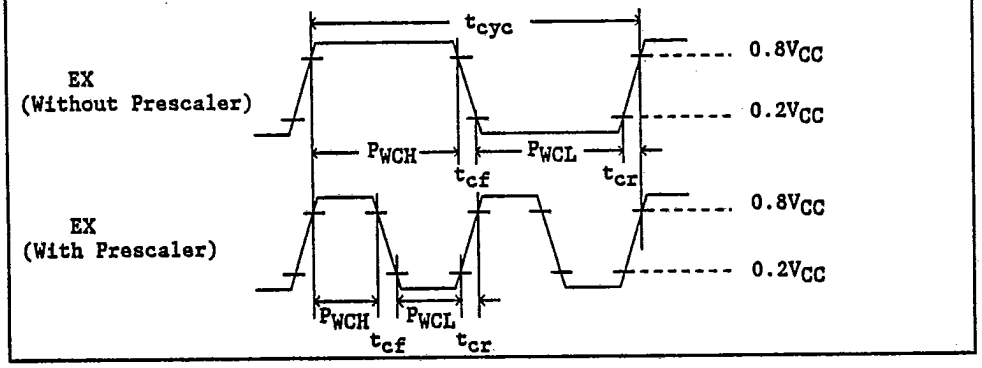
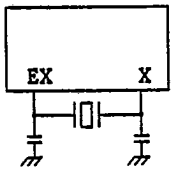
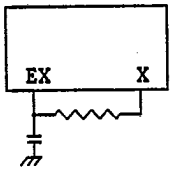


Fig. 7: CLOCK CIRCUIT CONFIGURATIONS

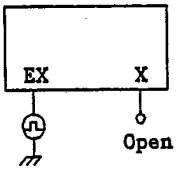
(1) Crystal/Ceramic Oscillator



(2) RC-Network Oscillator*



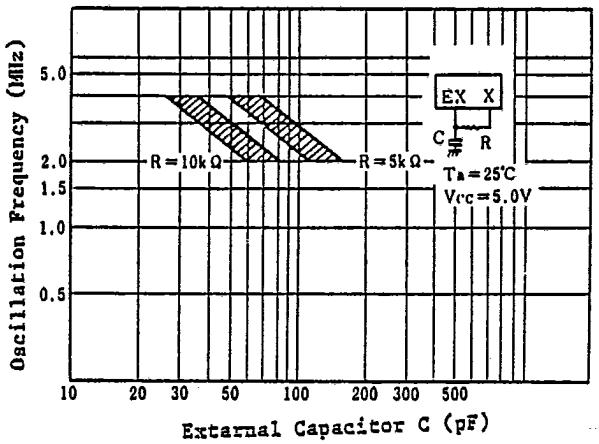
(3) External Clock Drive



* When the RC-network oscillator is used, the following conditions must be met: 1) The prescaler is not used.
2) V_{CC}=5V±10%
3) T_A=-40°C to +85°C(Standard version), T_A=-30°C to +70°C(A-version)
4) f_C does not exceed 4 MHz (Max. clock frequency is about 3.2 MHz at V_{CC}=5V and T_A=25°C.)

T-49-19-44

Fig. 8: RC-NETWORK OSCILLATOR CHARACTERISTICS (EXAMPLE)



Note:
When the RC-network oscillator is used, the following conditions must be met:
1) The prescaler is not used. 2) V_{CC} = 5 V ± 10 %
3) T_A = -40 °C to +85 °C (Standard version) TA= -30 °C to +70 °C (A-version)
4) fc does not exceed 3.2 MHz.

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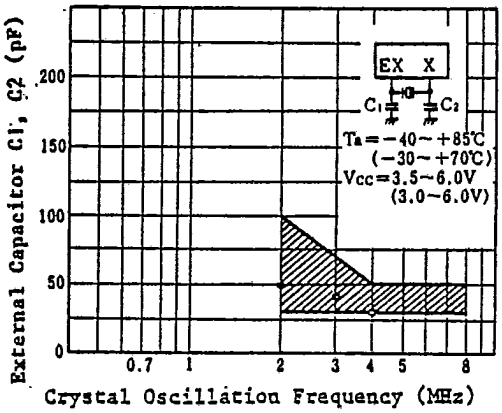
Fig. 9: CRYSTAL OSCILLATOR CHARACTERISTICS (EXAMPLE)



Notes:
1) The cross-hatched portion is an area where the on-chip oscillator has stable characteristics and short stabilization time when a typical crystal resonator is used. This chart gives an target value of the external capacitor to realize the desired frequency. When an exact frequency is needed, capacitor value should be determined, adjusted to individual crystal resonator characteristics.

2) Generally speaking, crystal resonators with lower oscillation frequency tend to have longer stabilization time and wider characteristic variations which affect on-chip oscillator characteristics. So, we recommend a high-frequency crystal resonator with on-chip 1/2 prescaler.

OUTPUT TIMING (Standard and A-version)

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Conditions	Value		Unit
				Min.	Max.	
O-,P-,R-Ports Delay Time	t_{PDH}	O-Port P-Port R-Port	Fig. 10		1000	ns
	t_{PDL}				350	
Serial Port Delay Time	t_{SDH}	SO	Fig. 10		1000	ns
	t_{SDL}				350	

Notes:
1. A 10kΩ pull-up is required when open-drain output is used.
2. All the output loading values are 50pF + 1TTL. See figure below.

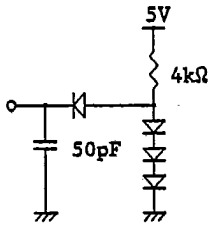
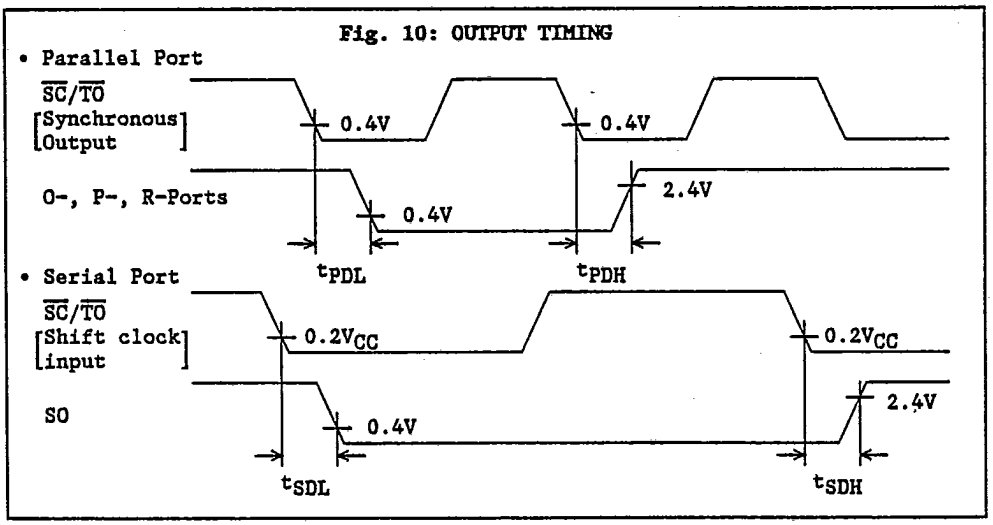


Fig. 10: OUTPUT TIMING



INPUT TIMING (Standard and A-version)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pin/Port	Conditions	Value		Unit
				Min.	Max.	
Input Data Setup Time	t_{DS}	K-Port, R-Port	Fig. 11	t_{cyc}+1000		ns
Input Data Hold Time	t_{DH}				t_{cyc}-50	
SI Input Setup Time	t_{SDS}	SI	Fig. 11	600		ns
SI Input Hold Time	t_{SDH}			600		
Device Control Setup Time (Synchronous mode)	t_{CS}	$\overline{RESET}$	Fig. 11		$2t_{cyc}$-200	ns
		$\overline{IRQ}$			$2t_{cyc}$-200	
Device Control Hold Time (Synchronous mode)	t_{CH}	$\overline{RESET}$	Fig. 11	$8t_{cyc}$+50		ns
		$\overline{IRQ}$		$2t_{cyc}$+50		
Timing Input Setup Time (synchronous mode)	t_{TS}	$\overline{TC}$	Fig. 11		$2t_{cyc}$-200	ns
Timing Input Hold Time (Synchronous mode)	t_{TH}	$\overline{TC}$	Fig. 11	$2t_{cyc}$+50		ns
Control Signal Low Level Time (Asynchronous mode)	P_{WCNL}	$\overline{SC}/\overline{TO}$	Fig. 11	$6t_{cyc}$+250		ns
		$\overline{IRQ}$, $\overline{TC}$		$6t_{cyc}$+250		
		$\overline{RESET}$		$12t_{cyc}$+250		
Control Signal High Level Time (Asynchronous mode)	P_{WCNH}	$\overline{SC}/\overline{TO}$	Fig. 11	$12t_{cyc}$+250		ns
		$\overline{RESET}$, $\overline{TC}$, $\overline{IRQ}$		$6t_{cyc}$+250		
		START		500		
Control Signal Rise and Fall Time	t_{CNr}, t_{CNf}	START, $\overline{SC}/\overline{TO}$, $\overline{IRQ}$ $\overline{RESET}$, $\overline{TC}$	Fig. 11	Should be less than 200ns		

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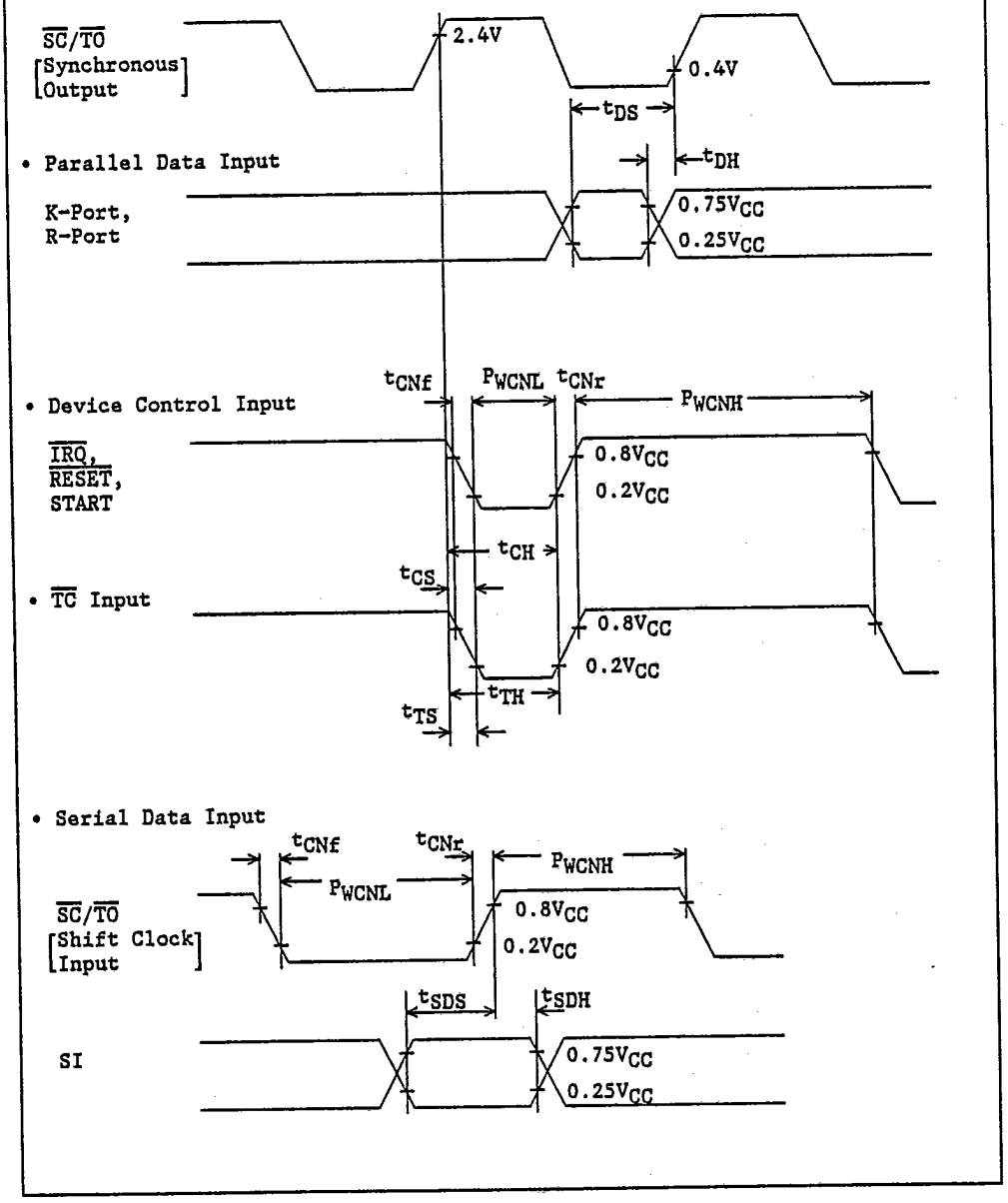
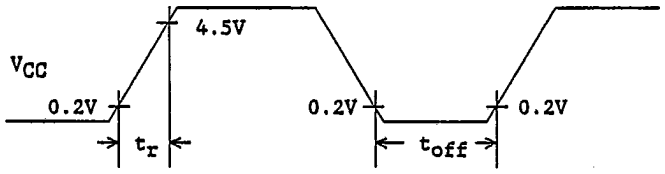
Fig. 11: INPUT TIMING



- **POWER-ON RESET (Standard and A-version)**

Parameter	Symbol	Condi-tions	Value		Unit	Remarks
			Min.	Max.		
Power Supply Rise Time	t_r	Fig. 12	0.05	50	ms	Required for operation of the power-on reset circuit
Power Supply Shut-off Time	t_{off}	Fig. 12	1		ms	Required for accurate circuit operation repeatability

Fig. 12: POWER-ON RESET TIMING



Note:
Power supply should be raised smoothly.

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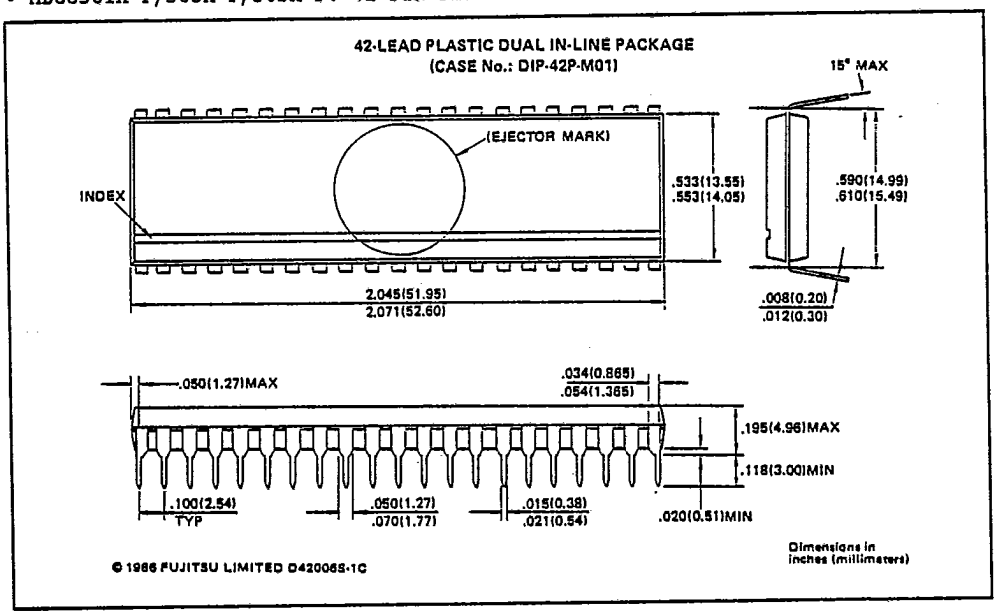
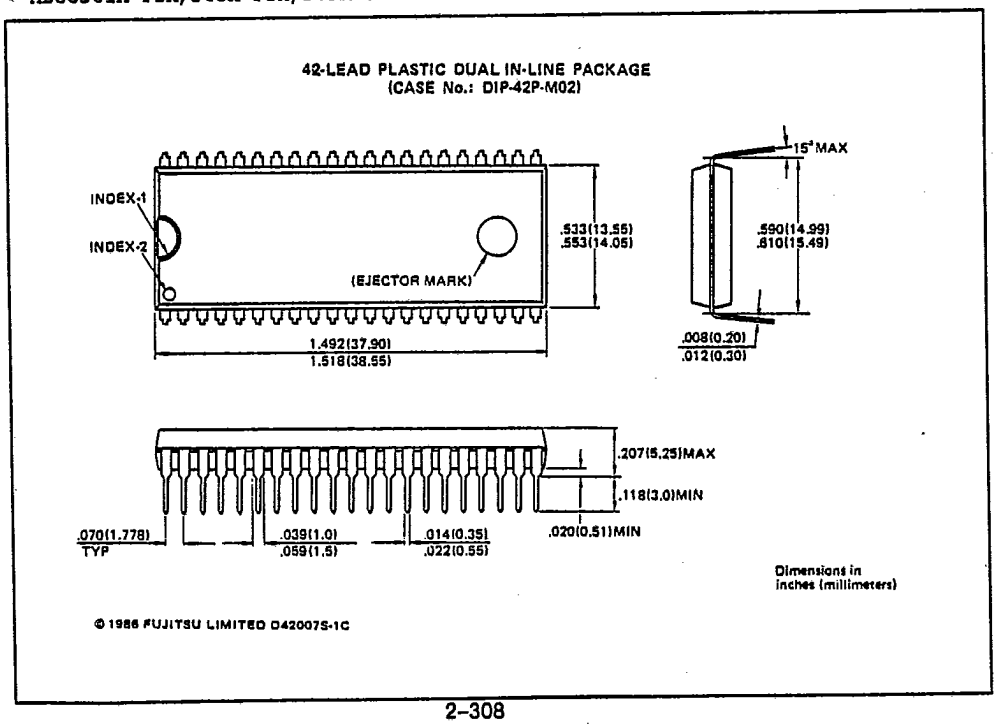
T-49-19-44

PACKAGE DIMENSIONS

- MB88501H-P/503H-P/505H-P: 42-PIN PLASTIC STANDARD DIP

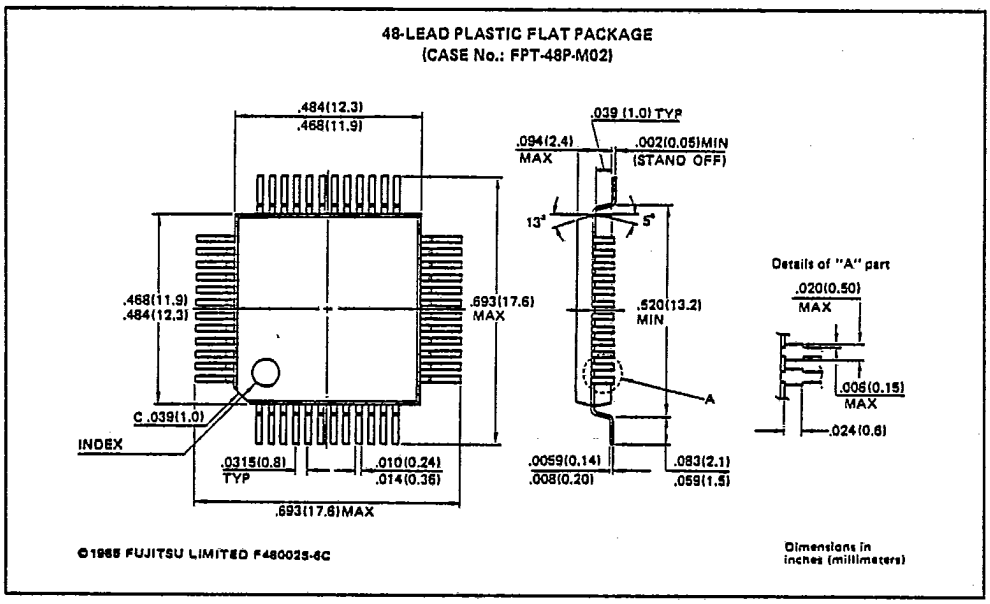


- MB88501H-PSH/503H-PSH/505H-PSH: 42-PIN PLASTIC SHRINK DIP



PACKAGE DIMENSIONS (Continues)

• MB88501H-PF/503H-PF/505H-PF: 48-PIN PLASTIC FLAT PACKAGE



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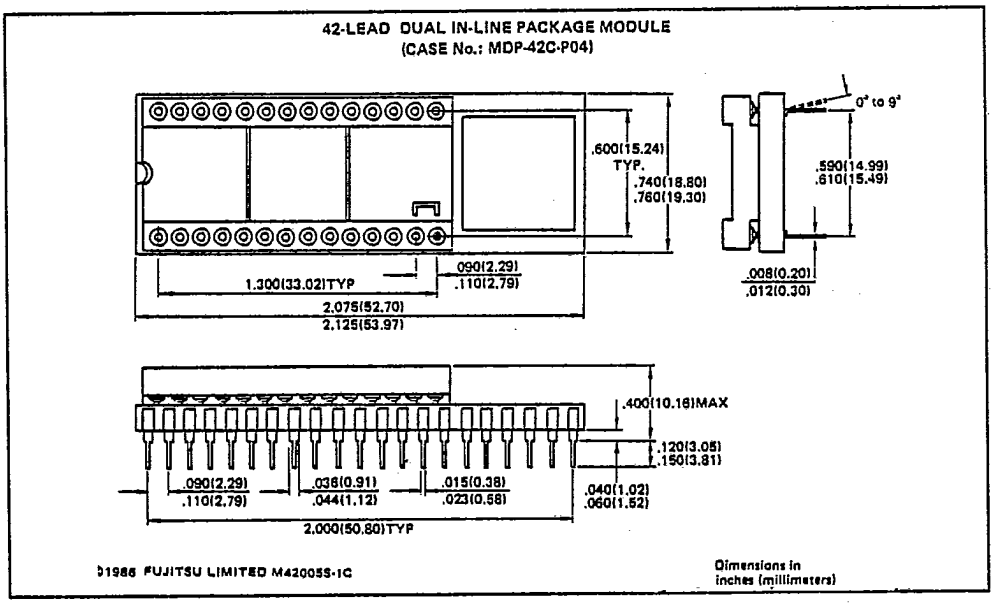
T-49-19-44

PACKAGE DIMENSIONS (Continues)

• MB88508H-C/MB88508U-C: 42-PIN CERAMIC MODULE



• MB88508H-CF/MB88508U-CF: 48-PIN CERAMIC MODULE