

Transcend 44-Pin IDE Flash Module (Horizontal)

128M ~ 4GB

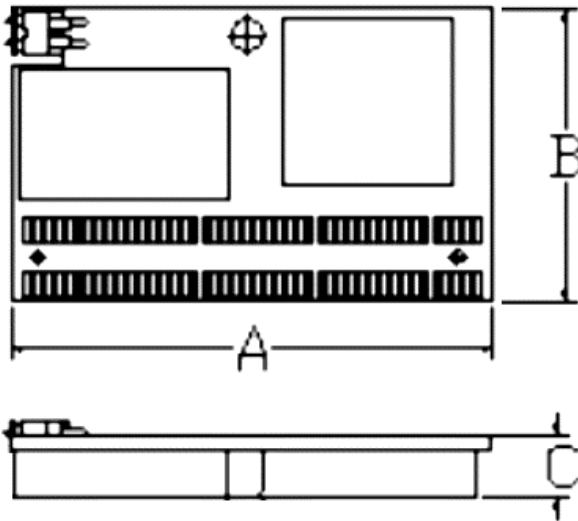
Description

With an IDE interface and strong data retention ability, 44-Pin IDE Flash Modules are ideal for use in the harsh environments where Industrial PCs, Set-Top Boxes, etc. are used.

Features

- RoHS compliant
- Fully compatible with devices and OS that support the IDE standard (44-Pin, pitch = 2.00 mm)
- Non-volatile Flash Memory for outstanding data retention
- Built-in ECC (Error Correction Code) functionality and wear-leveling algorithm ensures highly reliable of data transfer
- Supports up to Ultra DMA Mode 4
- Supports PIO Mode 6
- LED indicates status of usage (Data Access)
- Shock resistance

Placement



Dimensions

Side	Millimeters	Inches
A	46.00 ± 0.40	1.81 ± 0.016
B	28.00 ± 0.20	1.10 ± 0.008
C	6.00 ± 0.50	0.24 ± 0.020

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Specifications

Physical Specifications		
Storage Capacities	128 MB to 4 GB	
Dimensions (mm)	Length	46.00 ± 0.40
	Width	28.00 ± 0.20
	Height	5.87 ± 0.50
Weight	7 g (Max.)	
Connector	44-Pin standard IDE/ATA connector (Pitch 2.0 mm)	

Environmental Specifications	
Operating Temperature	0 °C to 70 °C
Storage Temperature	- 40 °C to 85 °C

Reliability	
Write/Erase Endurance	> 2,000,000 cycles
Read Endurance	Unlimited
Data Reliability	Built-in 4 symbol correction ECC (per 512 bytes Sector)
Data Retention	10 years
Connector Durability	5,000 times

Interface Specifications	
Jumper Settings	Master/Slave Settings
ATA Compatibility	ATA/ATAPI 5
	PIO Modes 0 – 6
	UDMA Modes 0 – 4

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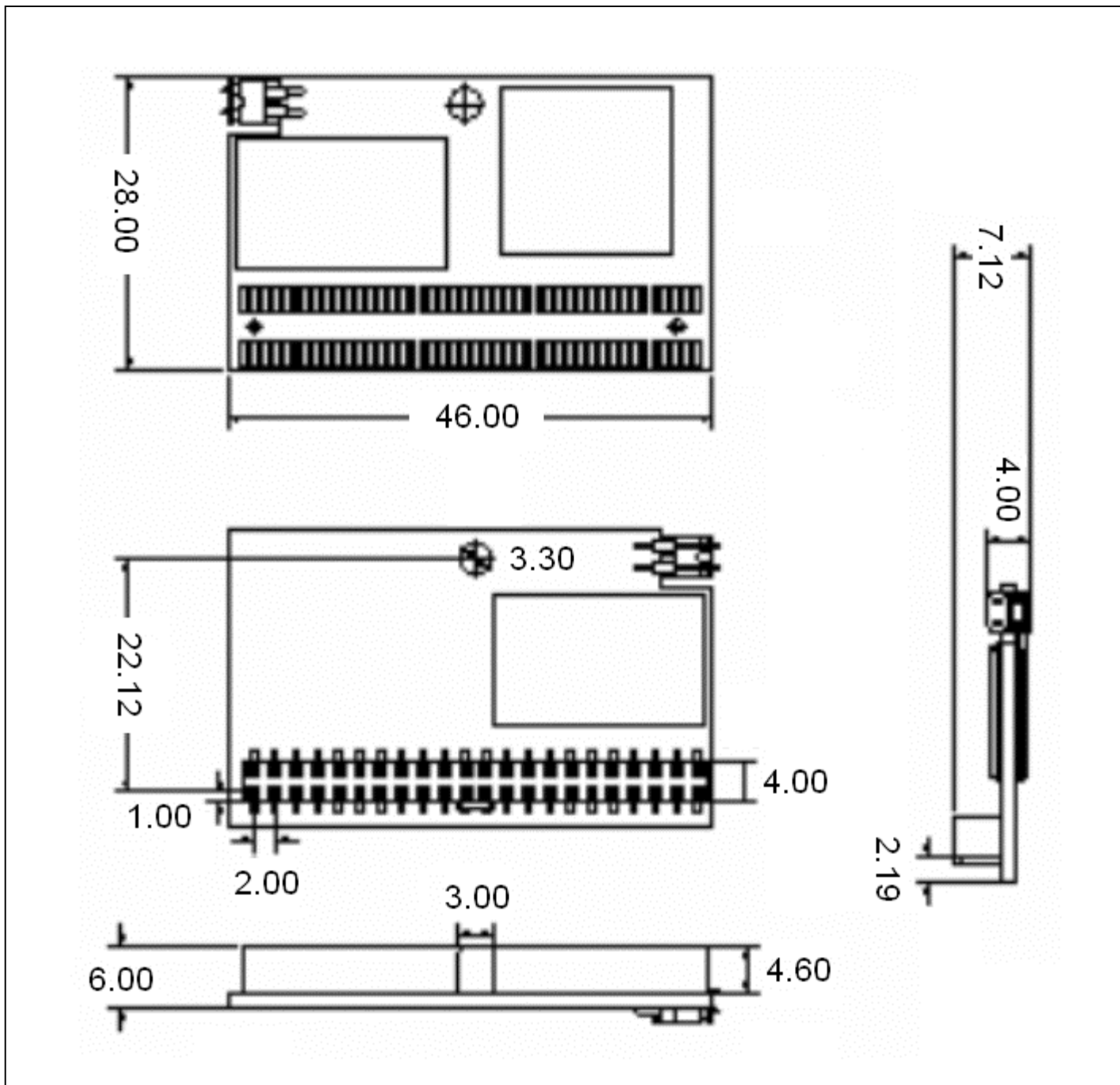
Capacity Specifications				
Transcend P/N	Capacity	Cylinder (C)	Head (H)	Sector (S)
TS128MDOM44H	128MB	978	8	32
TS256MDOM44H	256MB	978	16	32
TS512MDOM44H	512MB	993	16	63
TS1GDOM44H	1GB	1985	16	63
TS2GDOM44H	2GB	3954	16	63
TS4GDOM44H	4GB	7889	16	63

Compliance and Warranty	
Compliance	CE, FCC and BSMI
Warranty	2 years

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Package Dimensions

Below figure illustrates the Transcend 44-Pin IDE Flash Module (Horizontal). All dimensions are in mm.



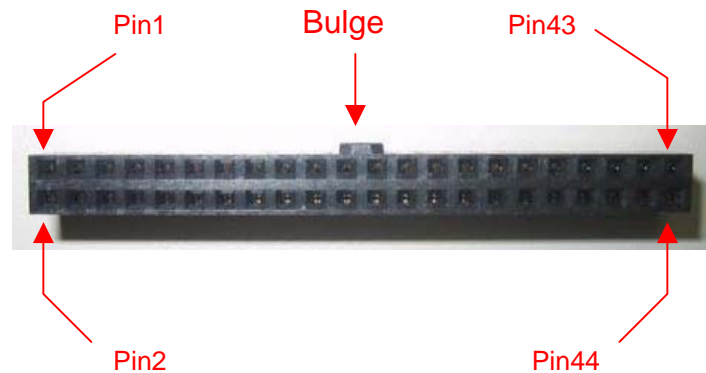
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Pin Assignments

Pin No.	Pin Name	Pin No.	Pin Name
01	-RESET	02	GND
03	DD7	04	DD8
05	DD6	06	DD9
07	DD5	08	DD10
09	DD4	10	DD11
11	DD3	12	DD12
13	DD2	14	DD13
15	DD1	16	DD14
17	DD0	18	DD15
19	GND	20	KEY-PIN (OPEN)
21	DMARQ	22	GND
23	-DIOW : STOP	24	GND
25	-DIOR : -HDMARDY : HSTROBE	26	GND
27	IORDY : DDMARDY : DSTROBE	28	CSEL
29	-DMACK	30	GND
31	INTRQ	32	IOCS16B
33	DA1	34	-PDIAG : -CBLID
35	DA0	36	DA2
37	-CS0	38	-CS1
39	-DASP	40	GND
41	VCC	42	VCC
43	GND	44	NC (No Connect)

Pin Layout



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Pin Description

Pin No.	Signal	I/O*	Description
01	-RESET	I	Hardware reset signal from the host.
17, 15, 13, 11, 09, 07, 05, 03, 04, 06, 08, 10, 12, 14, 16, 18	DD0 ~ DD15 (Device Data)	I/O	16-bit bi-direction Data Bus. DD(7:0) are used for 8-bit register transfers.
21	DMARQ (DMA Request)	O	For DMA data transfers. Device will assert DMARQ when the device is ready to transfer data to or from the host.
23	-DIOW (I/O Write)	I	This is the strobe signal used by the host to write to the device register or Data port.
	STOP (Stop UDMA Burst)		The host asserts this signal during an UDMA burst to stop the DMA burst.
25	-DIOR (I/O Read)	I	This is the strobe signal used by the host to read from the device register or the Data port.
	-HDMARDY (UDMA ready)		When UDMA mode DMA Read is ready, -HDMARDY should be asserted by the host to indicate that the host is ready to receive DMA data-in burst.
	HSTROBE (UDMA Strobe)		HSTROBE receives the data-out strobe signal from the host for an UDMA burst.
27	IORDY (I/O channel ready)	O	This signal is used to temporarily stop the host register access (read or write) when the device is not ready to respond to a data transfer request.
	DDMARDY (UDMA ready)		The device will assert this signal to indicate that the device is ready to receive UDMA data-out burst.
	DSTROBE (UDMA data strobe)		When UDMA mode DMA Read is active, this signal is the data-in strobe generated by the device.
28	CSEL (Cable select)	I	This pin is used to configure this device as Device 0 or Device 1. When this pin is grounded, this device is configured as Device 0. When this pin is High, this device is configured as Device 1.
29	-DMACK (DMA acknowledge)	I	This signal is used by the host in response to DMARQ to initiate DMA transfer.
31	INTRQ (Interrupt)	O	When this device is selected, this signal is the active high Interrupt Request to the host.
32	IOCS16B	O	During PIO transfer mode 0, 1 or 2, this pin indicates to the host the 16-bit data port has been addressed and the device is prepared to send or receive a 16-bit data word. When transferring in PIO mode 3, 4, or above, this signal should not be used by the host, and all transfers will be 16-bit. When transferring in DMA mode, the host must use a 16-bit DMA channel and this signal will not be asserted.

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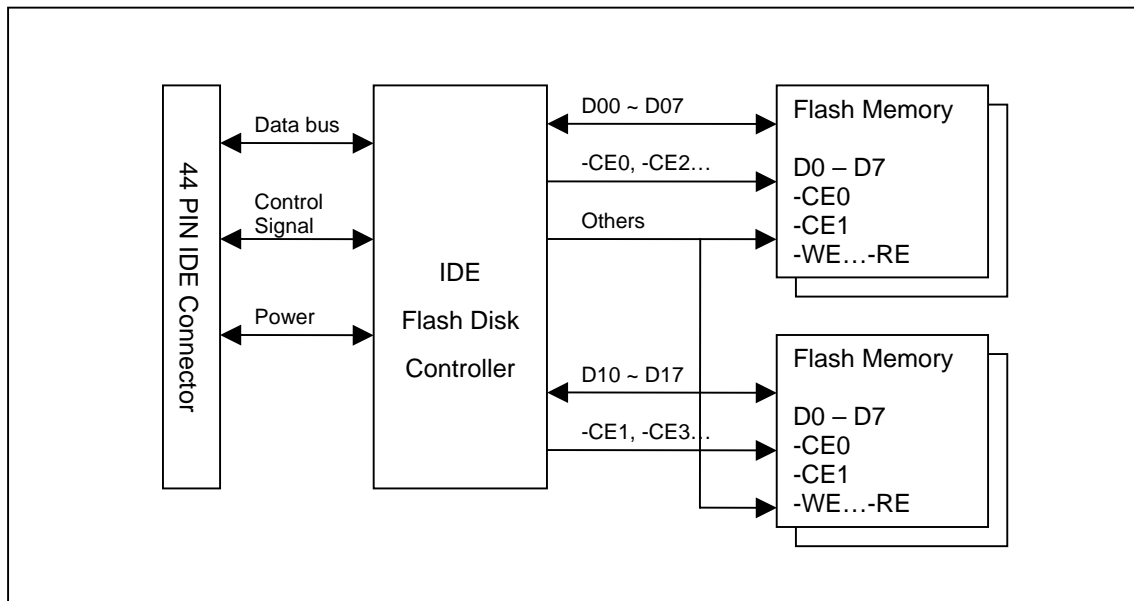
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35, 33, 36	DA0 ~ DA2 (Device Address)	I	This is the 3-bit binary coded Address Bus.
34	-PDIAG (Passed diagnostics)	I/O	This signal will be asserted by Device 1 to indicate to Device 0 that Device 1 has completed diagnostics.
	-CBLID (Cable assembly type identifier)		
37, 38	-CS0, -CS1 (Chip select)	I	These signals are used to select the Command Block and Control Block registers. When -DMACK is asserted, -CS0 and -CS1 shall be negated and transfers shall be 16-bit wide.
39	-DASP (Device active, Device 1 present)	I/O	During the reset protocol, -DASP shall be asserted by Device 1 to indicate that the device is present.
41, 42	VCC	P	Power supply.
2, 19, 22, 24, 26, 30, 40, 43	GND	-	Ground.

* Note:

- “I” An input from the host system to the device.
- “O” An output from the device to the host system.
- “I/O” An input/output (bi-direction) common.
- “P” Power supply.

Block Diagram



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Command Set

The following table summarizes the command defined in the ATAPI-5 specification and lists the commands supported by the TS128M-4GDOM44H.

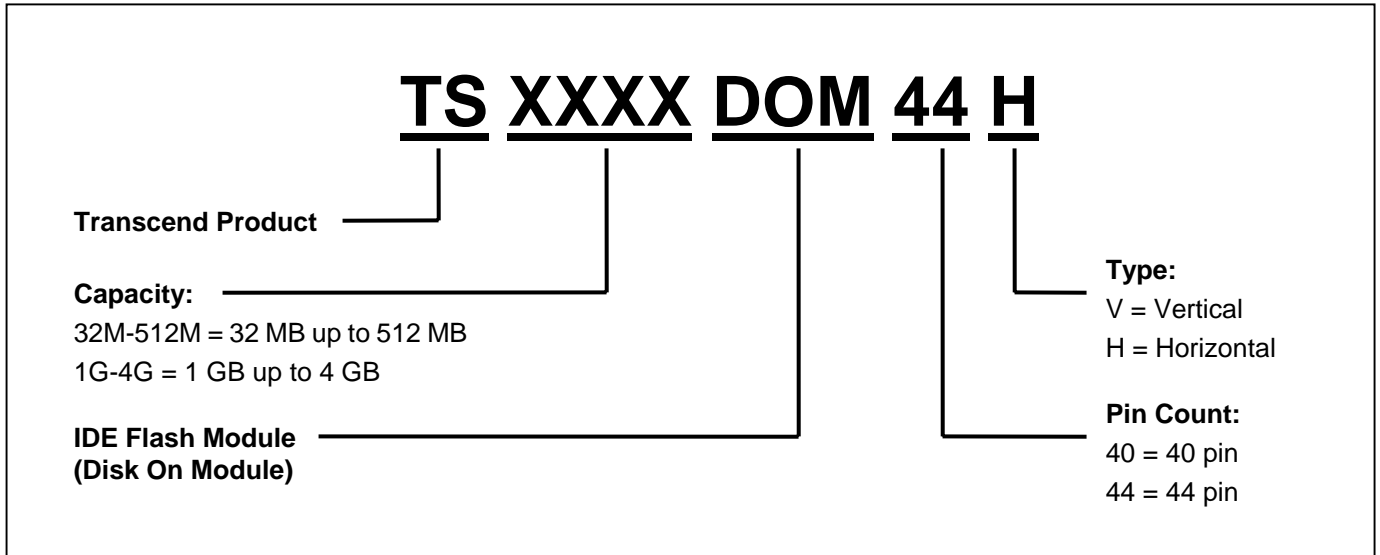
No.	Command set	Code	FR ¹	SC ¹	SN ¹	CY ¹	DR ¹	HD ¹	LBA ¹
1	CFA Erase Sector(s)	C0h	—	Y	Y	Y	Y	Y	Y
2	CFA Request Extended Error Code	03h	—	—	—	—	Y	—	—
3	CFA Translate Sector	87h	—	Y	Y	Y	Y	Y	Y
4	CFA Write Multiple w/o Erase	CDh	—	Y	Y	Y	Y	Y	Y
5	CFA Write Sector w/o Erase	38h	—	Y	Y	Y	Y	Y	Y
6	Check Power Mode	E5h	—	—	—	—	Y	—	—
7	Execute Device Diagnostic	90h	—	—	—	—	Y	—	—
8	Identify Device	ECh	—	—	—	—	Y	—	—
9	Idle	E3h	—	Y	—	—	Y	—	—
10	Idle Immediate	E1h	—	—	—	—	Y	—	—
11	Initialize Device Parameters	91h	—	Y	—	—	Y	Y	—
12	NOP	00h	—	—	—	—	Y	—	—
13	Read Buffer	E4h	—	—	—	—	Y	—	—
14	Read DMA	C8h	—	Y	Y	Y	Y	Y	Y
15	Read Multiple	C4h	—	Y	Y	Y	Y	Y	Y
16	Read Sector(s)	20h	—	Y	Y	Y	Y	Y	Y
17	Read Verify Sector(s)	40h	—	Y	Y	Y	Y	Y	Y
18	Seek	70h	—	—	Y	Y	Y	Y	Y
19	Set Features	EFh	Y	C	—	—	Y	—	—
20	Set Multiple Mode	C6H	—	Y	—	—	Y	—	—
21	Sleep	E6h	—	—	—	—	Y	—	—
22	Standby	E2h	—	—	—	—	Y	—	—
23	Standby Immediate	E0h	—	—	—	—	Y	—	—
24	Write Buffer	E8h	—	—	—	—	Y	—	—
25	Write DMA	CAh	—	Y	Y	Y	Y	Y	Y
26	Write Multiple	C5h	—	Y	Y	Y	Y	Y	Y
27	Write Sector	30h	—	Y	Y	Y	Y	Y	Y

Note 1: **FR** (Feature Register), **SC** (Sector Count Register), **SN** (Sector Number Register), **CY** (Cylinder Low/High Register), **DR** (Drive bit of Drive/Head Register), **HD** (Head No. bit0-bit3 of Drive/Head Register), **LBA** (Logical Block Address Mode supported). **Y**: Set up; **—**: Not set up; **C**: The register contains command specific data.


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Ordering Information



The above technical information is based on industry standard data and has been tested to be reliable. However, Transcend makes no warranty, either expressed or implied, as to its accuracy and assumes no liability in connection with the use of this product. Transcend reserves the right to make changes to the specifications at any time without prior notice.

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