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FUJITSU

DATA SHEET

MB88351

R-2R TYPE 12-BIT D/A CONVERTER WITH OPERATIONAL AMPLIFIER OUTPUT BUFFERS

PRELIMINARY

DESCRIPTION

The Fujitsu MB88351 is an R-2R type 12-bit resolution digital-to-analog converter (DAC), designed for interface with a wide range of general 4-bit and 8-bit microcontrollers including Fujitsu's MB88200 family, MB8850 family, and MB88500 family 4-bit single-chip microcontrollers.

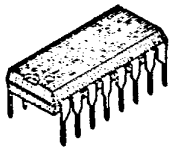
The MB88351 has an 12-bit x 4-channel D/A converter with operational amplifier output buffers. Digital data are input serially by individual channel units. The loaded digital data are converted into analog DC voltages by the D/A converter in maximum 30 µs settling time. Also, the MB88351 has operational amplifier output buffers. These operational amplifier output buffers are connected to each channel of the D/A converter, and provide high current drive capability. The MB88351 is suitable for electronic volumes and replacement for potentiometers for adjustment, in addition to normal D/A converter applications.

FEATURES

- Conversion method : R-2R resistor ladder
- 12-bit x 4-channel D/A converter with operational amplifier output buffers
- Max. 2.5MHz Serial data input
- Serial data output for cascade connection
- Max. 30 µs DAC output settling time
- Max. +1.0/-1.0 mA analog output sink/source current
- Two separate power supply/ground lines for MCU interface block/operational amplifier output buffer block and D/A converter block
- Pin compatible with MB88353
- Low power dissipation : Typ. 1.5mW/channel
- Single +5V power supply
- Wide operating temperature range: -20°C to +85°C
- Silicon-gate CMOS process
- Three package options :

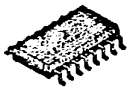
  16-pin plastic DIP (Suffix : -P), 16-pin plastic SOP (Suffix : -PF),
  20-pin plastic SSOP (Suffix : -PFV)

MB88351-P



PLASTIC DIP
(DIP-16P-M04)

MB88351-PF



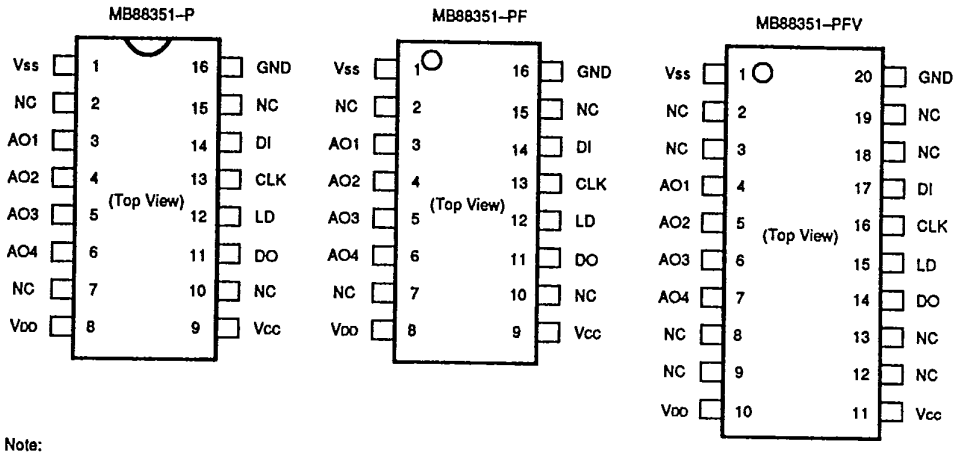
PLASTIC SOP
(FPT-16P-M06)

MB88351-PFV

PLASTIC SSOP
(FPT-20P-M03)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Figure 1 Pin Assignment



Note:

NC : No connection

Figure 2 Logic Symbol

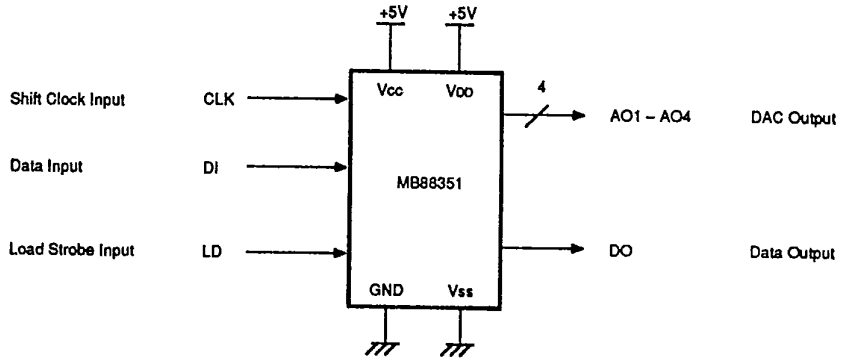
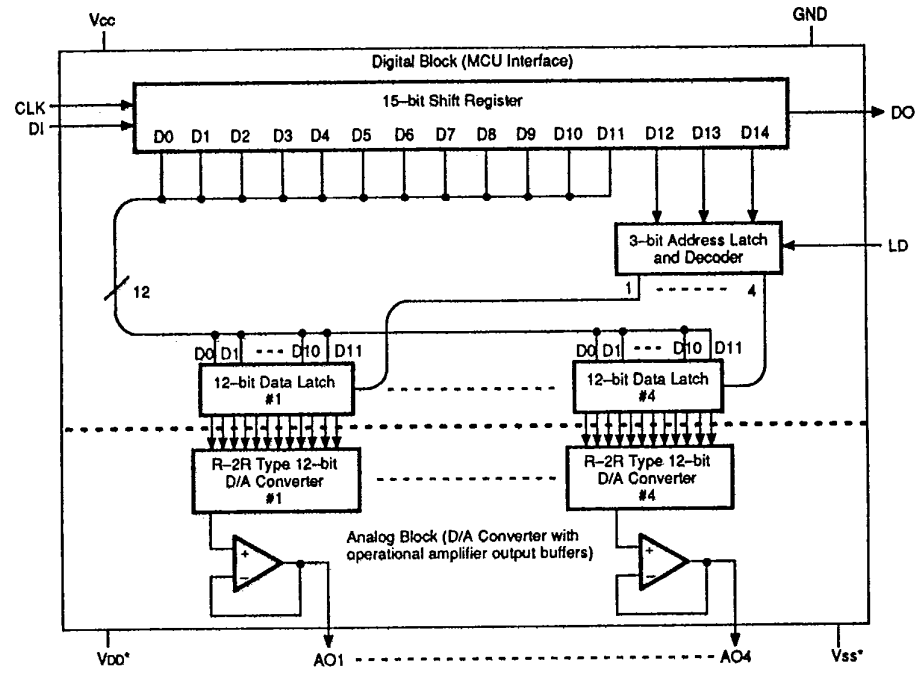


Figure 3 Block Diagram



* : Only for D/A converter block except operational amplifier block

PIN DESCRIPTION

Figure 1 and Table 1 show the pin assignment and pin description of the MB88351.

Table 1 Pin Description

Symbol	Pin No.		Type	Name & Function
	DIP/SOP	SSOP		
Power Supply				
Vcc	9	11	–	+5V DC power supply pin for the digital block (MCU interface) and operational amplifier output buffers.
GND	16	20	–	Ground pin for the digital block (MCU interface) and operational amplifier output buffers.
VDD	8	10	–	DC power supply pin for the analog block (D/A converter) except operational amplifier output buffers.
Vss	1	1	–	Ground pin for the analog block (D/A converter) except operational amplifier output buffers.
Control Input				
CLK	13	16	I	Shift clock input to the internal 15–bit shift register: At the rising edge of CLK data on the DI pin is shifted into the LSB of the shift register and contents of the shift register are shifted right (to the MSB).
LD	12	15	I	Load strobe input for a 15–bit address/data : A high level on the LD pin latches a 3–bit address (upper 3 bits: D14 to D12) of the internal 15–bit shift register into the internal address latch/decoder, and writes 12–bit data (lower 12 bits: D11 to D0) of the shift register into an internal data latch selected by the latched address.
Data Input/Output				
DI	14	17	I	Serial address/data input to the internal 15–bit shift register: The address/data format is that upper 3 bits (D14 to D12) indicate an address and lower 12 bits (D11 to D0) indicate data. The D14 (MSB) is the first–in bit and D0 (LSB) is the last–in bit.
DO	11	14	O	Serial address/data output from the internal 15–bit shift register: This is an output pin of the MSB bit data of the 15–bit shift register. This pin allows a cascade connection of the device.
DAC Output				
AO1 AO2 AO3 AO4	3 4 5 6	4 5 6 7	O	12–bit resolution D/A converter outputs : 4 channels (AO1 to AO4) of DAC outputs are provided. Each output channel has an operational amplifier output buffer for analog output data.
Others				
NC	2, 7, 10, 15	2, 3, 8, 9, 12, 13, 18, 19	–	No connection. They must be left open.

FUNCTIONAL DESCRIPTION

OVERVIEW

The MB88351 is an R–2R resistor ladder type, 12–bit resolution digital–to–analog converter (DAC) device. The MB88351 has 4 channels of D/A converters with operational amplifier output buffers. 12–bit digital data are loaded into internal data latches by individual DAC channel units. The loaded digital data are converted into analog DC voltages through the internal D/A converter in max. 30 µs settling time. And the analog DC voltages source/sink the output current through the operational amplifier output buffers. For cascade connection, a serial data output is provided.

DEVICE CONFIGURATION

As illustrated in Figure 3 block diagram, the MB88351 device is composed by the digital block (MCU interface) and analog block (D/A converter with operational amplifier output buffers). The digital block consists of a 15–bit shift register, a 3–bit address latch/decoder, and 4 channels of 12–bit data latches. The analog block includes 4 channels of 12–bit D/A converters with operational amplifier output buffers connecting to the data latches. For electrically stable operation the power supply and ground lines are separate between the digital block (MCU interface) and operational amplifier output buffers, and analog block except operational amplifier output buffers.

DEVICE OPERATION

Figure 4 shows the input/output timing. A 15–bit address/data is serially input into the shift register through the DI pin synchronously with the rising edge of CLK. The format of the shift register is shown in Figure 5. The lower 12 bits (D11 to D0) are data bits to be converted, and the upper 3 bits are address bits (D14 to D12) to select a data latch to be written. A high level on the LD pin loads the address latch/decoder with the 3–bit address to select a data latch, and writes the 12–bit data into a selected data latch. Figure 6 shows the data latch address map, and Table 2 lists the address decoding. 12–bit data written into individual data latches are converted into analog DC voltages, dividing the supply voltage |V_{DD}–V_{SS}| through R–2R resistor ladders of D/A converters. The operational amplifier output buffers at individual D/A converter outputs can source up to 1 mA of the output current. Figure 7 shows a configuration of the R–2R resistor ladder D/A converter with operational amplifier, and Table 3 lists the analog DC voltages corresponding to each digital data.

Figure 4 Input/Output Timing

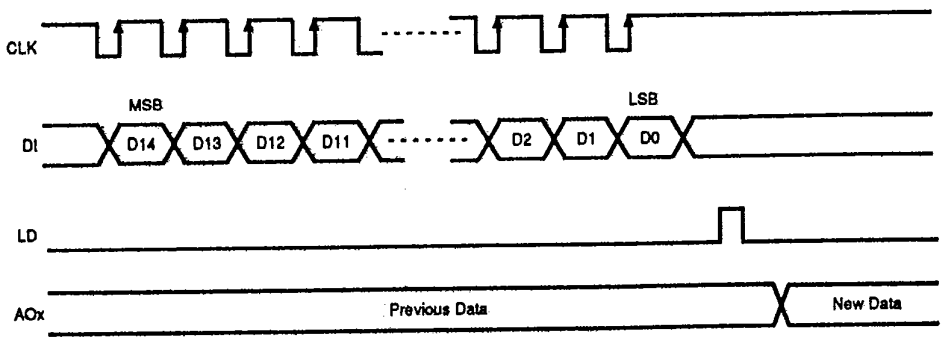


Figure 5 Shift Register Format

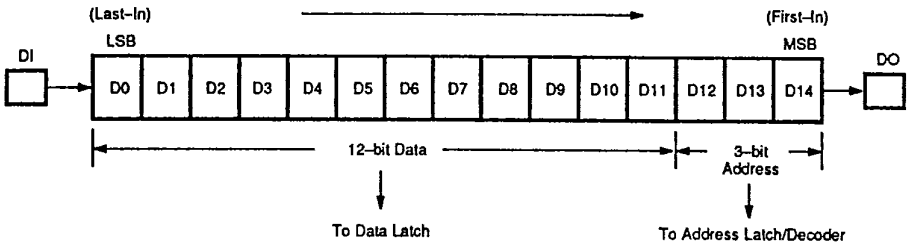


Figure 6 Data Latch Address Map

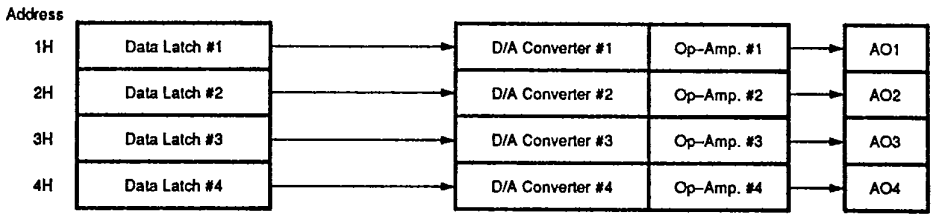
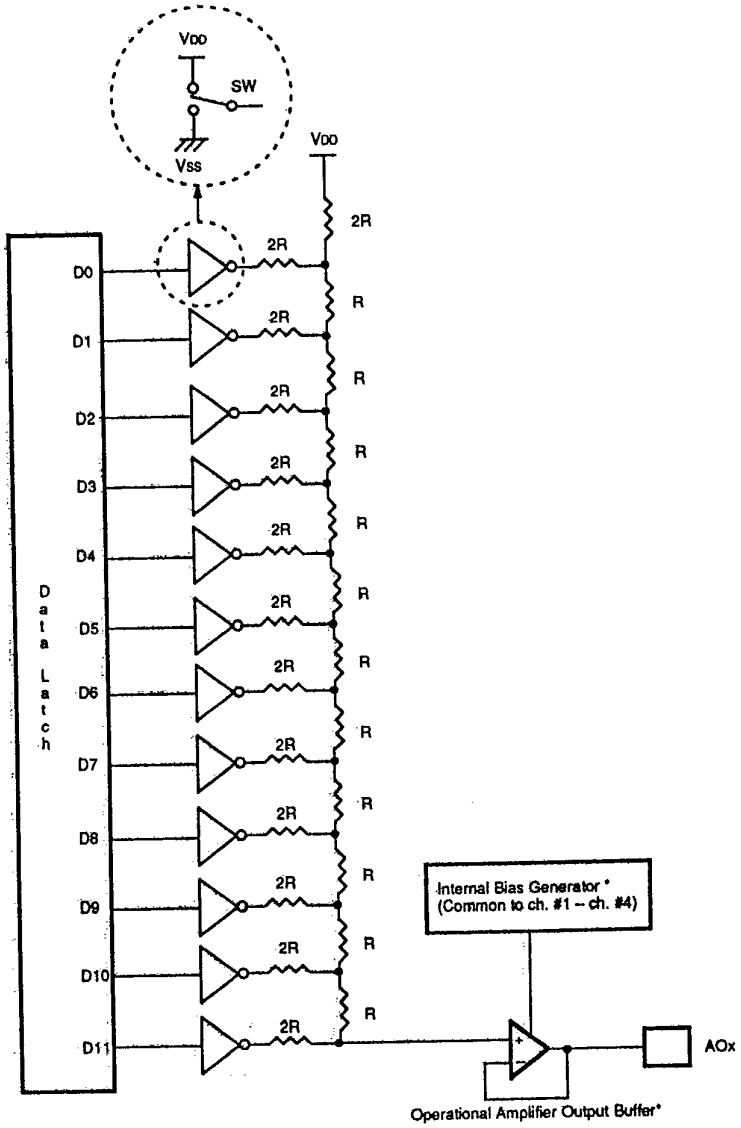


Figure 7 Configuration of R–2R Resistor Ladder D/A Converter with Operational Amplifier Output Buffer



*: Powered/grounded by the Vcc and GND pins.

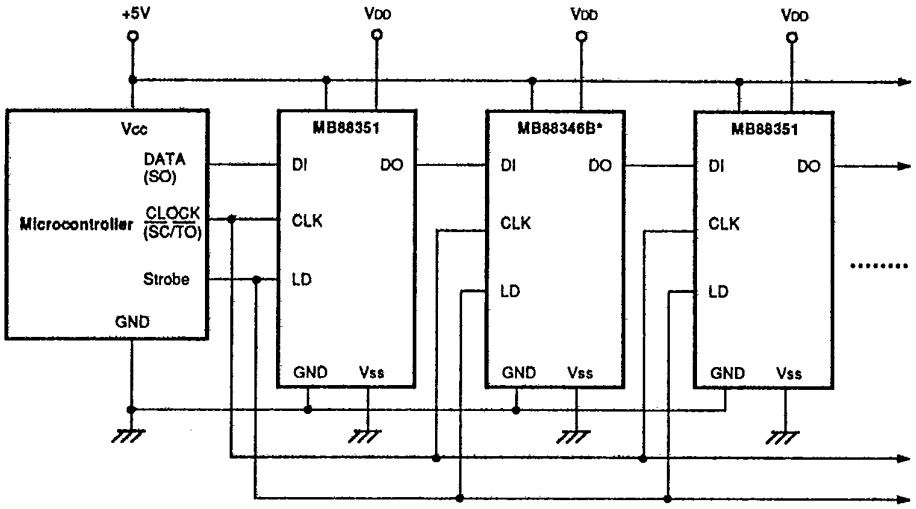
Table 2 Address Decoding

Address			Data Latch Selected
D12	D13	D14	MB88351
0	0	0	Deselected
0	0	1	Data Latch #1
0	1	0	Data Latch #2
0	1	1	Data Latch #3
1	0	0	Data Latch #4
1	0	1	Deselected
1	1	0	Deselected
1	1	1	Deselected

Table 3 Data Conversion

Data												DAC Output Level
D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	AOx
0	0	0	0	0	0	0	0	0	0	0	0	≈ Vss
0	0	0	0	0	0	0	0	0	0	0	1	≈ (VDD – Vss) x 1/4095 + Vss
0	0	0	0	0	0	0	0	0	0	1	0	≈ (VDD – Vss) x 2/4095 + Vss
0	0	0	0	0	0	0	0	0	0	1	1	≈ (VDD – Vss) x 3/4095 + Vss
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	1	1	1	1	0	0	≈ (VDD–Vss) x 4092/4095+Vss
1	1	1	1	1	1	1	1	1	1	0	1	≈ (VDD–Vss) x 4093/4095+Vss
1	1	1	1	1	1	1	1	1	1	1	0	≈ (VDD–Vss) x 4094/4095+Vss
1	1	1	1	1	1	1	1	1	1	1	1	≈ VDD

Figure 8 Cascade Connection Example

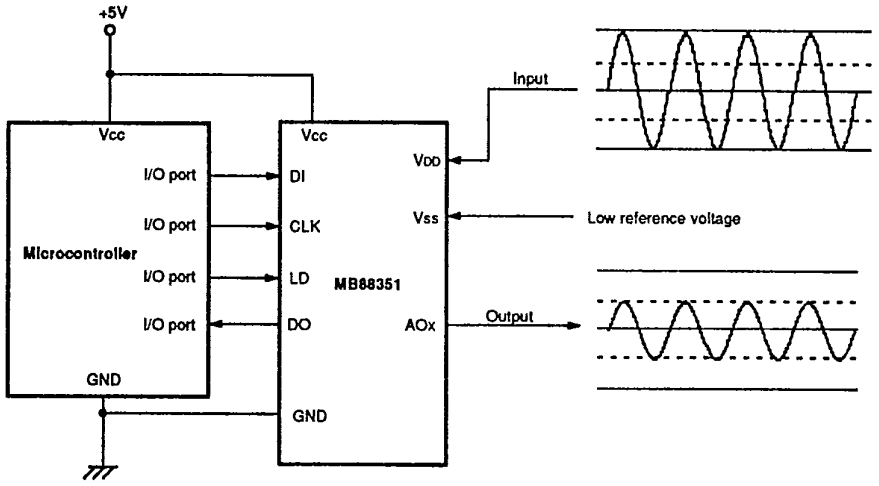


* : MB88351 can be used mixed with MB88346B.

APPLICATION DESCRIPTION

The MB88351 is suitable for electronic volumes and replacement for adjustment potentiometers, in addition to normal D/A converter applications. Figure 9 illustrates application example for a gain control.

Figure 9 Application Example – Gain Control



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Parameter	Symbol	Rating			Unit	Condition
		Min	Typ	Max		
Supply Voltage	V_{CC}	−0.3		7.0	V	Ta = +25°C GND = 0 V $V_{DD} \leq V_{CC}$
	V_{DD}	−0.3		7.0	V	
Input Voltage	V_{IN}	−0.3		Vcc+0.3	V	Ta = 25°C GND = 0 V Should not exceed Vcc + 0.3V
Output Voltage	V_{OUT}	−0.3		Vcc+0.3	V	
Power Dissipation	P_D			250	mW	
Operating Ambient Temperature	T_A	−20		+85	°C	
Storage Temperature	T_{STG}	−55		+150	°C	

NOTE : Permanent device damage may occur if the above ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Condition
		Min	Typ	Max		
Supply Voltage (for MCU Interface/ Op.-Amp. Block)	V_{CC}	4.5	5.0	5.5	V	$V_{CC} \geq V_{DD}$
	GND		0		V	
Supply Voltage (for Analog Block*)	V_{DD}	2.0		Vcc	V	$V_{CC} \geq V_{DD}$, $V_{DD}-V_{SS} \geq 2.0V$
	V_{SS}	GND		Vcc−2.0	V	
Analog Output Source Current	I_{AL1}			−1.0	mA	
Analog Output Sink Current	I_{AL2}			+1.0	mA	
Analog Output Load Capacitance for oscillation limit	C_{AL}			1.0	µF	
Operating Ambient Temperature	T_A	−20		+85	°C	

* : Except operational amplifier output buffer block

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Digital Block (MCU Interface)

Parameter	Symbol	Value			Unit	Condition
		Min	Typ.	Max		
Active Supply Current (Vcc) *	Icc		1.0	2.5	mA	CLK = 1MHz, Unloaded
Input Leakage Current (CLK, DI, and LD)	I_{ILK}	−10		+10	µA	V_{IN} = 0 to Vcc
Input Low Voltage (CLK, DI, and LD)	V_{IL}			0.2•Vcc	V	
Input High Voltage (CLK, DI, and LD)	V_{IH}	0.8•Vcc			V	
Output Low Voltage (DO)	V_{OL}			0.4	V	I_{OL} = 2.5 mA
Output High Voltage (DO)	V_{OH}	Vcc−0.4			V	I_{OH} = −400 µA

* : Including the supply current to the operational amplifier block

Analog Block (D/A Converters with Operational Amplifier Output Buffers)

Parameter	Symbol	Value			Unit	Condition
		Min	Typ	Max		
Supply Current (V_{DD}) **	I_{DD}		0.1	0.3	mA	Unloaded
Analog Supply Voltage (V_{DD}, Vss)	V_{DD}	2.0		Vcc	V	V_{DD}−Vss≥2.0V
	Vss	GND		Vcc−2.0	V	
Resolution (AOx)	Res		12		bit	
Monotonicity (AOx)	Rem		10		bit	Unloaded
Offset Error (AOx)***	Eo	−0.1	0	+0.1	V	Unloaded
Nonlinearity Error (AOx)	E_{NL}	−8.0	0	+8.0	LSB	Unloaded, V_{DD}≤Vcc−0.1V, Vss≥0.1V See Figure 10.

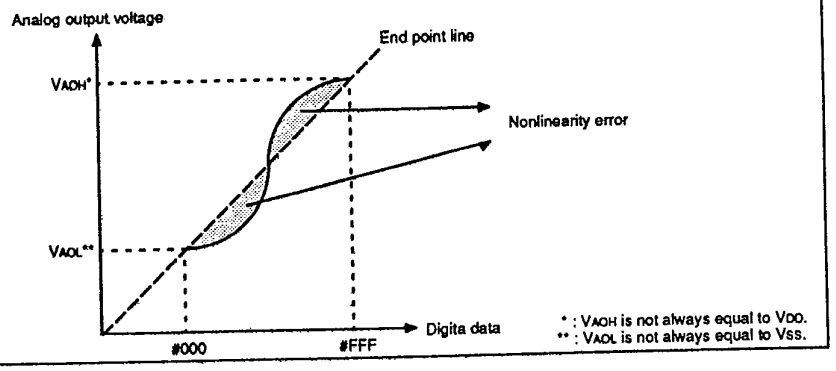
** : Excluding the supply current to the operational amplifier block

Analog Block (D/A Converters with Operational Amplifier Output Buffers) – Continued

Parameter	Symbol	Value			Unit	Condition
		Min	Typ	Max		
Min. Analog Output Voltage 1 (AOx)	V_{AOL1}	GND		GND+0.1	V	Unloaded, Vss = 0V, Digital data=#000
Min. Analog Output Voltage 2 (AOx)	V_{AOL2}	GND–0.1	GND	GND+0.1	V	V_{DD}=Vcc=5.0V, Vss=GND=0V, I_{AL1}=–400µA, Digital data=#000
Min. Analog Output Voltage 3 (AOx)	V_{AOL3}	GND–0.3	GND	GND+0.3	V	V_{DD}=Vcc=5.0V, Vss=GND=0V, I_{AL1}=–1.0mA, Digital data=#000
Min. Analog Output Voltage 4 (AOx)	V_{AOL4}	GND		GND+0.1	V	V_{DD}=Vcc=5.0V, Vss=GND=0V, I_{AL2}=+400µA, Digital data=#000
Min. Analog Output Voltage 5 (AOx)	V_{AOL5}	GND		GND+0.3	V	V_{DD}=Vcc=5.0V, Vss=GND=0V, I_{AL2}=+1.0mA, Digital data=#000
Max. Analog Output Voltage 1 (AOx)	V_{AOH1}	Vcc–0.1		Vcc	V	Unloaded, V_{DD} = Vcc, Digital data=#FFF
Max. Analog Output Voltage 2 (AOx)	V_{AOH2}	Vcc–0.1		Vcc	V	V_{DD}=Vcc=5.0V, Vss=GND=0V, I_{AL1}=–400µA, Digital data=#FFF
Max. Analog Output Voltage 3 (AOx)	V_{AOH3}	Vcc–0.3		Vcc	V	V_{DD}=Vcc=5.0V, Vss=GND=0V, I_{AL1}=–1.0mA, Digital data=#FFF
Max. Analog Output Voltage 4 (AOx)	V_{AOH4}	Vcc–0.1	Vcc	Vcc+0.1	V	V_{DD}=Vcc=5.0V, Vss=GND=0V, I_{AL2}=+400µA, Digital data=#FFF
Max. Analog Output Voltage 5 (AOx)	V_{AOH5}	Vcc–0.3	Vcc	Vcc+0.3	V	V_{DD}=Vcc=5.0V, Vss=GND=0V, I_{AL2}=+1.0mA, Digital data=#FFF

** : Excluding the supply current to the operational amplifier block

Figure 10 Definition of Nonlinearity Error



AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Value		Unit	Condition
		Min	Max		
Clock Low Time	t_{CKL}	200		ns	
Clock High Time	t_{CKH}	200		ns	
Clock Rise Time	t_{Cr}		200	ns	
Clock Fall Time	t_{Cf}		200	ns	
Data Setup Time	t_{DCH}	30		ns	
Data Hold Time	t_{CHD}	60		ns	
Load Strobe High Time	t_{LDH}	100		ns	
Load Strobe Setup Time	t_{CHL}	200		ns	
Load Strobe Hold Time	t_{LDC}	100		ns	
DAC Output Settling Time	t_{LDO}		30	µs	*R_{AL} = 10 kΩ, C_{AL} = 50 pF
Data Output Delay Time	t_{DO}	70	350	ns	**C_L = 20 pF (Min.), 100 pF (Max.)

Figure 11 AC Test Conditions

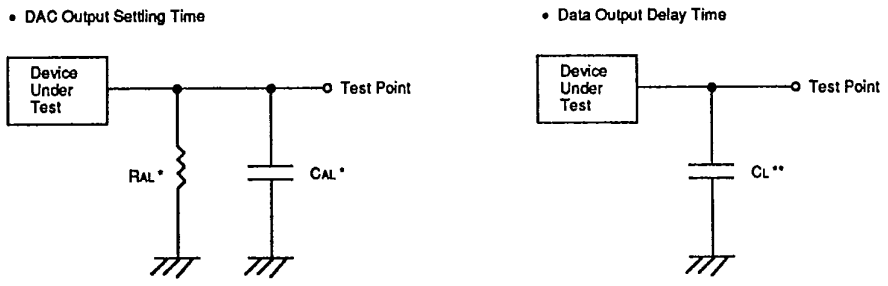


Figure 12 Input/Output Timing

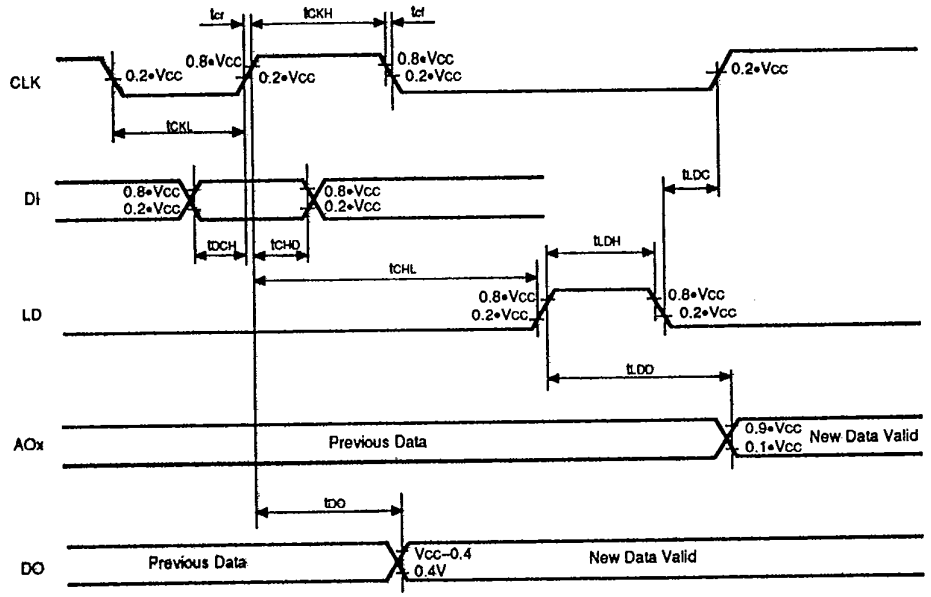
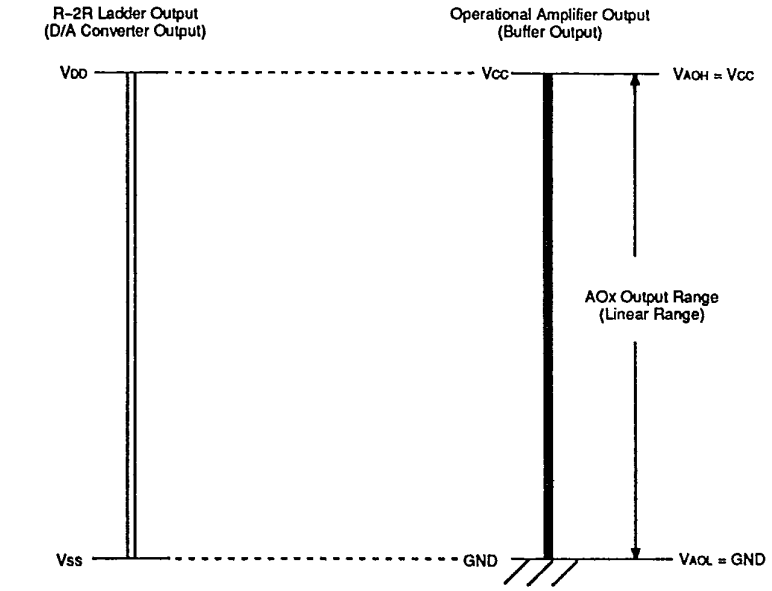
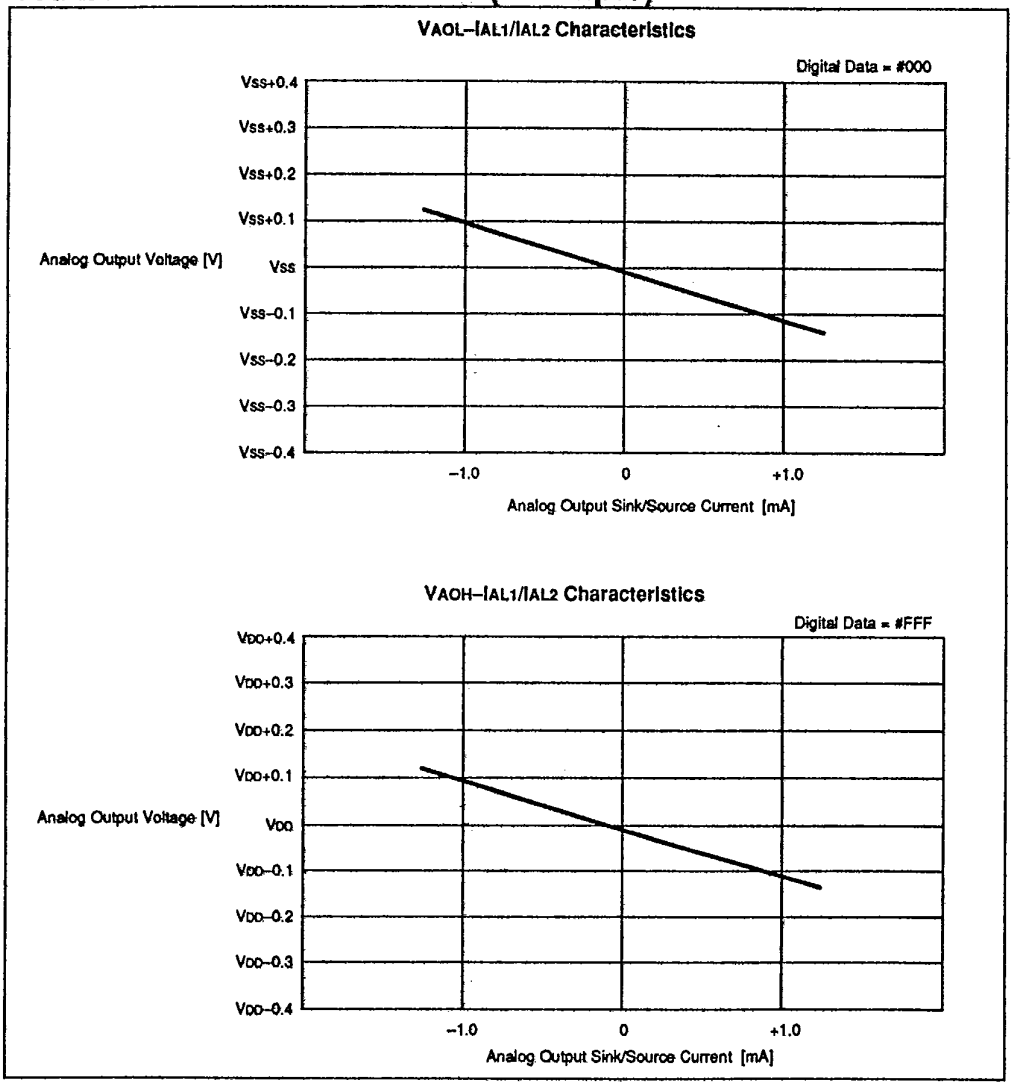


Figure 13 Analog Output Voltage Range



Notes: V_{DD}=V_{CC}
V_{SS}=GND

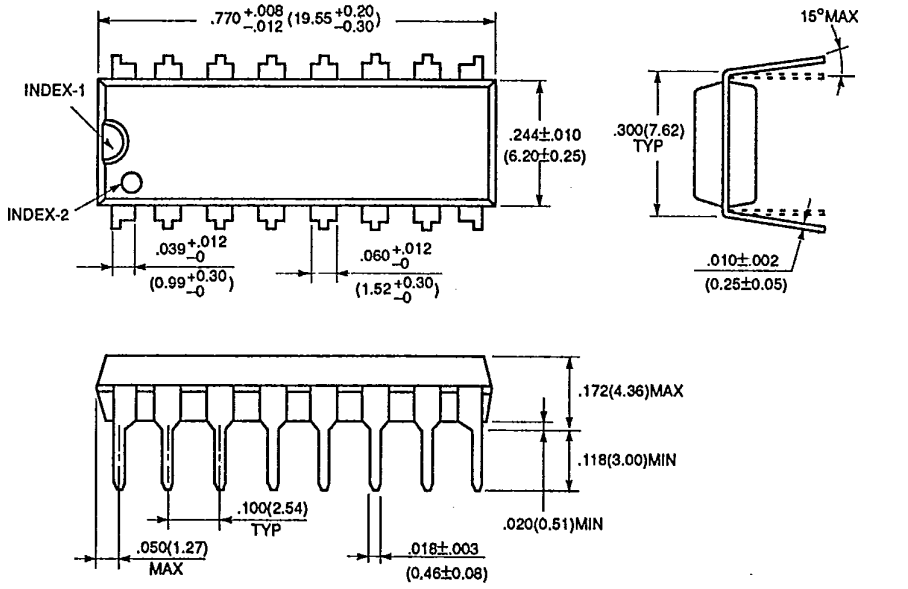
CHARACTERISTICS CURVE (Example)



PACKAGE DIMENSIONS

MB88351-P

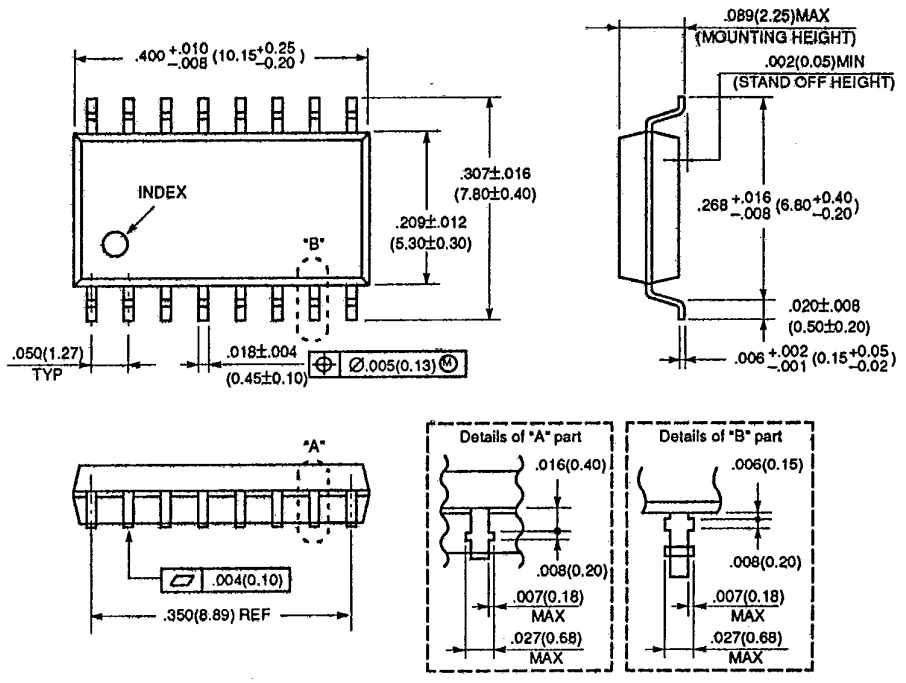
16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M04)



Dimensions in inches (millimeters)

MB88351-PF

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M06)

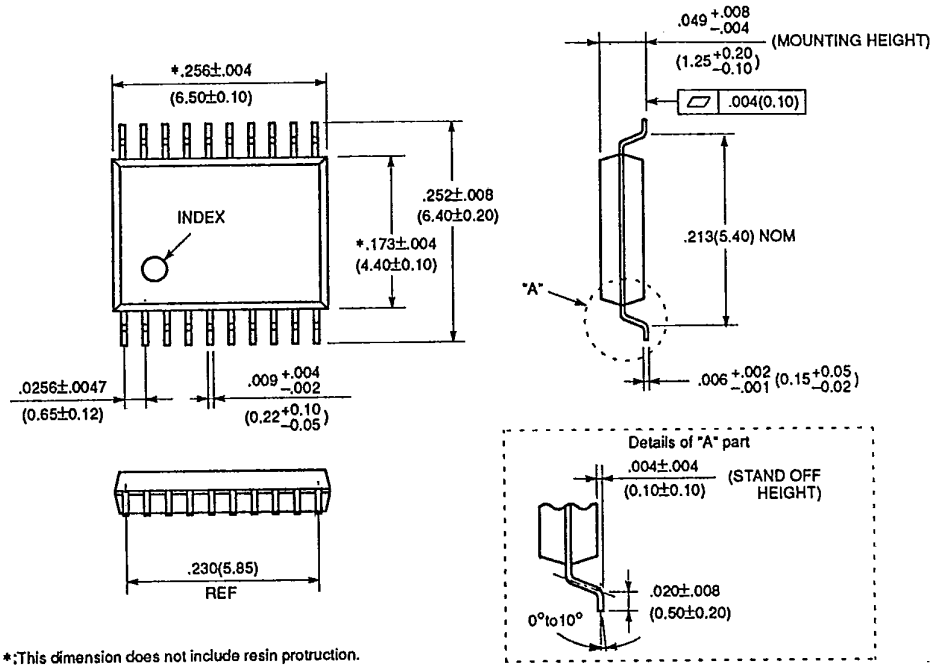


Dimensions in
inches (millimeters)

MB88351

MB88351-PFV

20-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-20P-M03)



*:This dimension does not include resin protruction.

Dimensions in inches (millimeters)