FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-13501-3E

Linear IC General purpose Converter

CMOS

D/A Converter for Digital Tuning

(12 channels. 8-bit, with OP amplifier)

MB88346B

■ DESCRIPTION

The MB88346B features 12 channels of 8-bit D/A converters with output amplifier for digital tuning. The output amplifier provides high current drive capability.

As the MB88346B inputs data in serial, it requires only three control lines and can also be cascade-connected with the MB88340 series.

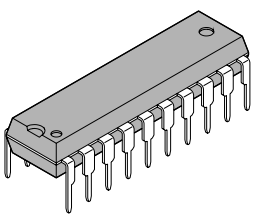
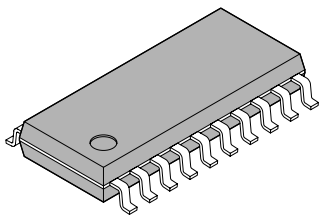
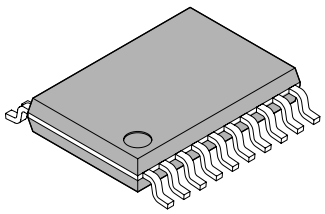
The MB88346B is suitable for electronic volumes and replacement for potentiometers for adjustment, in addition to normal D/A converter applications.

■ FEATURES

- Low power consumption
- Small package
- Integrating 12 channels of R-2R type 8-bit D/A converter

(Continued)

■ PACKAGES

20-pin plastic DIP	20-pin plastic SOP	20-pin plastic SSOP
		
(DIP-20P-M02)	(FPT-20P-M01)	(FPT-20P-M03)

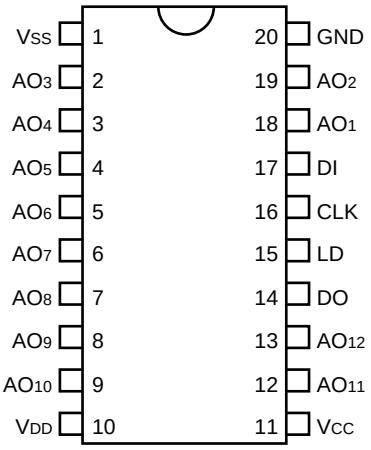
FUJITSU

(Continued)

- Built-in analog output amplifier (Max +1.0 mA sink/source current)
- Analog output range : 0 to V_{CC}
- The range of D/A conversion can be independently set by separated the power supply for MCU interface and OP amplifier and the power supply for D/A converter.
- Capable of being controlled directly by a 3-V MCU (input voltage : “H” = 0.5 V_{CC}, “L” = 0.2 V_{CC})
- Serial data input, 2.5 MHz operation
- CMOS process
- Package lineup : DIP 20-pin, SOP 20-pin, SSOP 20-pin

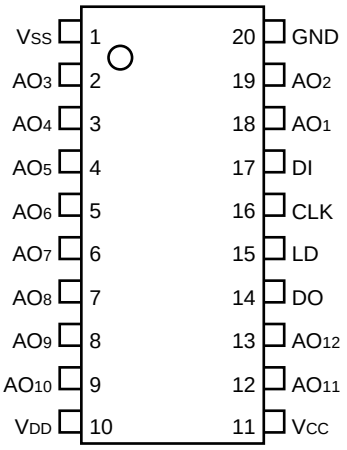
■ PIN ASSIGNMENTS

(TOP VIEW)



(DIP-20P-M02)

(TOP VIEW)



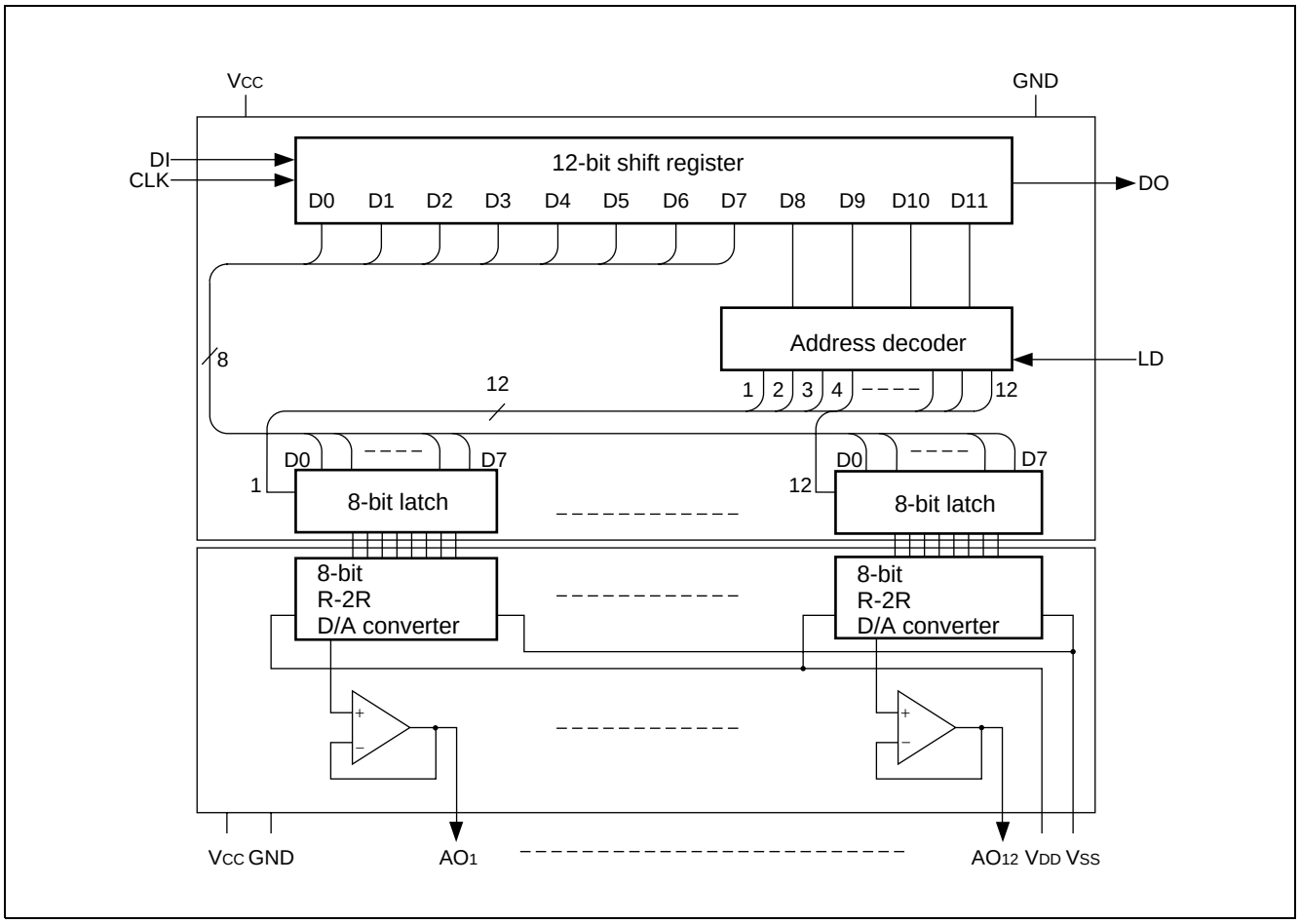
(FPT-20P-M01)
(FPT-20P-M03)

■ PIN DESCRIPTION

Pin No.	Symbol	I/O	Pin name	Function
17	DI*	I	Data input pin	This pin inputs 12-bit serial data.
14	DO	O	Data output pin	This pin outputs MSB bit data of 12-bit shift register.
16	CLK*	I	Shift clock input pin	Input signal from DI pin is inputted to 12-bit shift register at rising of shift clock.
15	LD*	I	Load signal input pin	If input “H” level to LD pin, the data of 12-bit shift register is loaded to the decoder and the register for D/A output.
18, 19, 2, 3, 4, 5, 6, 7, 8, 9, 12, 13	AO_1, AO_2, AO_3, AO_4, AO_5, AO_6, AO_7, AO_8, AO_9, AO_{10}, AO_{11}, AO_{12}	O	D/A output pin	These pins output analog data of 8-bit D/A converter with OP amplifier.
11	V_{CC}	—	Power supply pin	Power supply pin of MCU interface and OP amplifier
20	GND	—	Ground pin	Ground pin of MCU interface and OP amplifier
10	V_{DD}	—	Power supply pin	Power supply pin of D/A converter
1	V_{SS}	—	Ground pin	Ground pin of D/A converter

* : When three pins, DI, CLK, and LD pins are connected to 3-V MCU, they are fixed to “L” level at non transfer.

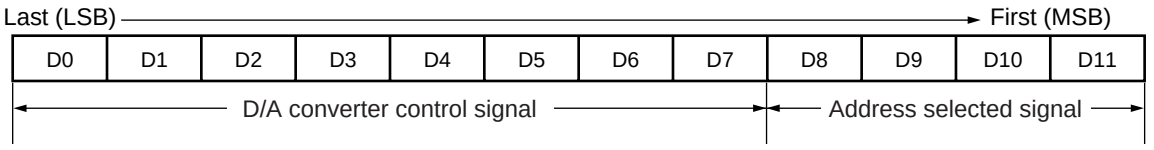
■ BLOCK DIAGRAM



■ DATA FOR CHIP CONTROL

1. Data for Shift Register

- The chip is controlled by 12 bits of data input to the shift register.
- The shift register inputs a total of 12 bits of data consisting of a four-bit address selection signal and an eight-bit D/A converter control signal.
- A data to the shift register is inputted to the DI pin in the order of D11 (MSB) to D0 (LSB) .



2. D/A Converter Control Signal

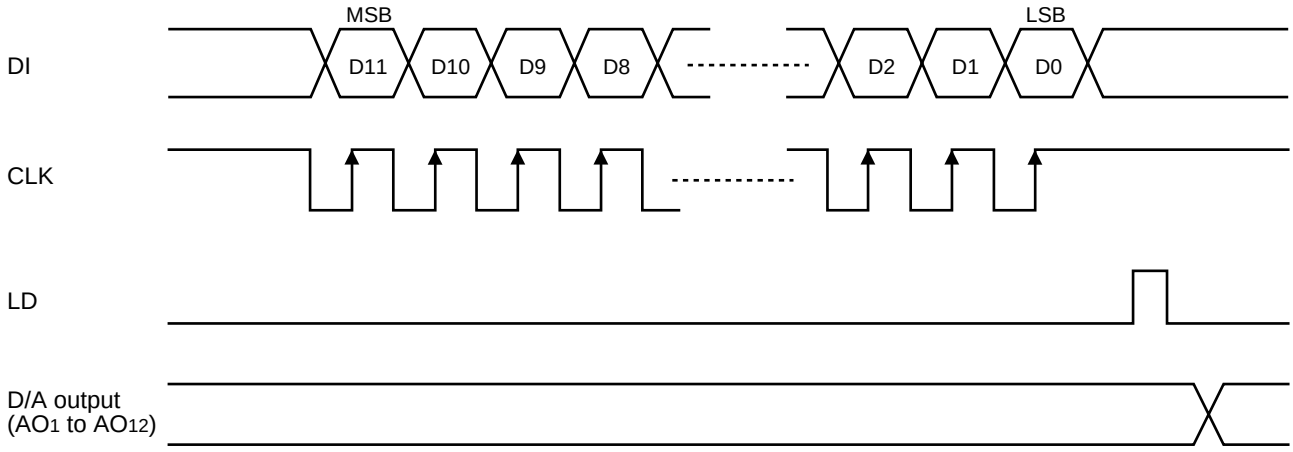
Input data signal								D/A converter output voltage
D0	D1	D2	D3	D4	D5	D6	D7	
0	0	0	0	0	0	0	0	≅ V_{SS}
1	0	0	0	0	0	0	0	≅ V_{REF} / 255 × 1 + V_{SS}
0	1	0	0	0	0	0	0	≅ V_{REF} / 255 × 2 + V_{SS}
1	1	0	0	0	0	0	0	≅ V_{REF} / 255 × 3 + V_{SS}
⧵	⧵	⧵	⧵	⧵	⧵	⧵	⧵	⧵
0	1	1	1	1	1	1	1	≅ V_{REF} / 255 × 254 + V_{SS}
1	1	1	1	1	1	1	1	≅ V_{DD}

$V_{REF} = V_{DD} - V_{SS}$

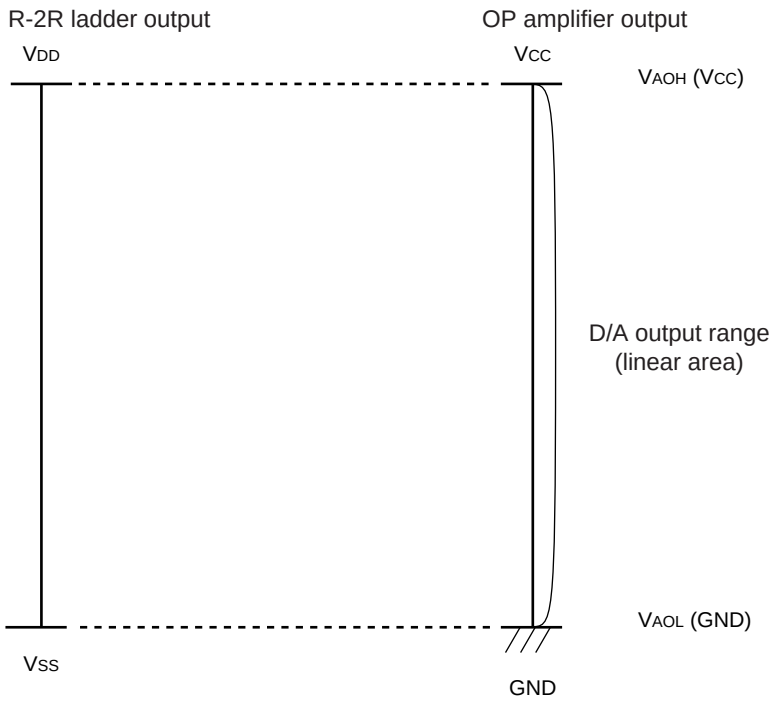
3. Address Selected Signal

Input data signal				Address selected sequence
D8	D9	D10	D11	
0	0	0	0	Don't Care
0	0	0	1	AO_1 selected
0	0	1	0	AO_2 selected
0	0	1	1	AO_3 selected
0	1	0	0	AO_4 selected
0	1	0	1	AO_5 selected
0	1	1	0	AO_6 selected
0	1	1	1	AO_7 selected
1	0	0	0	AO_8 selected
1	0	0	1	AO_9 selected
1	0	1	0	AO_{10} selected
1	0	1	1	AO_{11} selected
1	1	0	0	AO_{12} selected
1	1	0	1	Don't Care
1	1	1	0	Don't Care
1	1	1	1	Don't Care

■ TIMING CHART AT DATA SETTING



■ ANALOG OUTPUT VOLTAGE RANGE



Note : $V_{CC} = V_{DD}$, GND = V_{SS}

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating		Unit	Remarks
			Min	Max		
Power supply voltage	V_{CC}	The case that GND is referred. Ta = +25 °C	− 0.3	+ 7.0	V	
	V_{DD}		− 0.3	+ 7.0	V	$V_{CC} \geq V_{DD}$
Input voltage	V_{IN}		− 0.3	V_{CC} + 0.3	V	
Output voltage	V_{OUT}		− 0.3	V_{CC} + 0.3	V	
Power consumption	P_D	—	—	250	mW	
Operating temperature	Ta	—	− 40	+ 85	°C	
Storage temperature	Tstg	—	− 55	+ 150	°C	

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value		Unit
		Min	Max	
Power supply Voltage	V_{CC}	4.5	5.5	V
	GND	—	0	V
Analog output source current	I_{source}	—	1.0	mA
Analog output sink current	I_{sink}	—	1.0	mA
Oscillation limited output capacitance	C_{OL}	—	1.0	µF
Operating temperature	Ta	− 40	+ 85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(1) Digital block

(V_{DD}, V_{CC} = + 5 V ± 10% ($V_{CC} \geq V_{DD}$) , GND, V_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit
				Min	Typ	Max	
Power supply voltage	V_{CC}	V_{CC}	—	4.5	5.0	5.5	V
Power supply current	I_{CC}		At CLK = 1 MHz operating (at no load)	—	2.5	4.5	mA
Input leakage current	I_{ILK}	CLK DI LD	V_{IN} = 0 to V_{CC}	− 10	—	10	µA
"L" level input voltage	V_{IL}		—	—	—	0.2 V_{CC}	V
"H" level input voltage	V_{IH}		—	0.5 V_{CC}	—	—	V
"L" level output voltage	V_{OL}	DO	I_{OL} = 2.5 mA	—	—	0.4	V
"H" level output voltage	V_{OH}		I_{OH} = − 400 µA	V_{CC} − 0.4	—	—	V

Note : I_{OL} and I_{OH} are output load current.

(2) Analog block

(V_{DD}, V_{CC} = + 5 V ± 10% ($V_{CC} \geq V_{DD}$) , GND, V_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit
				Min	Typ	Max	
Consumption current	I_{DD}	V_{DD}	No load	—	0.2	0.5	mA
Analog power supply voltage	V_{DD}	V_{DD}	$V_{DD} - V_{SS} \geq 2.0$ V	2.0	—	V_{CC}	V
	V_{SS}	V_{SS}		GND	—	V_{CC} − 2.0	V
Resolution	Res	AO_1 to AO_{12}	Monotonic increase	—	8	—	bit
Non linearity error	LE		No load $V_{DD} \leq V_{CC}$ − 0.1 V, $V_{SS} \geq$ 0.1 V	− 1.5	0	1.5	LSB
Differential linearity error	D_{LE}		No load $V_{DD} \leq V_{CC}$ − 0.1 V, $V_{SS} \geq$ 0.1 V	− 1.0	—	1.0	LSB
Output minimum voltage 1	V_{AOL1}	AO_1 to AO_{12}	No load, V_{SS} = 0 V, When digital setting is #00.	V_{SS}	—	V_{SS} + 0.1	V
Output minimum voltage 2	V_{AOL2}		I_{source} = 500 µA, When digital setting is #00.	V_{SS} − 2.0	V_{SS}	V_{SS} + 0.2	V
Output minimum voltage 3	V_{AOL3}		I_{sink} = 500 µA, When digital setting is #00.	V_{SS}	—	V_{SS} + 0.2	V
Output minimum voltage 4	V_{AOL4}		$V_{DD} = V_{CC}$ = 5.0 V, V_{SS} = GND = 0.0 V, I_{source} = 1.0 mA, When digital setting is #00.	V_{SS} − 0.3	V_{SS}	V_{SS} + 0.3	V
Output minimum voltage 5	V_{AOL5}		$V_{DD} = V_{CC}$ = 5.0 V, V_{SS} = GND = 0.0 V, I_{sink} = 1.0 mA, When digital setting is #00.	V_{SS}	—	V_{SS} + 0.3	V

(Continued)

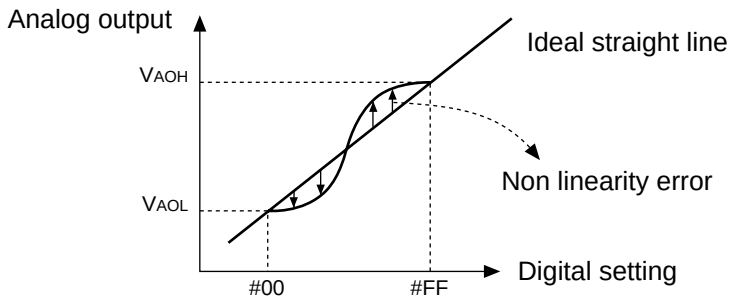
(Continued)

(V_{DD}, V_{CC} = + 5 V ± 10% ($V_{CC} \geq V_{DD}$) , GND, V_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit
				Min	Typ	Max	
Output maximum voltage 1	V_{AOH1}	AO 1 to AO 12	No load, $V_{DD} = V_{CC}$ When digital setting is #FF.	V_{DD} − 0.1	—	V_{DD}	V
Output maximum voltage 2	V_{AOH2}		I_{source} = 500 µA When digital setting is #FF.	V_{DD} − 0.2	—	V_{DD}	V
Output maximum voltage 3	V_{AOH3}		I_{sink} = 500 µA When digital setting is #FF.	V_{DD} − 0.2	V_{DD}	V_{DD} + 0.2	V
Output maximum voltage 4	V_{AOH4}		$V_{DD} = V_{CC}$ = 5.0 V V_{SS} = GND = 0.0 V I_{source} = 1.0 mA When digital setting is #FF.	V_{DD} − 0.3	—	V_{DD}	V
Output maximum voltage 5	V_{AOH5}		$V_{DD} = V_{CC}$ = 5.0 V V_{SS} = GND = 0.0 V I_{sink} = 1.0 mA When digital setting is #FF.	V_{DD} − 0.3	V_{DD}	V_{DD} + 0.3	V

Non linearity error : The error of the I/O curve from the ideal straight line between output voltages at "00" and "FF".

Differential linearity error : The error from the ideal increment given when the digital value is incremented by one bit.



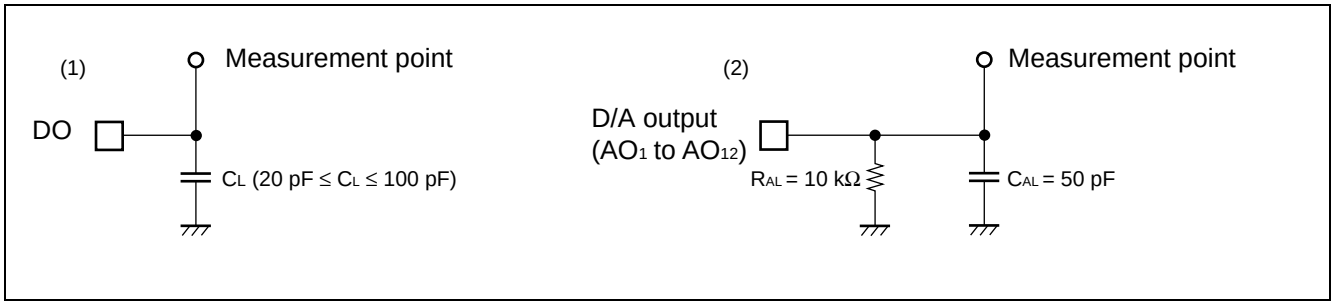
Note : V_{AOH} and V_{AOL} do not always match V_{DD} and V_{SS}, respectively.

2. AC Characteristics

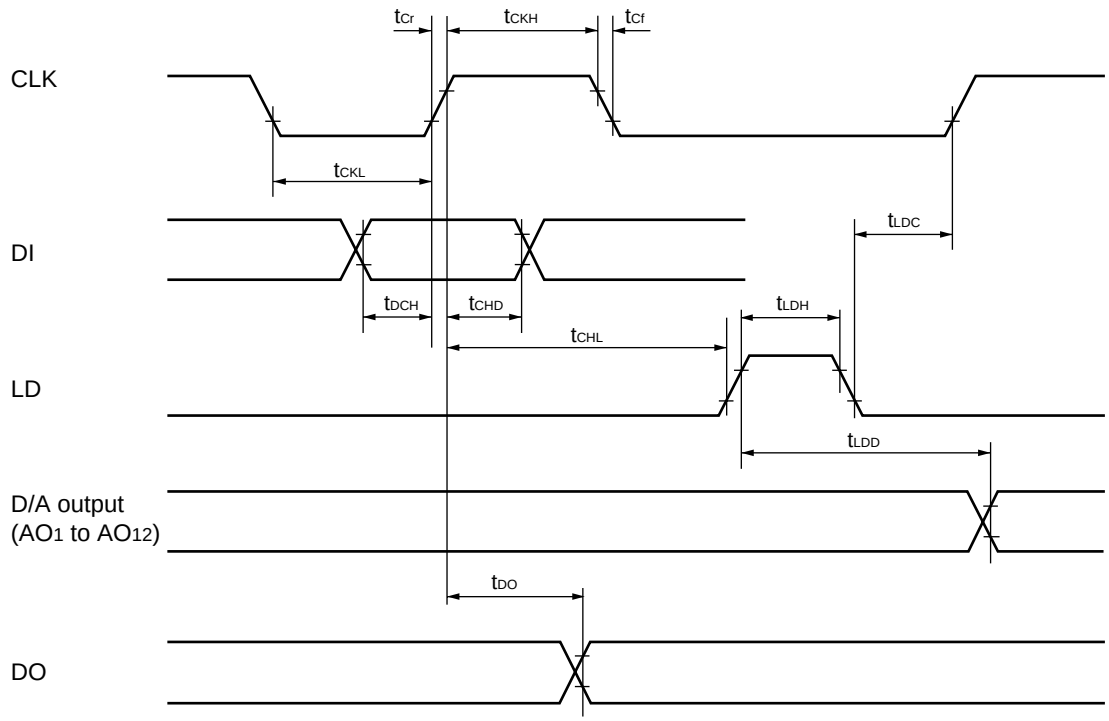
(V_{DD}, V_{CC} = + 5 V ± 10% ($V_{CC} \geq V_{DD}$) , GND, V_{SS} = 0 V, Ta = − 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
"L" level clock pulse width	t_{CKL}	—	200	—	ns
"H" level clock pulse width	t_{CKH}	—	200	—	
Clock rising time Clock falling time	t_{Cr} t_{Cf}	—	—	200	
Data setup time	t_{DCH}	—	30	—	
Data hold time	t_{CHD}	—	60	—	
Load setup time	t_{CHL}	—	200	—	
Load hold time	t_{LDC}	—	100	—	
"H" level load pulse width	t_{LDH}	—	100	—	
Data output delay time	t_{DO}	Refer to "Load condition (1) ".	70	350	
D/A output settling time	t_{LDD}	Refer to "Load condition (2) ".	—	20	µs

• Load condition



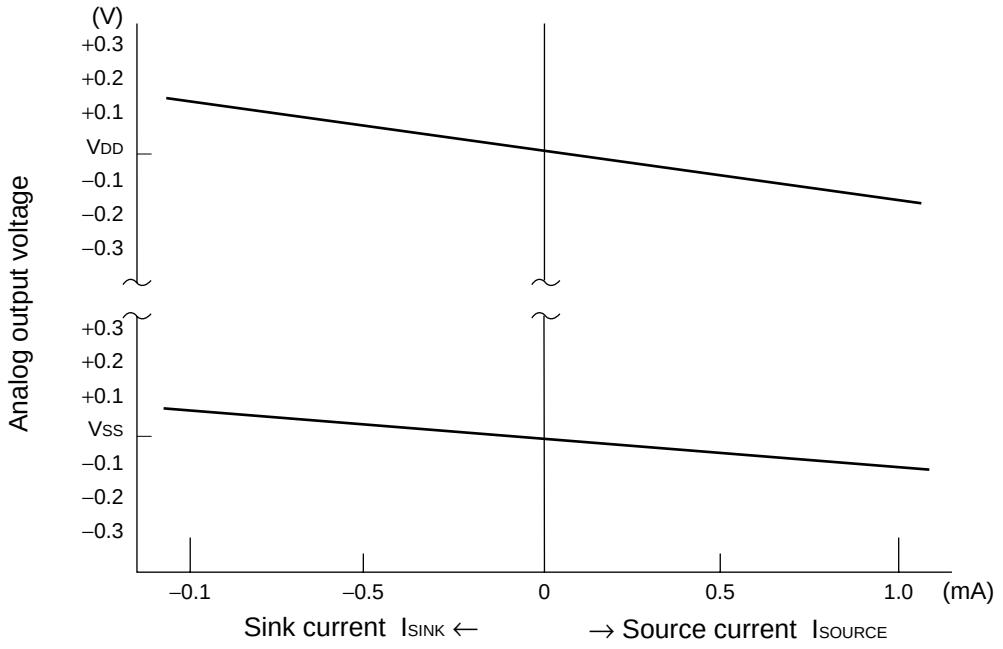
• Input/output timing



Note : The D/A output evaluation level is 90% and 10% of V_{CC}. The other evaluation level is 80% and 20% of V_{CC}.

■ EXAMPLE CHARACTERISTICS

Example of analog output voltage vs. sink/source current characteristics

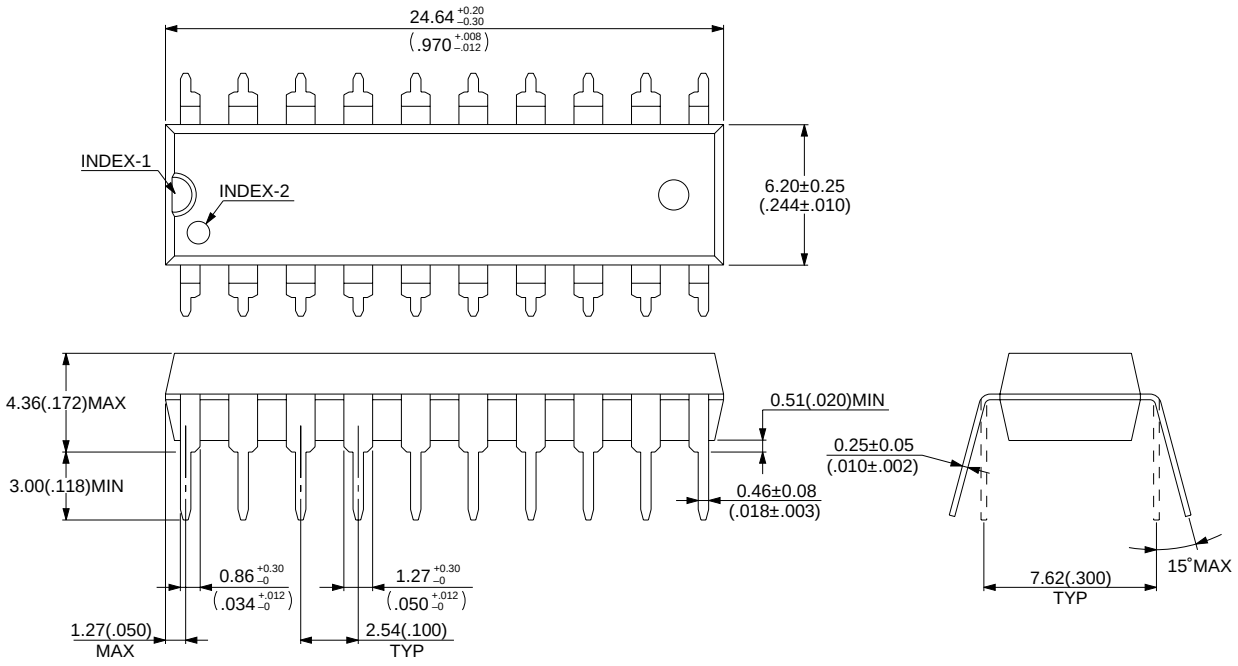


■ ORDERING INFORMATION

Part No.	Package	Remarks
MB88346BP	20-pin plastic DIP (DIP-20P-M02)	
MB88346BPF	20-pin plastic SOP (FPT-20P-M01)	
MB88346BPFV	20-pin plastic SSOP (FPT-20P-M03)	

■ PACKAGE DIMENSIONS

20-pin plastic DIP
(DIP-20P-M02)

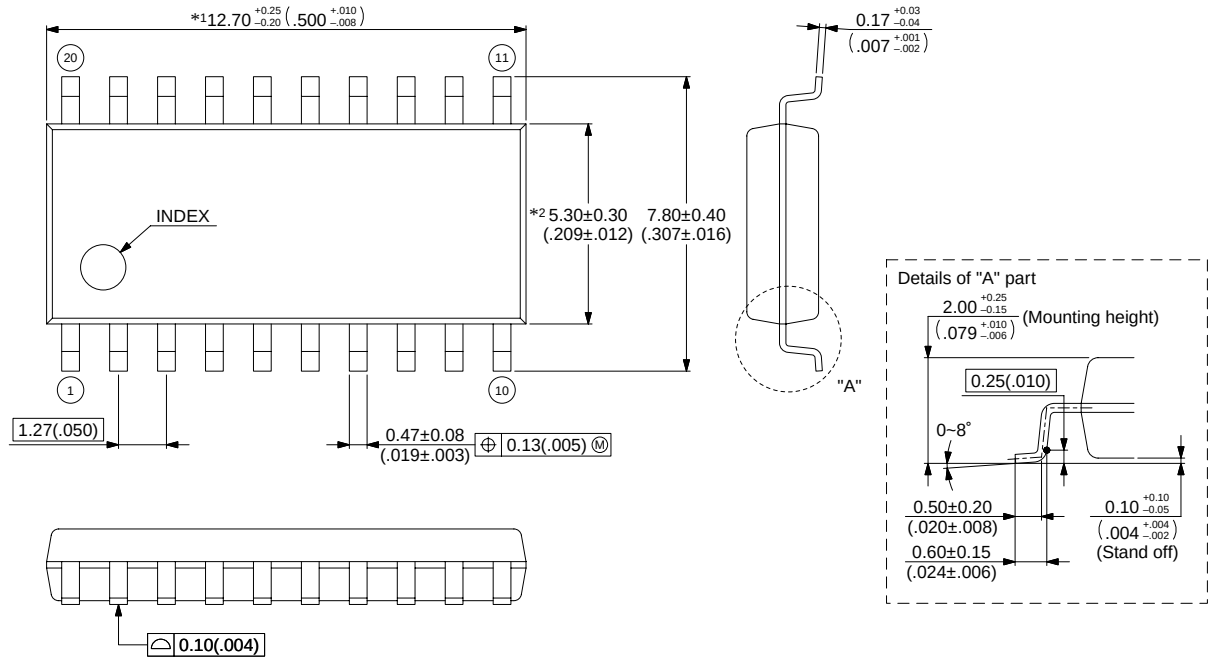


Dimensions in mm (inches).
Note : The values in parentheses are reference values.

(Continued)

20-pin plastic SOP
(FPT-20P-M01)

Note 1) *1 : These dimensions include resin protrusion.
Note 2) *2 : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.



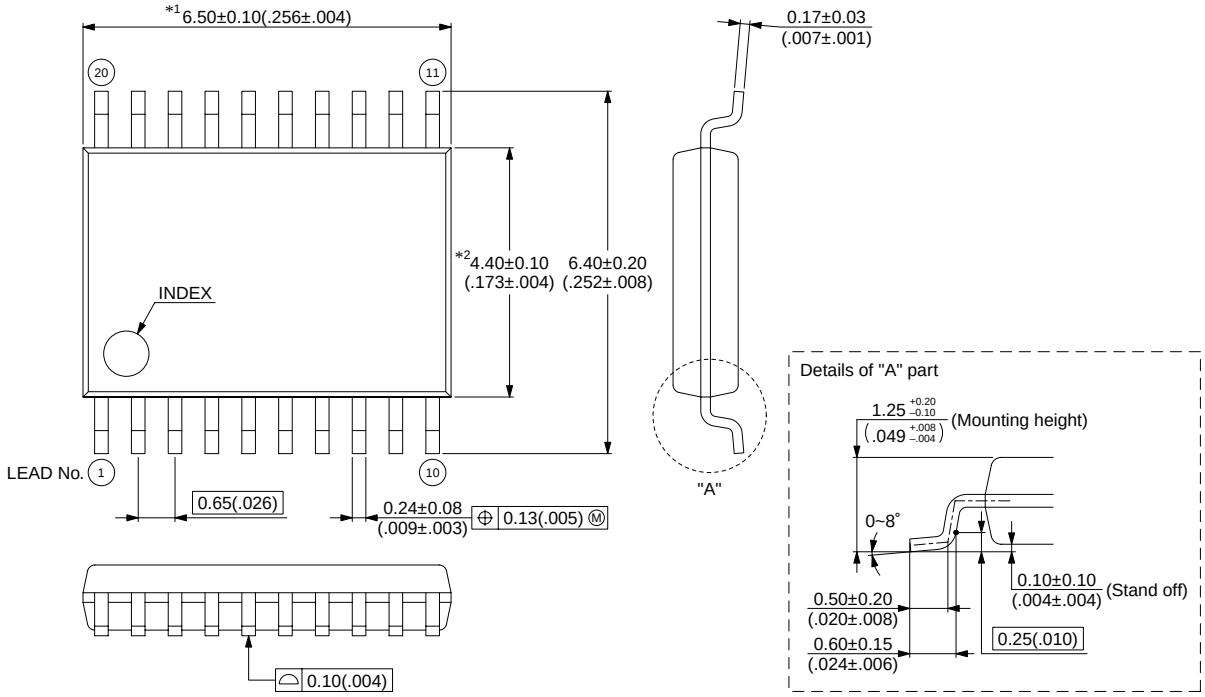
Dimensions in mm (inches).
Note: The values in parentheses are reference values.

(Continued)

(Continued)

20-pin plastic SSOP
(FPT-20P-M03)

Note 1) *1 : Resin protrusion. (Each side : +0.15 (.006) Max).
Note 2) *2 : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

FUJITSU LIMITED

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

The information, such as descriptions of function and application circuit examples, in this document are presented solely for the purpose of reference to show examples of operations and uses of Fujitsu semiconductor device; Fujitsu does not warrant proper operation of the device with respect to use based on such information. When you develop equipment incorporating the device based on such information, you must assume any responsibility arising out of such use of the information. Fujitsu assumes no liability for any damages whatsoever arising out of the use of the information.

Any information in this document, including descriptions of function and schematic diagrams, shall not be construed as license of the use or exercise of any intellectual property right, such as patent right or copyright, or any other right of Fujitsu or any third party or does Fujitsu warrant non-infringement of any third-party's intellectual property right or other right by using such information. Fujitsu assumes no liability for any infringement of the intellectual property rights or other rights of third parties which would result from the use of information contained herein.

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).

Please note that Fujitsu will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.

Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the prior authorization by Japanese government will be required for export of those products from Japan.

F0503