FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-13213-1E

Linear IC Converter

CMOS

D/A Converter for Digital Tuning
(Compatible with I²C Bus)

MB88141A

■ DESCRIPTION

The FUJITSU MB88141A is an 8-bit D/A converter with 12 built–in channels.

The 12 analog output channels have built-in OP Amps, providing large current drive capability.

Data input is compatible with I²C specifications, and is controlled by two control lines.

The built-in I/O expander function allows the MB88141A to be controlled by devices incompatible with I²C bus specifications (provides conversion between I²C serial and 8- or 4-bit parallel I/O).

The MB88141A is ideal for replacing electronic knob or pre-set variable resistance tuning devices.

■ FEATURES

- Ultra-low power consumption (0.9 mW/channel Typ.)
- Ultra-compact package
- Built-in 12-channel R-2R type 8-bit D/A converter
- Built-in analog output amplifier (maximum sink current 1.0 mA, maximum source current 1.0 mA)
- Analog output range 0 V to V_{CC}

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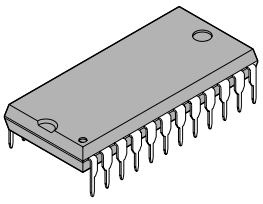
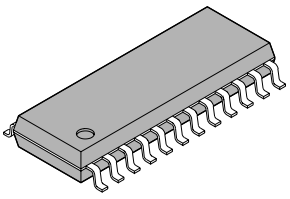
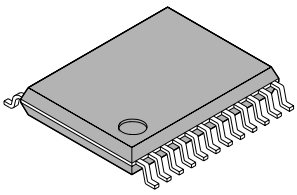
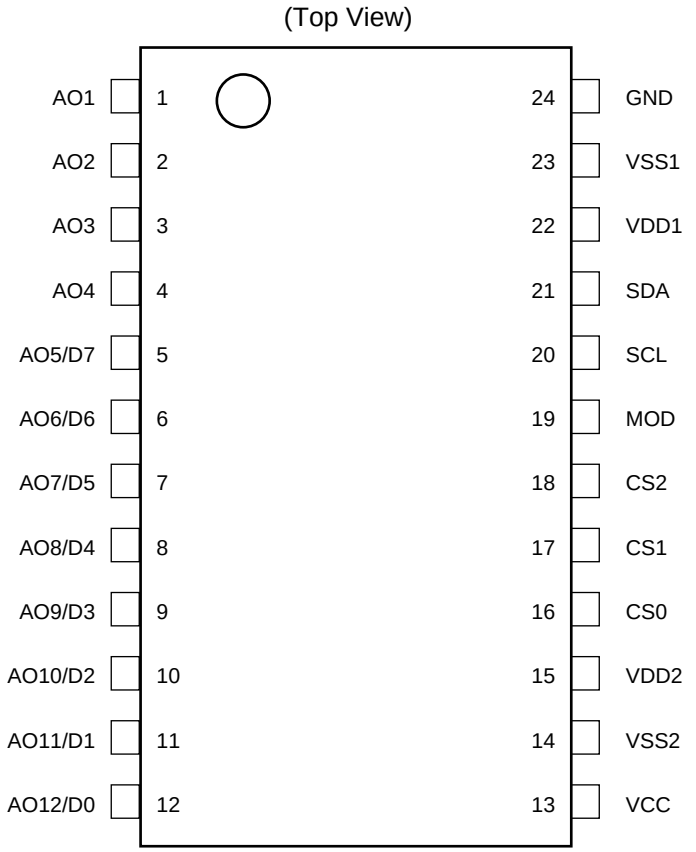
■ PACKAGES

24-pin plastic DIP	24-pin plastic SOP	24-pin plastic SSOP
		
(DIP-24P-M02)	(FPT-24P-M01)	(FPT-24P-M03)

(Continued)

- 5 V single power supply
- Power supply/GND for MCU interface and OP Amp is separate from power supply/GND for D/A converter
- Power supply for D/A converter is divided into two systems for V_{DD1}/V_{SS1} (AO1 to AO4) and V_{DD2}/V_{SS2} (AO5 to AO12) , allowing separate level settings for each system
- Compatible with serial data input, I^2C specifications
- Built-in I/O expander function (converts between I^2C serial and 8-or 4-bit parallel)
- CMOS process
- Packages : DIP 24-pin, SOP 24-pin, SSOP 24-pin

■ PIN ASSIGNMENT



(DIP-24P-M02)
(FPT-24P-M01)
(FPT-24P-M03)

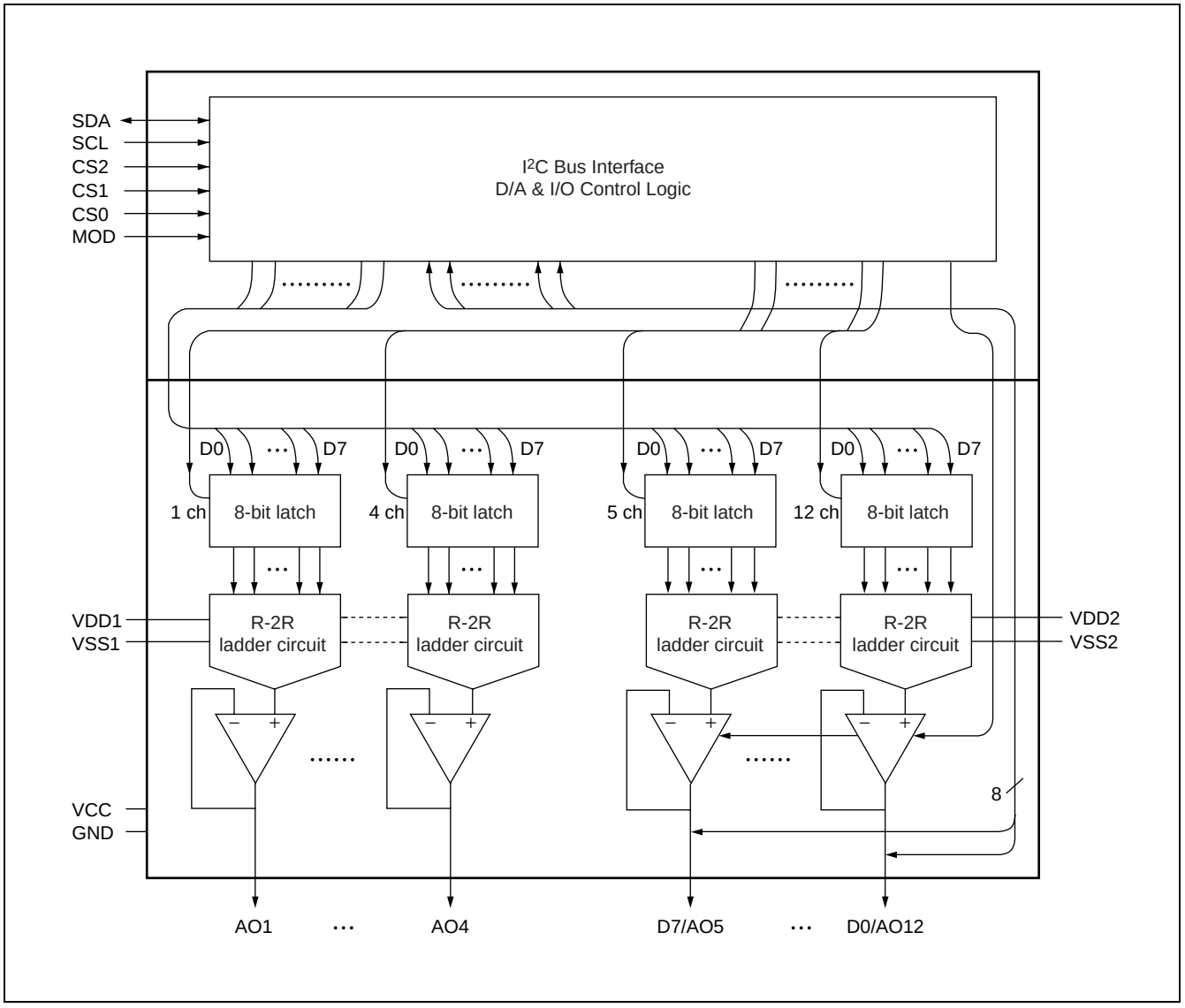
■ PIN DESCRIPTION

Pin no.	Symbol	Circuit Type	I/O	Description
21	SDA	C	I/O	I^2C bus data input/output pin (hysteresis input). Outputs the acknowledge signal.
20	SCL	B	I	I^2C bus shift clock input pin (hysteresis input) .
19	MOD	A	I	D/A converter and I/O expander mode switching pin. *1, *2 Input “L” to operate as a D/A converter, “H” to operate as I/O expander and D/A converter.
16 17 18	CS0 CS1 CS2	A	I	These pins set the lower 3 bits of the slave address. *1 This allows up to eight MB88141A chips to be used on the same bus line.
1 2 3 4	AO1 AO2 AO3 AO4	D	O	8-bit D/A outputs with OP Amp. *2
5 6 7 8 9 10 11 12	AO5/D7 AO6/D6 AO7/D5 AO8/D4 AO9/D3 AO10/D2 AO11/D1 AO12/D0	E	I/O	8-bit D/A outputs with OP Amp. *2 In I/O expander operation, these pins function as parallel data input/output pins.
13	VCC	Power supply	—	Power supply pin for digital circuits and OP Amp.
24	GND	GND	—	GND pin for digital circuits and OP Amp.
22	VDD1	Power supply	—	Reference power supply pin for D/A converter (H) . AO1 to AO4.
23	VSS1	Power supply	—	Reference power supply pin for D/A converter (L) . AO1 to AO4.
15	VDD2	Power supply	—	Reference power supply pin for D/A converter (H) . AO5 to AO12.
14	VSS2	Power supply	—	Reference power supply pin for D/A converter (L) . AO5 to AO12.

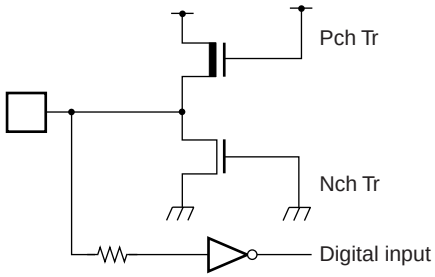
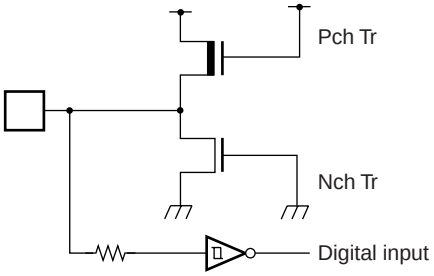
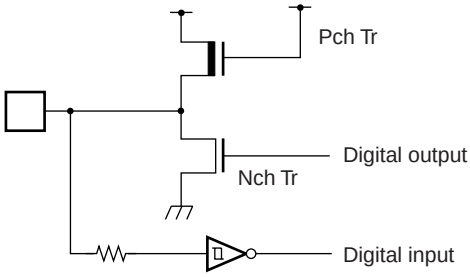
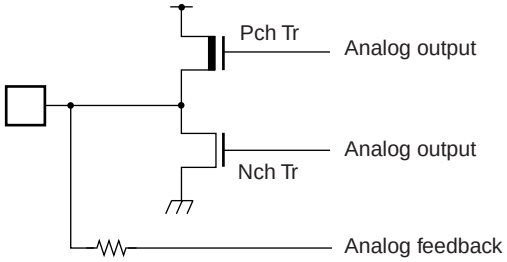
*1: The MOD and CS0-CS2 pins should be used with fixed level input.

*2: When using the I/O expander function together with the D/A converter function, take care that D/A converter output precision is within a range that will not affect overall system operation.

■ BLOCK DIAGRAM



■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		Input dedicated pin
B		Input dedicated pin • I²C bus pin • Hysteresis input
C		Input/output pin • I²C bus pin • Hysteresis input • N-ch open drain output
D		Analog output pin

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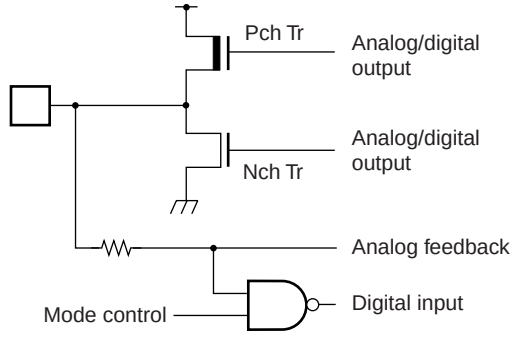
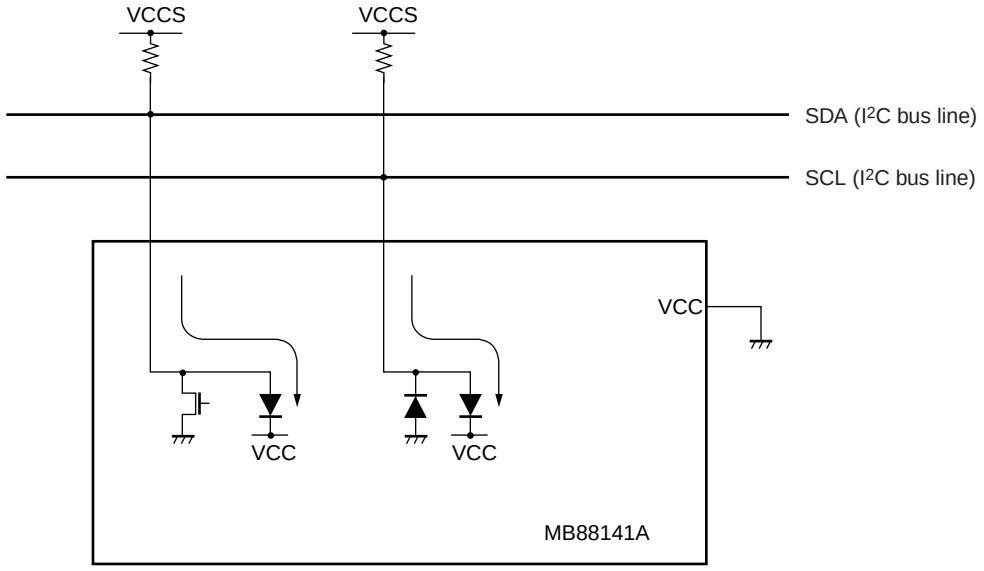
Type	Circuit	Remarks
E		Analog/digital input/output pin

Note : Circuit types B and C are I²C bus pins. Caution should be taken in using these pins because when the VCC power is off current from the I²C bus line power supply VCCS can enter the VCC side of the device power supply.



■ DATA CONFIGURATION

The MB88141A has the following data configuration the two operating modes (D/A converter (12-channel) and I/O expander plus D/A converter), selected by the MOD pin.

1. For D/A Converter (12-channel) Operation (MOD = “L”)

(1) I²C Bus Format

First S6 ⟶ S0 R/W C7 ⟶ C0 D7 ⟶ D0 Last

S	Slave address (7 bits)	0	A	Channel selection (8 bits)	A	D/A data (8 bits)	A	P

: Sent from master device : Sent from MB88141A (slave device)

S : “Start” condition P : “Stop” condition A : “Acknowledge” output

(2) Slave Address Comparison (7 bits)

Slave address input (7 bits)								Internally fixed				Externally set		
S6	**S5**	**S4**	**S3**	**S2**	**S1**	**S0**		**CS6**	**CS5**	**CS4**	**CS3**	**CS2**	**CS1**	**CS0**
1	0	0	1	0	0	0	=	1	0	0	1	0	0	0
1	0	0	1	0	0	1	=	1	0	0	1	0	0	1
1	0	0	1	0	1	0	=	1	0	0	1	0	1	0
1	0	0	1	0	1	1	=	1	0	0	1	0	1	1
1	0	0	1	1	0	0	=	1	0	0	1	1	0	0
1	0	0	1	1	0	1	=	1	0	0	1	1	0	1
1	0	0	1	1	1	0	=	1	0	0	1	1	1	0
1	0	0	1	1	1	1	=	1	0	0	1	1	1	1

Address comparison: Operates only for devices whose own slave address (internally fixed CS6 to CS3 and externally set CS2 to CS0) matches the slave address input value.

(3) R/W Selection (1 bit)

Fixed at “0” (the D/A converter performs write operations only) .

(4) Channel Selection (8 bits)

C7	C6	C5	C4	C3	C2	C1	C0	Channel select
×	×	×	×	0	0	0	0	All channels selected *1
×	×	×	×	0	0	0	1	AO1 selected
≀	≀	≀	≀	≀	≀	≀	≀	≀
×	×	×	×	1	1	0	0	AO12 selected
×	×	×	×	1	1	0	1	Don't Care
×	×	×	×	1	1	1	0	Don't Care
×	×	×	×	1	1	1	1	All channels selected *2

× : Don't Care

*1: The 1 byte of data following the channel selection is set on all channels (all channels set to same data value) .

S	Slave address (7 bits)	0	A	X X X X 0 0 0 0	A	D/A data (8 bits)	A	P

*2: The 12 bytes of data following the channel selection are set on all channels (all channels set to separate data values) .

S	Slave address	0	A	X X X X1 1 1 1	A	AO1 data	A	---	AO12 data	A	P

: Sent from master device : Sent from MB88141A (slave device)

S : "Start" condition P : "Stop" condition A : "Acknowledge" output

Note: Setting will repeat, continuing in order from ch1, until the start and stop conditions are acknowledged.

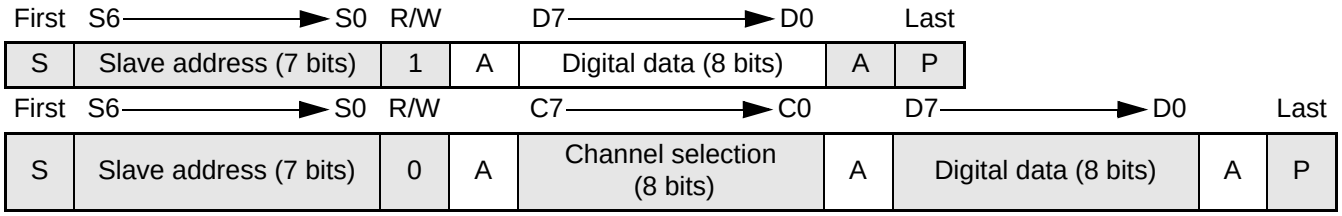
(5) D/A Data (8 bits)

D7	D6	D5	D4	D3	D2	D1	D0	D/A output
0	0	0	0	0	0	0	0	$\cong V_{SS}$
0	0	0	0	0	0	0	1	$\cong (V_{REF} / 256) \times 1 + V_{SS}$
0	0	0	0	0	0	1	0	$\cong (V_{REF} / 256) \times 2 + V_{SS}$
≀	≀	≀	≀	≀	≀	≀	≀	≀
1	1	1	1	1	1	1	0	$\cong (V_{REF} / 256) \times 254 + V_{SS}$
1	1	1	1	1	1	1	1	$\cong (V_{REF} / 256) \times 255 + V_{SS}$

Note: $V_{REF} = V_{DD} - V_{SS}$

2. For D/A Converter + I/O Expander Operation (MOD = "H")

(1) I²C Bus Format



: Sent from master device : Sent from MB88141A (slave device)

S : "Start" condition P : "Stop" condition A : "Acknowledge" output

(2) Slave Address Comparison (7 bits)

Slave address comparison is the same as for D/A converter (12-channel) operation (see "1. (2) "Slave Address Comparison"), with the exception that the CS2 setting determines the number of D/A converter channels and the number of I/O expander bits.

CS2	D/A converter	I/O expander
0	4 channels (AO1 to AO4)	8 bits (D7 to D0)
1	8 channels (AO1 to AO8)	4 bits (D3 to D0)

When CS2 = "1" is selected, the upper 4 bits (D7 to D4) of write operations (I²C bus to parallel interface) are ignored, and the upper 4 bits of read operations (parallel interface to I²C bus) are output at "0" (low) .

(3) R/W Selection (1 bit)

R/W	I/O expander operation	D/A converter operation
0	I²C bus input → parallel data output	I²C bus input → analog output
1	Parallel data input → I²C bus output	—

(4) Channel Selection (8 bits)

C7	C6	C5	C4	C3	C2	C1	C0	Channel select
×	×	×	×	0	0	0	0	I/O expander operation
×	×	×	×	0	0	0	1	AO1 selected
≀	≀	≀	≀	≀	≀	≀	≀	≀
×	×	×	×	0	1	0	0	AO4 selected
×	×	×	×	0	1	0	1	Don't care (AO5 selected)
≀	≀	≀	≀	≀	≀	≀	≀	≀
×	×	×	×	1	0	0	0	Don't care (AO8 selected)
×	×	×	×	1	0	0	1	Don't Care
≀	≀	≀	≀	≀	≀	≀	≀	≀
×	×	×	×	1	1	1	0	Don't Care
×	×	×	×	1	1	1	1	I/O expander continuous operation

( ): When using D/A converter 8 channel, I/O expander 4 bit operation.
× : Don't Care

(5) D/A Data (8 bits)

Same as "1 (5) D/A Data (8 bits)".

(6) I/O Expander Continuous Operation

I^2C bus input → parallel data output

S	Slave address	0	A	X X X X1 1 1 1	A	Digital data	A	···	Digital data	A	P

Note: In continuous operation, operation continues until start and stop conditions are acknowledged.

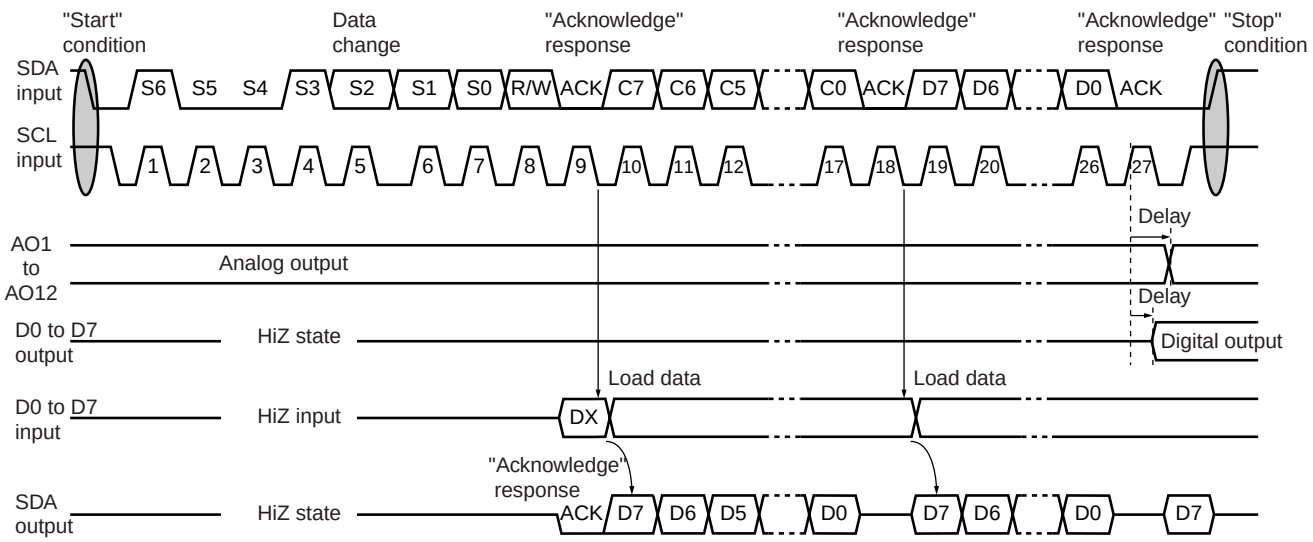
Parallel data input → I^2C bus output

S	Slave address	1	A	Digital data	A	Digital data	A	···	Digital data	A	P

: Sent from master device : Sent from MB88141A (slave device)

S : "Start" condition P : "Stop" condition A : "Acknowledge" output

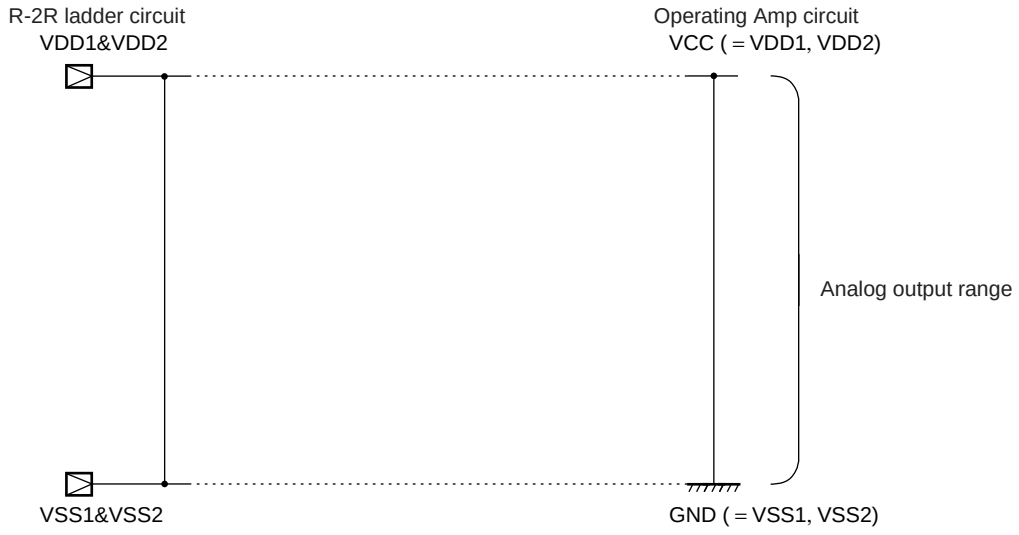
■ TIMING DIAGRAM (I²C BUS SPECIFICATIONS)



Note:

- The SDA input acknowledge response (ACK) is an output signal from the MB88141A.
- The D0-D7 input and output timing represent the timing of switching to write and read operations respectively. Also, D0-D7 input remains in HiZ state between the end of a read operation and the acknowledgment of the next I/O write signal.

■ ANALOG OUTPUT VOLTAGE RANGE



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating		Unit
			Min.	Max.	
Supply voltage	V_{CC}	With reference to GND, at Ta = +25 °C	–0.3	+7.0 *	V
	V_{DD}		–0.3	+7.0 *	V
	V_{SS}		–0.3	+7.0 *	V
Input voltage	V_{IN}		–0.3	V_{CC} + 0.3	V
Output voltage	V_{OUT}		–0.3	V_{CC} + 0.3	V
Power consumption	P_D	—	—	250	mW
Operating temperature	Ta	—	–20	+85	°C
Storage temperature	Tstg	—	–55	+120	°C

*: $V_{CC} \geq V_{DD1} \geq V_{SS1}$, $V_{CC} \geq V_{DD2} \geq V_{SS2}$

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Value			Unit
			Min.	Typ.	Max.	
Supply voltage 1	V_{CC}	—	4.50	5.00	5.50	V
	GND	—	—	0	—	V
Supply voltage 2	V_{DD1}	$V_{CC} \geq V_{DD1} > V_{SS1}$ $V_{DD1} - V_{SS1} \geq 2.0$ V	2.00	—	V_{CC}	V
	V_{SS1}		0.00	—	3.50	V
Supply voltage 3	V_{DD2}	$V_{CC} \geq V_{DD2} > V_{SS2}$ $V_{DD2} - V_{SS2} \geq 2.0$ V	2.00	—	V_{CC}	V
	V_{SS2}		0.00	—	3.50	V
Analog output current	I_{AL}	Source current	0	—	1.00	mA
	I_{AH}	Sink current	0	—	1.00	mA
Oscillator limit output capacitance	C_{OL}	—	—	—	1.00	µF
Digital data setting range	—	—	#00	—	#FF	—
Operating temperature	Ta	—	–20	—	+85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(1) Digital Circuits

(VCC = +5 V ± 10%, GND = 0 V, Ta = –20 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit
				Min.	Typ.	Max.	
Supply voltage	V_{CC}	VCC	—	4.50	5.00	5.50	V
Supply current	I_{CC}		SCL = 400 kHz, no load	—	1.00	3.70	mA
Input leak current	I_{ILK}	SDA, SCL CS0, CS1 CS2, MOD D0 to D7	V_{IN} = 0 to V_{CC}	–10	—	+10	µA
"L" level input voltage	V_{IL}		—	0	—	0.30 V_{CC}	V
"H" level input voltage	V_{IH}		—	0.70 V_{CC}	—	V_{CC}	V
Input hysteresis width	V_{HYS}	SDA, SCL	—	0.05 V_{CC}	—	—	V
"H" level output voltage	V_{OH}	D0 to D7	I_{OH} = –400 µA	V_{CC} – 0.4	—	—	V
"L" level output voltage	V_{OL1}		I_{OL} = 2.5 mA	—	—	0.40	
	V_{OL2}	SDA	I_{OL} = 3.0 mA	—	—	0.40	V
	V_{OL3}		I_{OL} = 6.0 mA	—	—	0.60	

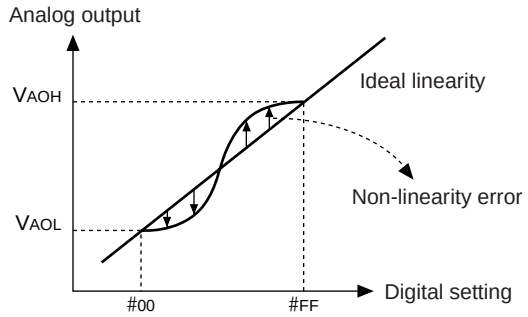
(2) Analog Circuits 1

(VCC = +5 V ± 10%, GND = 0 V, Ta = –20 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit
				Min.	Typ.	Max.	
Current consumption	I_{DD}	VDD1, VDD2	No load $I_{DD} = I_{DD1} + I_{DD2}$	—	1.20	2.50	mA
Analog voltage	V_{DD}		$V_{DD1} – V_{SS1} \geq 2.0$ V $V_{DD2} – V_{SS2} \geq 2.0$ V	2.0	—	V_{CC}	V
	V_{SS}	VSS1, VSS2		GND	—	3.5	
Resolution	Res	AO1 to AO12	No load $V_{DD1}, V_{DD2} \leq V_{CC} – 0.1$ V $V_{SS1}, V_{SS2} \geq 0.1$ V	—	8	—	bit
Monotonic increase	Rem			—	8	—	bit
Non-linearity error	LE			–1.5	—	+1.5	LSB
Differential linearity error	D_{LE}			–1.0	—	+1.0	LSB

Non-linearity error :
Error in the input/output curve with respect to a straight line connecting output voltage at “00” and output voltage at “FF” levels.

Differential linearity error :
Deviation from ideal voltage with respect to a 1-bit increase in digital value.



Note: V_{AOH} and V_{DD}, as well as V_{AOL} and Vss are not necessarily the same values.

(3) Analog Circuits 2

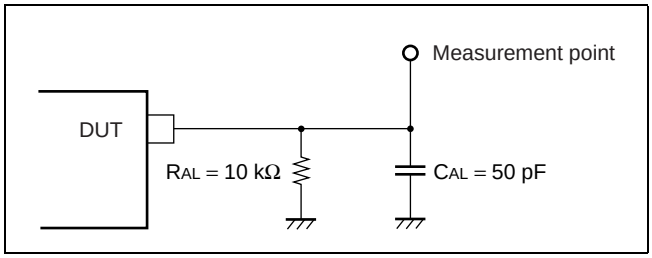
(VCC = VDD1 = VDD2 = +5 V, GND = VSS1 = VSS2 = 0 V, Ta = –20 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions		Value			Unit
					Min.	Typ.	Max.	
Output minimum voltage 1	V_{AOL1}	AO1 to AO12	I_{AL} = 0 µA	Digital data “00”	V_{SS}	—	V_{SS} + 0.1	V
Output minimum voltage 2	V_{AOL2}		I_{AL} = 500 µA		V_{SS} – 0.2	V_{SS}	V_{SS} + 0.2	V
Output minimum voltage 3	V_{AOL3}		I_{AH} = 500 µA		V_{SS}	—	V_{SS} + 0.2	V
Output minimum voltage 4	V_{AOL4}		I_{AL} = 1.0 mA		V_{SS} – 0.3	V_{SS}	V_{SS} + 0.3	V
Output minimum voltage 5	V_{AOL5}		I_{AH} = 1.0 mA		V_{SS}	—	V_{SS} + 0.3	V
Output maximum voltage1	V_{AOH1}		I_{AL} = 0 µA	Digital data “FF”	V_{DD} – 0.1	—	V_{DD}	V
Output maximum voltage2	V_{AOH2}		I_{AL} = 500 µA		V_{DD} – 0.2	—	V_{DD}	V
Output maximum voltage3	V_{AOH3}		I_{AH} = 500 µA		V_{DD} – 0.2	V_{DD}	V_{DD} + 0.2	V
Output maximum voltage4	V_{AOH4}		I_{AL} = 1.0 mA		V_{DD} – 0.3	—	V_{DD}	V
Output maximum voltage5	V_{AOH5}		I_{AH} = 1.0 mA		V_{DD} – 0.3	V_{DD}	V_{DD} + 0.3	V

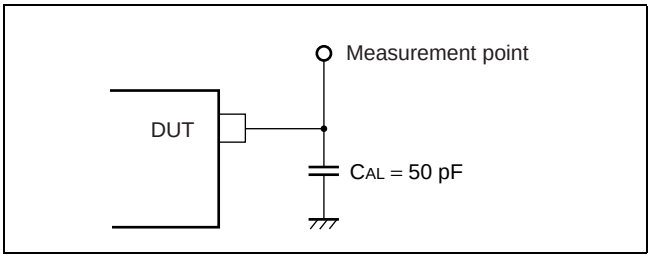
2. AC Characteristics

Parameter		Symbol	Condition	Value				Unit
				Standard mode		High-speed mode		
				Min.	Max.	Min.	Max.	
SCL clock frequency		f_{SCL}	—	0	100	0	400	kHz
Bus free time between “stop” condition and “start” condition		t_{BUF}	—	4.7	—	1.3	—	µs
Hold time (resend) “start” condition. The first clock pulse is generated after this interval.		$t_{HD\ ;\ STA}$	—	4.0	—	0.6	—	
SCL clock low hold time		t_{LOW}	—	4.7	—	1.3	—	
SCL clock high hold time		t_{HIGH}	—	4.0	—	0.6	—	
Resend “start” condition setup time		$t_{SU\ ;\ STA}$	—	4.7	—	0.6	—	
Data hold time		$t_{HD\ ;\ DAT}$	—	0	—	0	0.9	
Data setup time		$t_{SU\ ;\ DAT}$	—	250	—	100	—	ns
SDA and SCL signal fall time		t_R	—	—	1000	20 + 0.1 Cb	300	
SDA and SCL signal rise time		t_F	—	—	300	20 + 0.1 Cb	300	
“Stop” condition setup time		$t_{SU\ ;\ STO}$	—	4.0	—	0.6	—	µs
Pulse width of spike suppressed by input filter		t_{SP}	—	—	—	0	50	ns
Output fall time when bus capacitance is between 10 pF and 400 pF	Sink current 3mA	t_{OF}	—	—	250	20 + 0.1 Cb	250	
	Sink current 6mA		—	—	—	20 + 0.1 Cb	250	
I^2C bus line capacitance load		Cb	—	—	400	—	400	pF
D/A	Analog output settling time	$t_{DL\ ;\ AO}$	*1	—	100	—	100	µs
I/O expander	Digital output delay time	$t_{DL\ ;\ DO}$	*2	—	300	—	300	ns
	Input open time	$t_{DZ\ ;\ DI}$	*3	200	—	200	—	
	Digital input setup time	$t_{SU\ ;\ DI}$	—	250	—	100	—	
	Digital input hold time	$t_{HD\ ;\ DI}$	—	0.9	—	0.9	—	µs

*1: Load condition 1

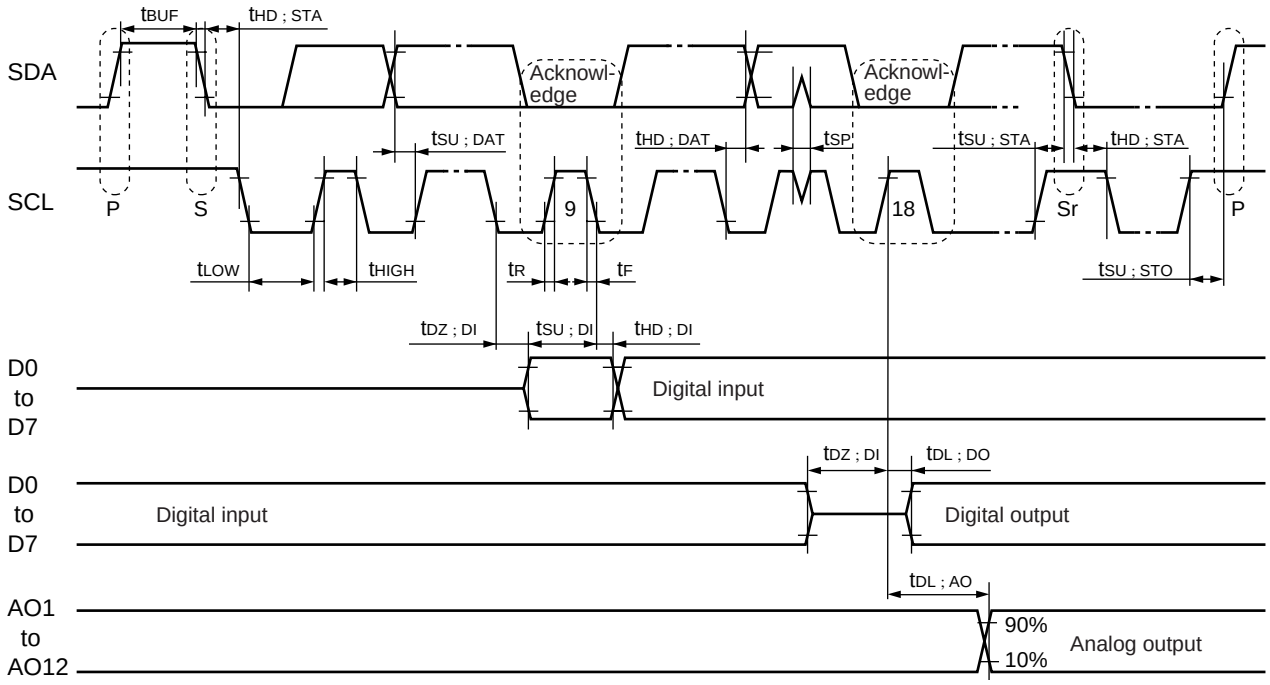


*2: Load condition 2



*3 : The I/O expander input open time value applies to a read operation following an I/O write operation, or to an I/O write operation following a read operation.

- **Input/Output Timing**



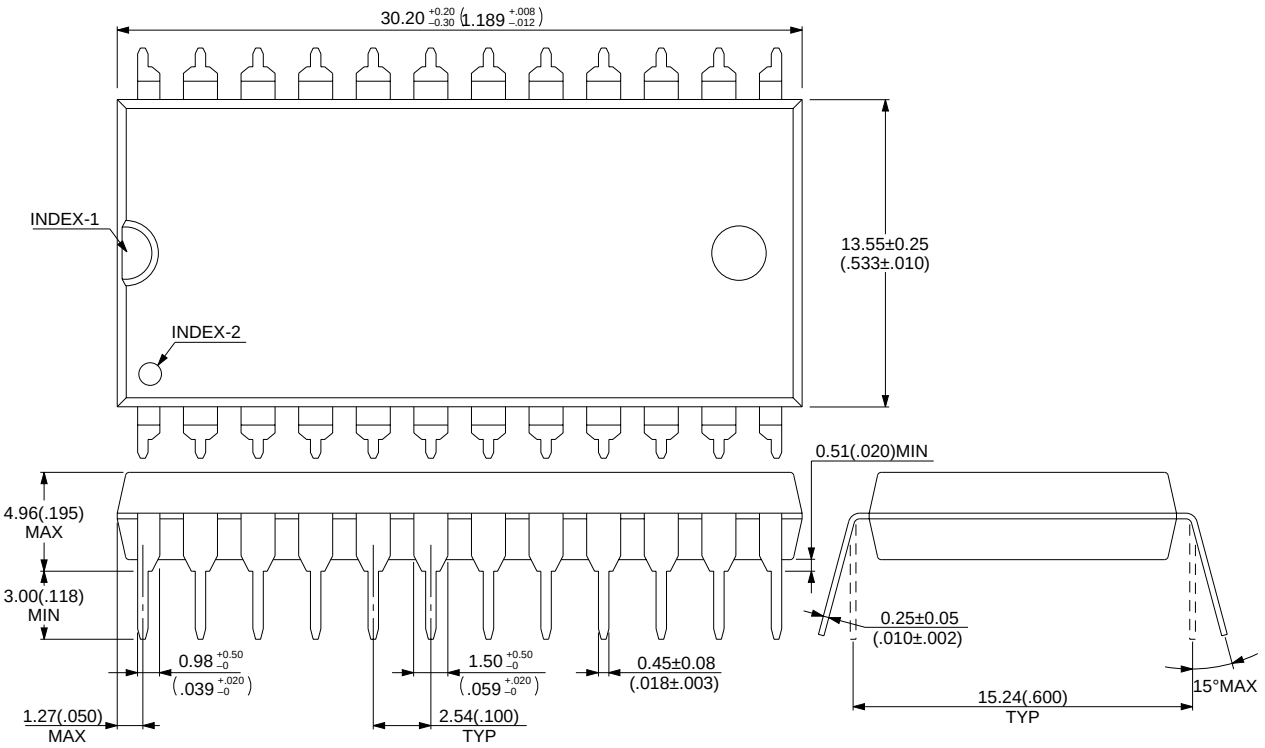
Note: The discrimination levels are 70% and 30% of V_{CC}.

■ ORDERING INFORMATION

Part number	Package	Remarks
MB88141AP	24-pin plastic DIP (DIP-24P-M02)	
MB88141APF	24-pin plastic SOP (FPT-24P-M01)	
MB88141APFV	24-pin plastic SSOP (FPT-24P-M03)	

■ PACKAGE DIMENSIONS

24-pin plastic DIP
(DIP-24P-M02)

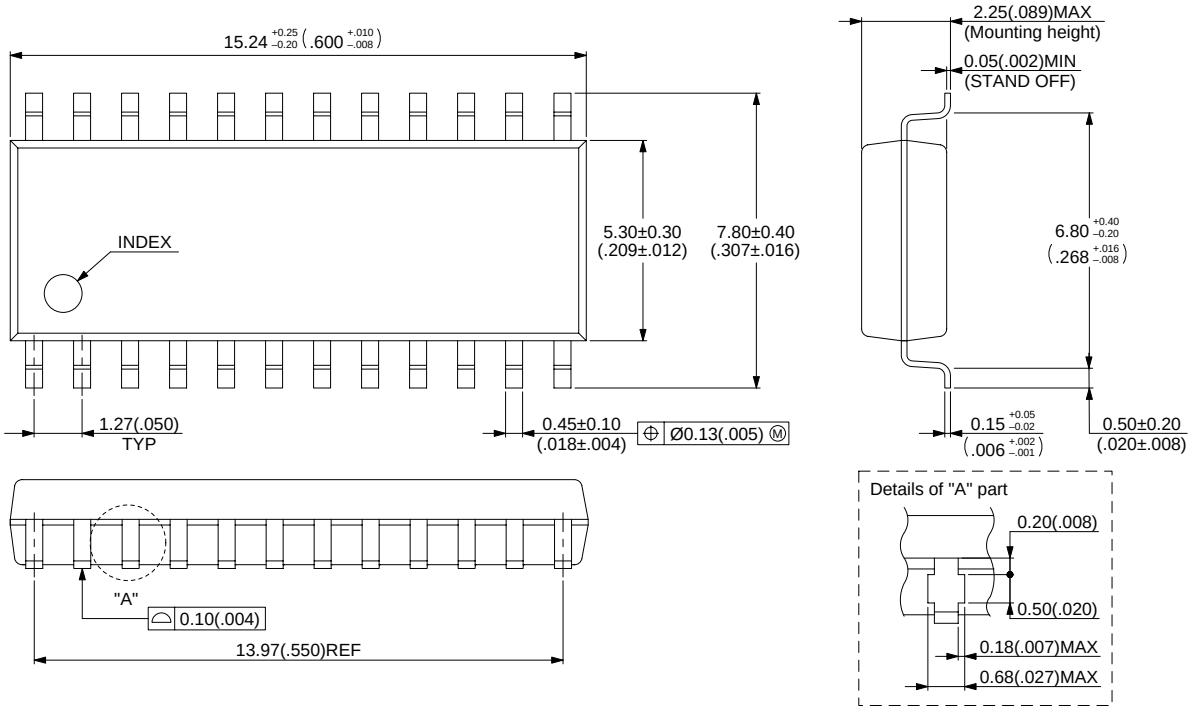


Dimensions in mm (inches)

(Continued)

(Continued)

24-pin plastic SOP
(FPT-24P-M01)



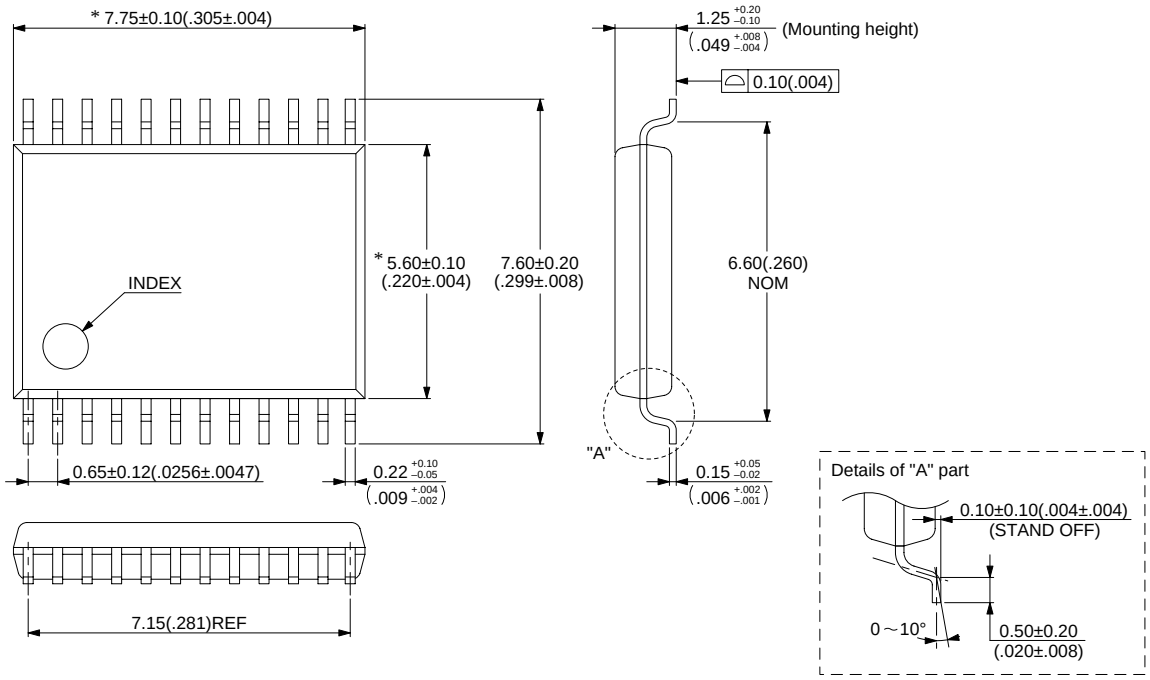
Dimensions in mm (inches)

(Continued)

(Continued)

24-pin plastic SSOP
(FPT-24P-M03)

Note) * marked dimensions do not include resin residues.



Dimensions in mm (inches)

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