FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-11424-4E

MEMORY Mobile FCRAM™

CMOS

16 Mbit (1 M word × 16 bit)

Mobile Phone Application Specific Memory

MB82D01181E-60L

■ DESCRIPTION

MB82D01181E is a Fast Cycle Random Access Memory (FCRAM) with asynchronous Static Random Access Memory (SRAM) interface containing 16,777,216 storages accessible in a 16-bit format. MB82D01181E is suited for mobile applications such as Cellular Handset and PDA.

Note: FCRAM is a trademark of Fujitsu Limited, Japan.

■ FEATURES

- Asynchronous SRAM Interface
- 1 M word × 16 bit Organization
- Low-voltage Operating Conditions : V_{DD} = 2.3 V to 3.5 V
- Wide Operating Temperature : T_A = 0 °C to + 70 °C
- Read/Write Cycle Time : $t_{RC} = t_{WC}$ = 70 ns Min
- Fast Random Access Time : $t_{AA} = t_{CE}$ = 60 ns Max
- Active current : I_{DDA1} = 20 mA Max
- Standby current : I_{DDs1} = 100 µA Max ($V_{DD} \leq$ 3.1 V)
- Power down current : I_{DDP} = 10 µA Max
- Byte Control
- Shipping Form : Wafer/Chip, 48-pin plastic FBGA

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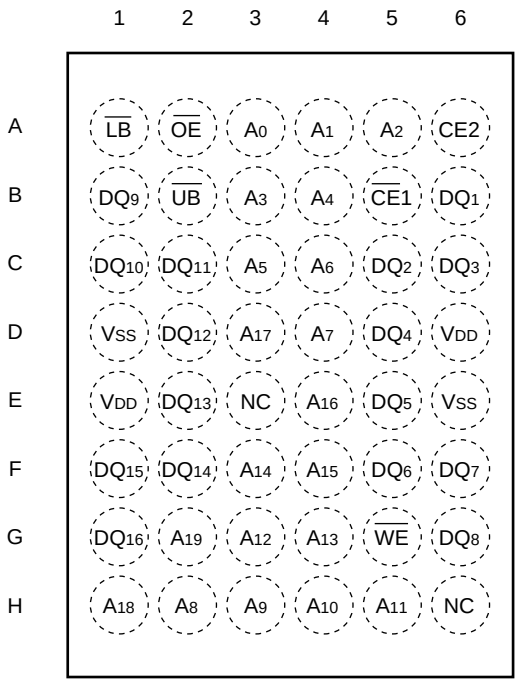
■ PIN ASSIGNMENT

(TOP VIEW)



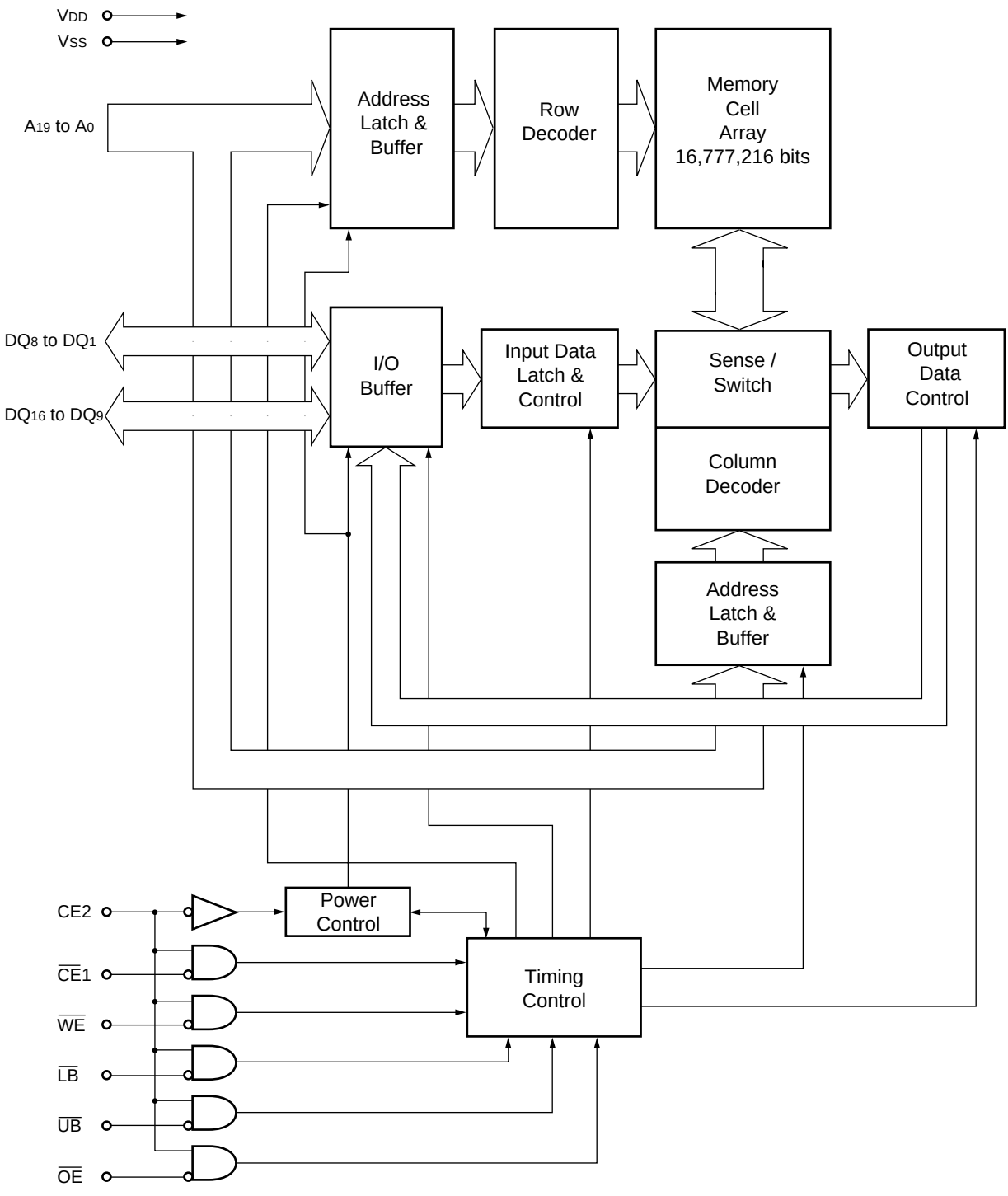
(BGA-48P-M18)

SRAM compatible FBGA (suffix PBN)

■ PIN DESCRIPTION

Pin Name	Description
A_{19} to A_0	Address Input
$\overline{CE}1$	Chip Enable (Low Active)
CE2	Chip Enable (High Active)
$\overline{WE}$	Write Enable (Low Active)
$\overline{OE}$	Output Enable (Low Active)
$\overline{LB}$	Lower Byte Control (Low Active)
$\overline{UB}$	Upper Byte Control (Low Active)
DQ_8 to DQ_1	Lower Byte Data Input/Output
DQ_{16} to DQ_9	Upper Byte Data Input/Output
V_{DD}	Power Supply
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM



■ FUNCTION TRUTH TABLE

Mode	CE2	$\overline{CE}$1	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	A_{19} to A_0	DQ_8 to DQ_1	DQ_{16} to DQ_9	I_{DD}	Data Retention
Standby (Deselect)	H	H	X	X	X	X	X	High-Z	High-Z	I_{DDS}	Yes
Output Disable*1	H	L	H	H	X	X	*3	High-Z	High-Z	I_{DDA}	Yes
No Read	H	L	H	L	H	H	Valid	High-Z	High-Z	I_{DDA}	Yes
Read (Upper Byte)	H	L	H	L	H	L	Valid	High-Z	Output Valid	I_{DDA}	Yes
Read (Lower Byte)	H	L	H	L	L	H	Valid	Output Valid	High-Z	I_{DDA}	Yes
Read (Word)	H	L	H	L	L	L	Valid	Output Valid	Output Valid	I_{DDA}	Yes
No Write	H	L	L	H	H	H	Valid	Invalid	Invalid	I_{DDA}	Yes
Write (Upper Byte)	H	L	L	H	H	L	Valid	Invalid	Input Valid	I_{DDA}	Yes
Write (Lower Byte)	H	L	L	H	L	H	Valid	Input Valid	Invalid	I_{DDA}	Yes
Write (Word)	H	L	L	H	L	L	Valid	Input Valid	Input Valid	I_{DDA}	Yes
Power Down *2	L	X	X	X	X	X	X	High-Z	High-Z	I_{DDP}	No

Note : L = V_{IL}, H = V_{IH}, X = either V_{IL} or V_{IH}, High-Z = High impedance

*1 : Output disable mode should not be kept longer than 1 μs.

*2 : Power down mode can be entered from standby state and all DQ pins are in High-Z state.

*3 : Can be either V_{IL} or V_{IH} but must be valid before read or write.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Supply Voltage *	V_{DD}	–0.5	+3.6	V
Input Voltage *	V_{IN}	–0.5	+3.6	V
Output voltage *	V_{OUT}	–0.5	+3.6	V
Short Circuit Output Current	I_{OUT}	–50	+50	mA
Storage Temperature	T_{STG}	–55	+125	°C

* : All voltages are referenced to V_{SS}.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value		Unit
		Min	Max	
Supply Voltage *1, *2	$V_{DD\,(31)}$	3.1	3.5	V
	$V_{DD\,(27)}$	2.7	3.1	V
	$V_{DD\,(23)}$	2.3	2.7	V
	V_{SS}	0	0	V
High Level Input Voltage *1, *2, *3	$V_{IH\,(31)}$	$V_{DD} \times 0.8$	$V_{DD} + 0.2$ and ≤ 3.5	V
	$V_{IH\,(23,\,27)}$	$V_{DD} \times 0.8$	$V_{DD} + 0.2$	V
Low Level Input Voltage *1, *4	V_{IL}	–0.3	$V_{DD} \times 0.2$	V
Ambient Temperature	T_A	0	+70	°C

*1 : All voltages are referenced to V_{SS}.

*2 : This device supports three voltage ranges, $V_{DD\,(31)}$, $V_{DD\,(27)}$, and $V_{DD\,(23)}$ on identical device. V_{DD} range is divided into three ranges on the table due to V_{IH} varied according to V_{DD} supply voltage.

*3 : Overshoot spec. ($V_{IH\,(Max)} = V_{DD} + 1.0$ V, pulse width ≤ 5.0 ns)

*4 : Undershoot spec. ($V_{IL\,(Min)} = -1.0$ V, pulse width ≤ 5.0 ns)

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ PIN CAPACITANCE

(f = 1.0 MHz, T_A = +25 °C)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Address Input Capacitance	C_{IN1}	V_{IN} = 0 V	—	—	5	pF
Control Input Capacitance	C_{IN2}	V_{IN} = 0 V	—	—	5	pF
Data Input/Output Capacitance	C_{IO}	V_{IO} = 0 V	—	—	8	pF

■ DC CHARACTERISTICS

Parameter	Symbol	Conditions		Value		Unit
				Min	Max	
Input Leakage Current	I_{LI}	$V_{SS} \le V_{IN} \le V_{DD}$		–1.0	+1.0	µA
Output Leakage Current	I_{LO}	$V_{SS} \le V_{OUT} \le V_{DD}$, Output Disable		–1.0	+1.0	µA
Output High Voltage Level	$V_{OH(31)}$	$V_{DD} = V_{DD(31)}$ Min, I_{OH} = –0.5 mA		2.5	—	V
	$V_{OH(27)}$	$V_{DD} = V_{DD(27)}$ Min, I_{OH} = –0.5 mA		2.2	—	V
	$V_{OH(23)}$	$V_{DD} = V_{DD(23)}$ Min, I_{OH} = –0.5 mA		1.8	—	V
Output Low Voltage Level	V_{OL}	I_{OL} = 1 mA		—	0.4	V
V_{DD} Power Down Current	I_{DDP}	$V_{DD} = V_{DD}$ Max, $V_{IN} = V_{IH}$ or V_{IL}, CE2 ≤ 0.2 V		—	10	µA
V_{DD} Standby Current	I_{DDS}	$V_{DD} = V_{DD(31)}$ Max, $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE}1$ = CE2 = V_{IH}		—	2.0	mA
		$V_{DD} = V_{DD(27, 23)}$ Max, $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE}1$ = CE2 = V_{IH}		—	1.0	
	I_{DDS1}	$V_{DD} = V_{DD(31)}$ Max, $V_{IN} \le 0.2$ V or $V_{IN} \ge V_{DD} – 0.2$ V, $\overline{CE}1$ = CE2 ≥ V_{DD} – 0.2 V		—	150	µA
		$V_{DD} = V_{DD(27, 23)}$ Max, $V_{IN} \le 0.2$ V or $V_{IN} \ge V_{DD} – 0.2$ V, $\overline{CE}1$ = CE2 ≥ V_{DD} – 0.2 V		—	100	
V_{DD} Active Current	I_{DDA1}	$V_{DD} = V_{DD}$ Max, $V_{IN} = V_{IH}$ or V_{IL}, $\overline{CE}1 = V_{IL}$ and CE2 = V_{IH}, I_{OUT} = 0 mA	t_{RC} / t_{WC} = Min	—	20	mA
			t_{RC} / t_{WC} = 1 µs	—	3.0	

Notes: • All voltages are referenced to Vss.
• DC Characteristics are measured after following POWER-UP timing.
• I_{OUT} depends on the output load conditions.

■ AC CHARACTERISTICS

(1) Read Operation

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
Read Cycle Time	t_{RC}	70	1000	ns	*1, *2
$\overline{CE}$1 Access Time	t_{CE}	—	60	ns	*3
$\overline{OE}$ Access Time	t_{OE}	—	40	ns	*3
Address Access Time	t_{AA}	—	60	ns	*3, *5
$\overline{LB}$, $\overline{UB}$ Access Time	t_{BA}	—	30	ns	*3
Output Data Hold Time	t_{OH}	5	—	ns	*3
$\overline{CE}$1 Low to Output Low-Z	t_{CLZ}	5	—	ns	*4
$\overline{OE}$ Low to Output Low-Z	t_{OLZ}	0	—	ns	*4
$\overline{LB}$, $\overline{UB}$ Low to Output Low-Z	t_{BLZ}	0	—	ns	*4
$\overline{CE}$1 High to Output High-Z	t_{CHZ}	—	20	ns	*3
$\overline{OE}$ High to Output High-Z	t_{OHZ}	—	20	ns	*3
$\overline{LB}$, $\overline{UB}$ High to Output Low-Z	t_{BHZ}	—	20	ns	*3
Address Setup Time to $\overline{CE}$1 Low	t_{ASC}	–5	—	ns	
Address Setup Time to $\overline{OE}$ Low	t_{ASO}	10	—	ns	
Address Invalid Time	t_{AX}	—	10	ns	*5
Address Hold Time from $\overline{CE}$1 High	t_{CHAH}	–5	—	ns	*6
Address Hold Time from $\overline{OE}$ High	t_{OHAH}	–5	—	ns	
$\overline{WE}$ High to $\overline{OE}$ Low Time for Read	t_{WHOL}	10	1000	ns	*7
$\overline{CE}$1 High Pulse Width	t_{CP}	10	—	ns	

*1 : Maximum value is applicable if $\overline{CE}$1 is kept at Low without any address change.

*2 : Address should not be changed within minimum t_{RC}.

*3 : The output load 50 pF with 50 Ω termination to $V_{DD} \times 0.5$ V.

*4 : The output load 5 pF without any other load.

*5 : Applicable when $\overline{CE}$1 is kept at Low.

*6 : t_{RC} (Min) must be satisfied.

*7 : If the actual value of t_{WHOL} is shorter than specified minimum value, the actual t_{AA} of following Read may become longer by the amount of subtracting actual value from specified minimum value.

(2) Write Operation

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
Write Cycle Time	t_{WC}	70	1000	ns	*1, *2
Address Setup Time	t_{AS}	0	—	ns	*2
$\overline{CE}1$ Write Pulse Width	t_{CW}	45	—	ns	*3
$\overline{WE}$ Write Pulse Width	t_{WP}	45	—	ns	*3
$\overline{LB}$, $\overline{UB}$ Write Pulse Width	t_{BW}	45	—	ns	*3
$\overline{LB}$, $\overline{UB}$ Byte Mask Setup Time	t_{BS}	–5	—	ns	*4
$\overline{LB}$, $\overline{UB}$ Byte Mask Hold Time	t_{BH}	–5	—	ns	*5
Write Recovery Time	t_{WR}	0	—	ns	*6
$\overline{CE}1$ High Pulse Width	t_{CP}	10	—	ns	
$\overline{WE}$ High Pulse Width	t_{WHP}	10	1000	ns	
$\overline{LB}$, $\overline{UB}$ High Pulse Width	t_{BHP}	10	1000	ns	
Data Setup Time	t_{DS}	15	—	ns	
Data Hold Time	t_{DH}	0	—	ns	
$\overline{OE}$ High to Address Setup Time for Write	t_{OES}	0	—	ns	*8
$\overline{OE}$ High to $\overline{CE}1$ Low Setup Time for Write	t_{OHCL}	–5	—	ns	*7
$\overline{LB}$ and $\overline{UB}$ Write Pulse Overlap	t_{BWO}	30	—	ns	

*1 : Maximum value is applicable if $\overline{CE}1$ is kept at Low without any address change.

*2 : Minimum value must be equal or greater than the sum of write pulse width (t_{CW}, t_{WP} or t_{BW}) and write recovery time (t_{WR}) .

*3 : Write pulse width is defined from High to Low transition of $\overline{CE}1$, $\overline{WE}$, $\overline{LB}$ or $\overline{UB}$, whichever occurs last.

*4 : Applicable for byte mask only. Byte mask setup time is defined to the High to Low transition of $\overline{CE}1$ or $\overline{WE}$ whichever occurs last.

*5 : Applicable for byte mask only. Byte mask hold time is defined from the Low to High transition of $\overline{CE}1$ or $\overline{WE}$ whichever occurs first.

*6 : Write recovery time is defined from Low to High transition of $\overline{CE}1$, $\overline{WE}$, $\overline{LB}$ or $\overline{UB}$, whichever occurs first.

*7 : If $\overline{OE}$ is Low after minimum t_{OHCL}, read cycle is initiated. In other words, $\overline{OE}$ must be brought to High within 5 ns after $\overline{CE}1$ is brought to Low.

*8 : If $\overline{OE}$ is Low after new address input, read cycle is initiated. In other words, $\overline{OE}$ must be brought to High at the same time or before new address valid.

Note : AC Characteristics are measured after following POWER-UP timing.

(3) Power Down Parameters

Parameter	Symbol	Value		Unit	Note
		Min	Max		
CE2 Low Setup Time for Power Down Entry	t_{CSP}	10	—	ns	
CE2 Low Hold Time after Power Down Entry	t_{C2LP}	80	—	ns	
$\overline{CE}$1 High Hold Time following CE2 High after Power Down Exit	t_{CHH}	300	—	µs	*
$\overline{CE}$1 High Setup Time following CE2 High after Power Down Exit	t_{CHS}	0	—	ns	

* : Applicable also to power-up.

(4) Other Timing Parameters

Parameter	Symbol	Value		Unit	Note
		Min	Max		
$\overline{CE}$1 High to $\overline{OE}$ Invalid Time for Standby Entry	t_{CHOX}	10	—	ns	
$\overline{CE}$1 High to $\overline{WE}$ Invalid Time for Standby Entry	t_{CHWX}	10	—	ns	*1
CE2 Low Hold Time after Power-up	t_{C2LH}	50	—	µs	
$\overline{CE}$1 High Hold Time following CE2 High after Power-up	t_{CHH}	300	—	µs	
Input Transition Time	t_T	1	25	ns	*2

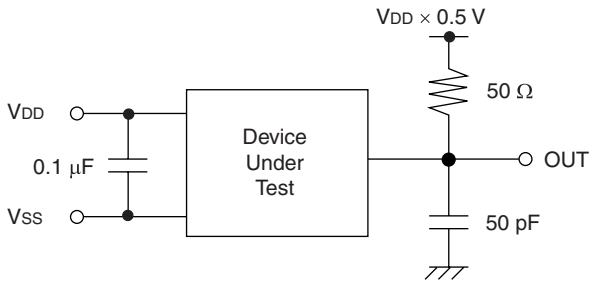
*1: Some data might be written into any address location if t_{CHWX} (Min) is not satisfied.

*2: The Input Transition Time (t_T) at AC testing is 5 ns as shown in below. If actual t_T is longer than 5 ns, it may violate AC specifications of some timing parameters.

(5) AC Test Conditions

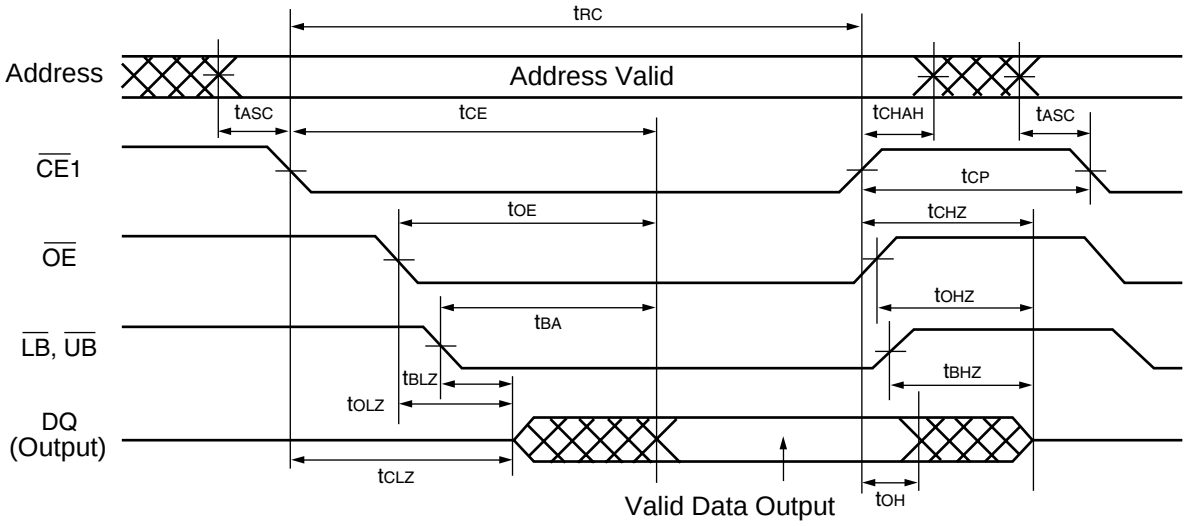
Parameter	Symbol	Conditions	Measured Value	Unit	Note
Input High Level	V_{IH}	—	$V_{DD} \times 0.8$	V	
Input Low level	V_{IL}	—	$V_{DD} \times 0.2$	V	
Input Timing Measurement Level	V_{REF}	—	$V_{DD} \times 0.5$	V	
Input Transition Time	t_T	Between V_{IL} and V_{IH}	5	ns	

(6) AC Measurement Output Load Circuit



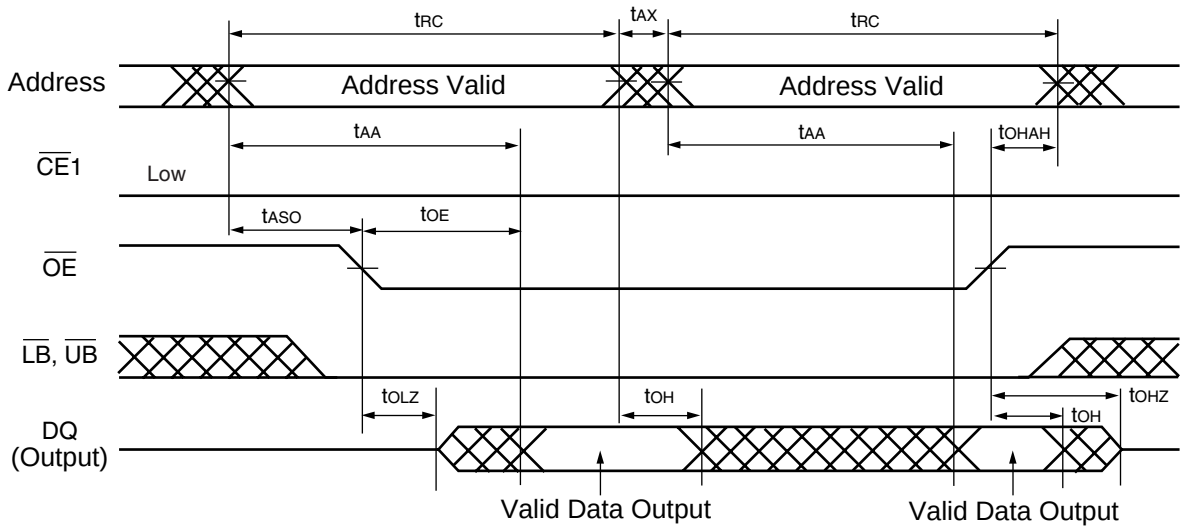
■ TIMING DIAGRAM

1. READ Timing 1 (Basic Timing)



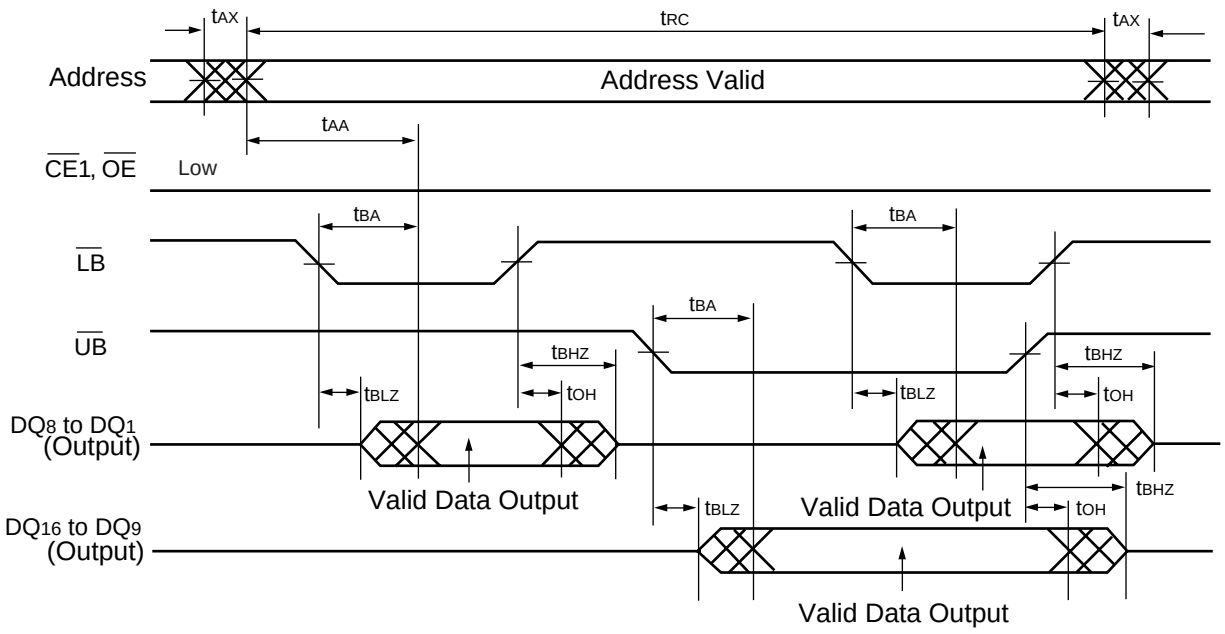
Note : This timing diagram assumes CE2 = “H” and $\overline{WE}$ = “H”.

2. READ Timing 2 ($\overline{OE}$ & Address Access)



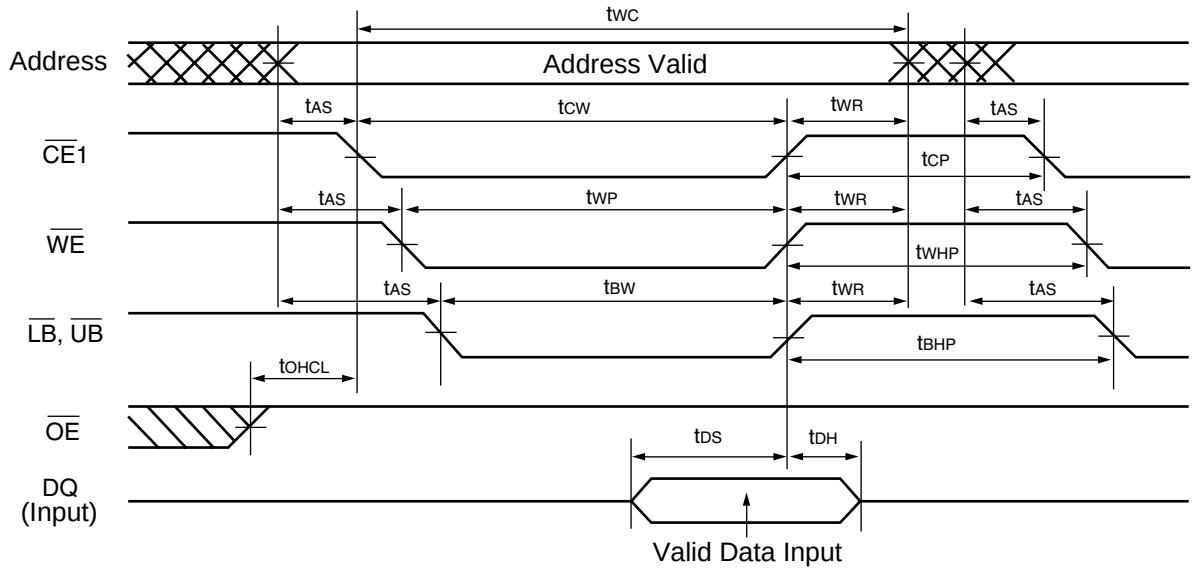
Note : This timing diagram assumes CE2 = “H” and $\overline{WE}$ = “H”.

3. READ Timing 3 ($\overline{LB}$, $\overline{UB}$ Byte Access)



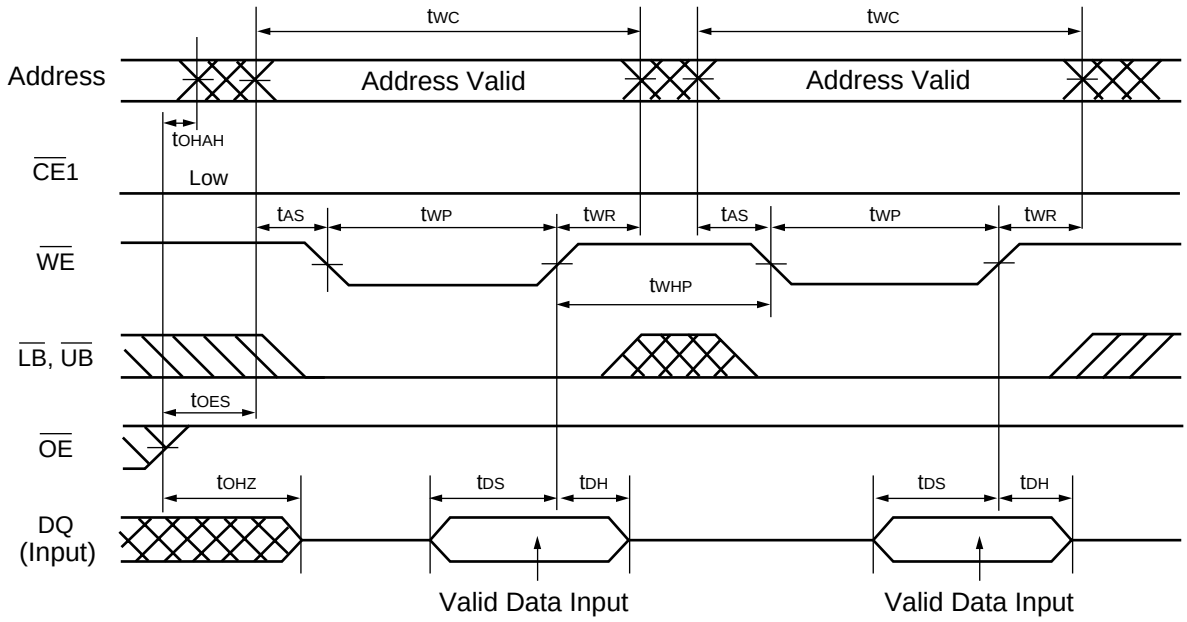
Note : This timing diagram assumes CE2 = “H” and $\overline{WE}$ = “H”.

4. WRITE Timing 1 (Basic Timing)



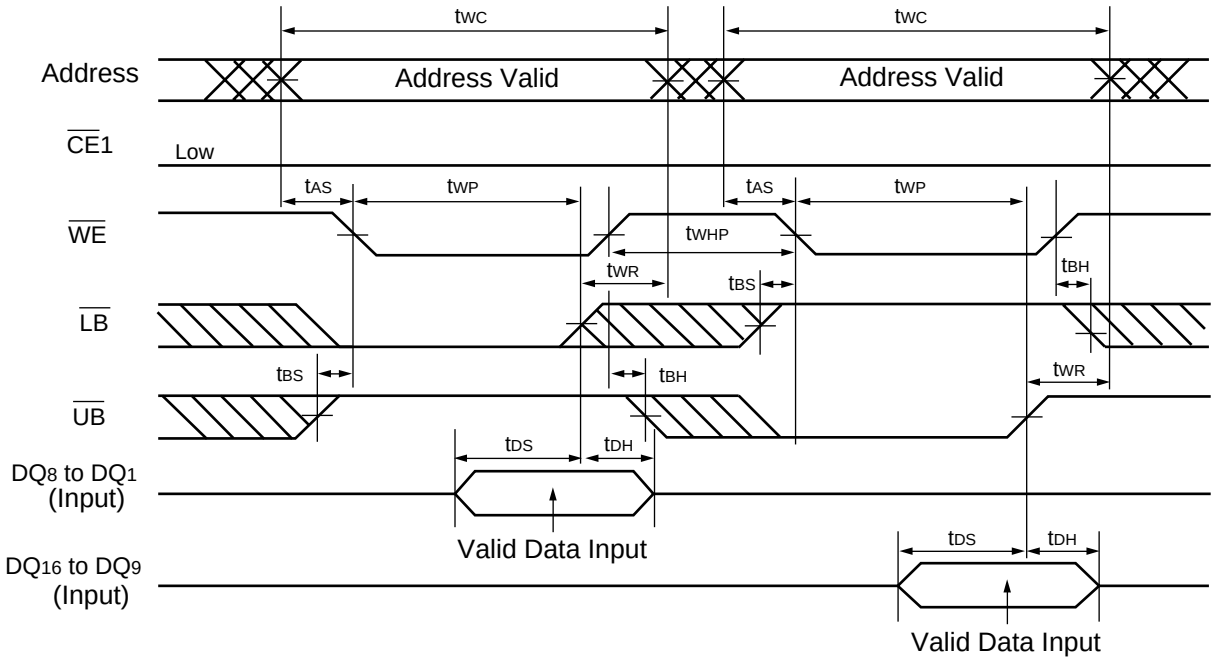
Note : This timing diagram assumes CE2 = “H”.

5. WRITE Timing 2 ($\overline{WE}$ Control)



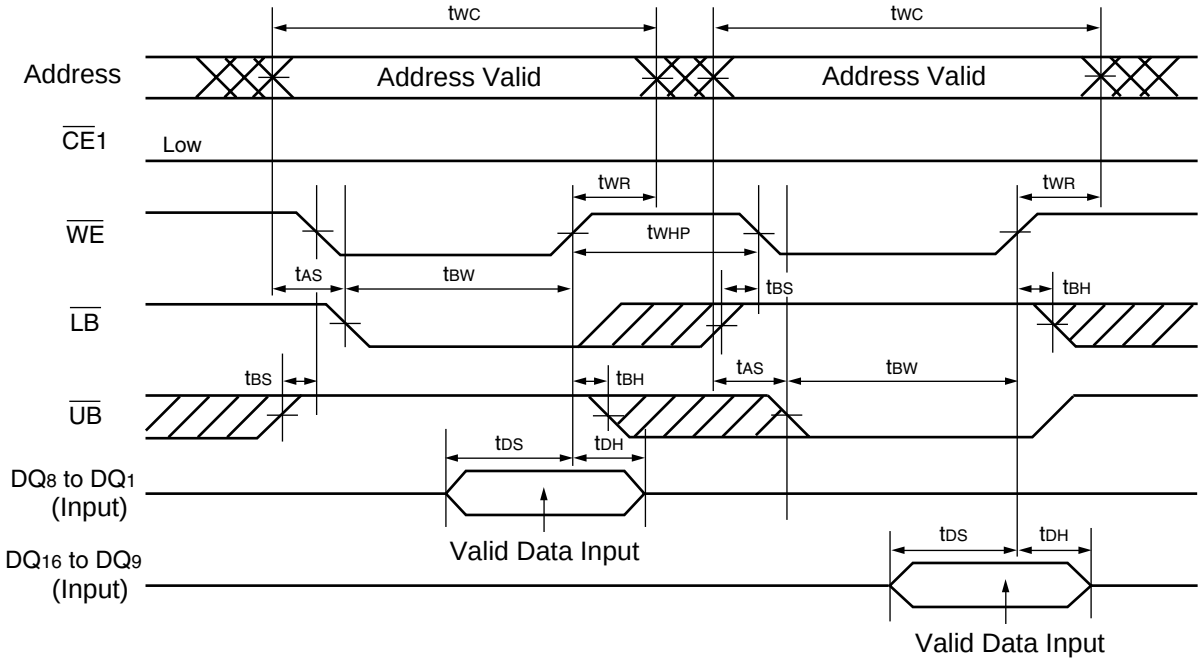
Note : This timing diagram assumes CE2 = “H”.

6. WRITE Timing 3-1 ($\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Byte Write Control)



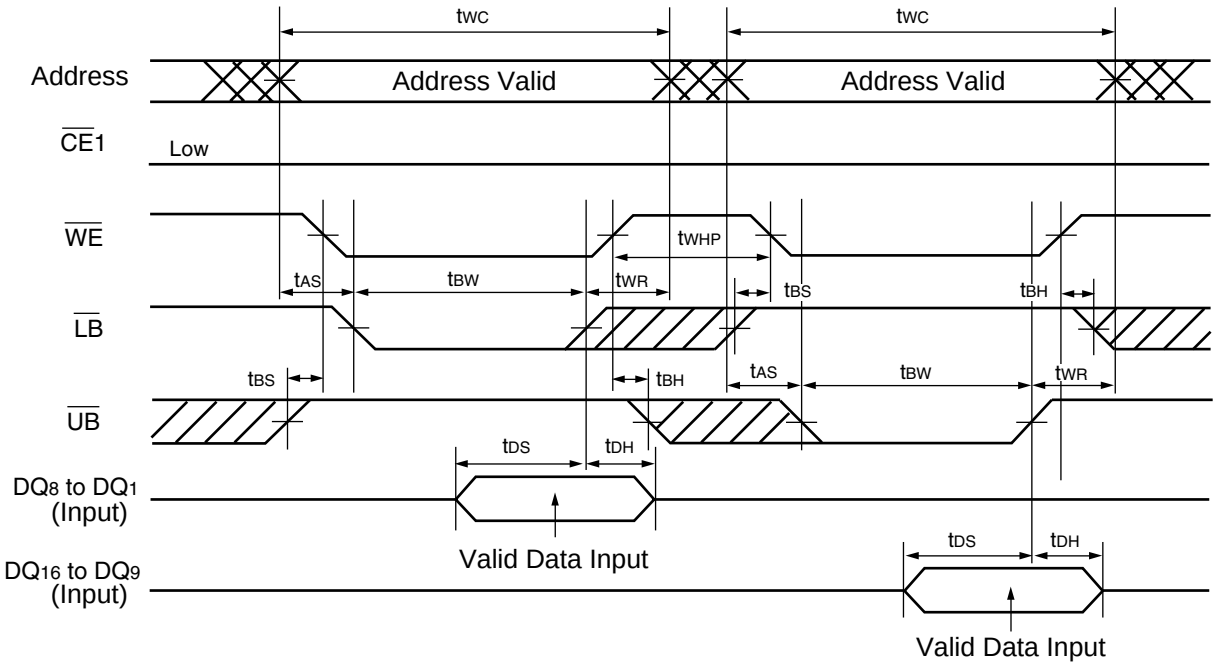
Note : This timing diagram assumes CE2 = “H” and $\overline{OE}$ = “H”.

7. WRITE Timing 3-2 ($\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Byte Write Control)



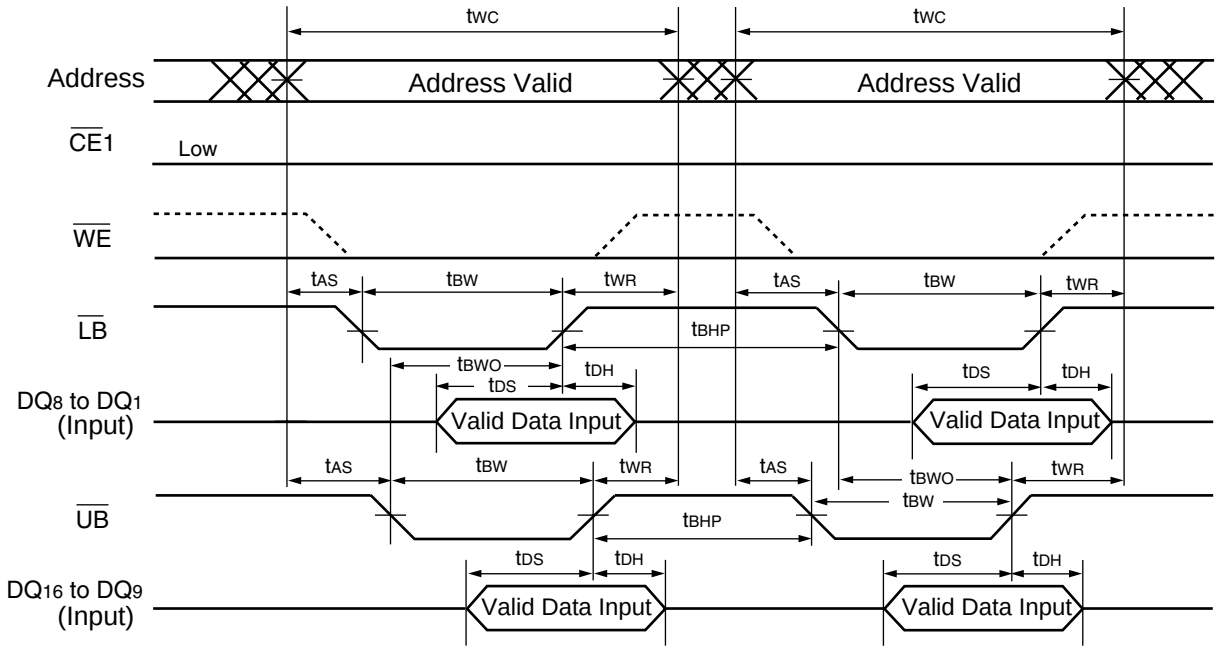
Note : This timing diagram assumes CE2 = "H" and $\overline{OE}$ = "H".

8. WRITE Timing 3-3 ($\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Byte Write Control)



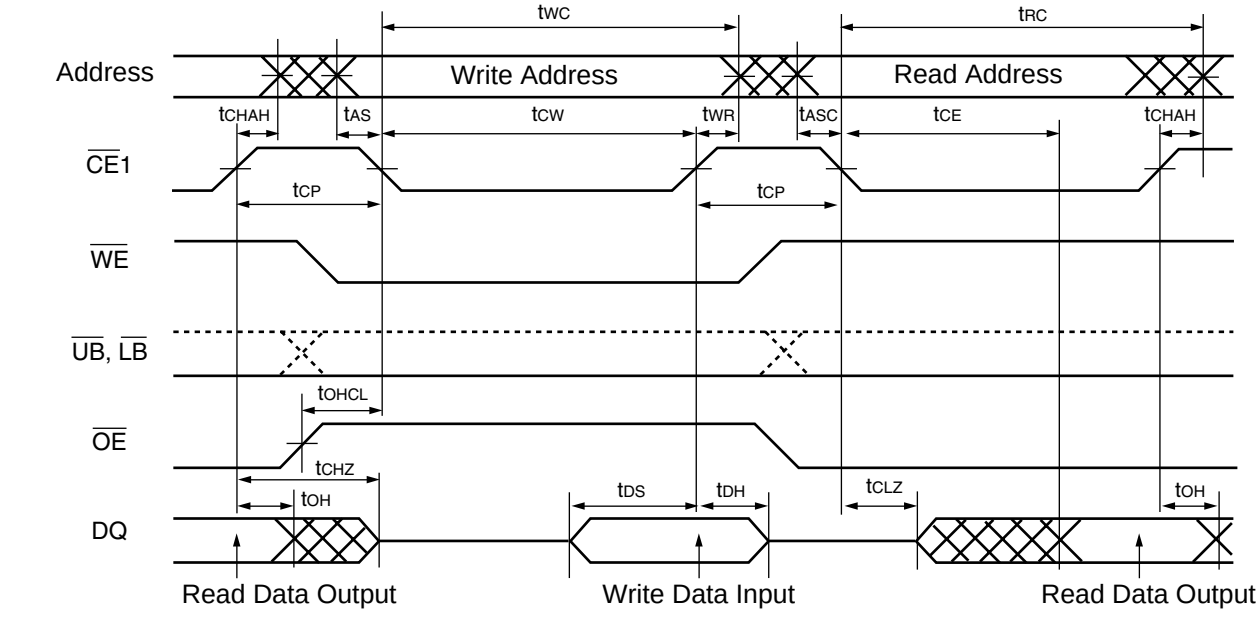
Note : This timing diagram assumes CE2 = "H" and $\overline{OE}$ = "H".

9. WRITE Timing 3-4 ($\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Byte Write Control)



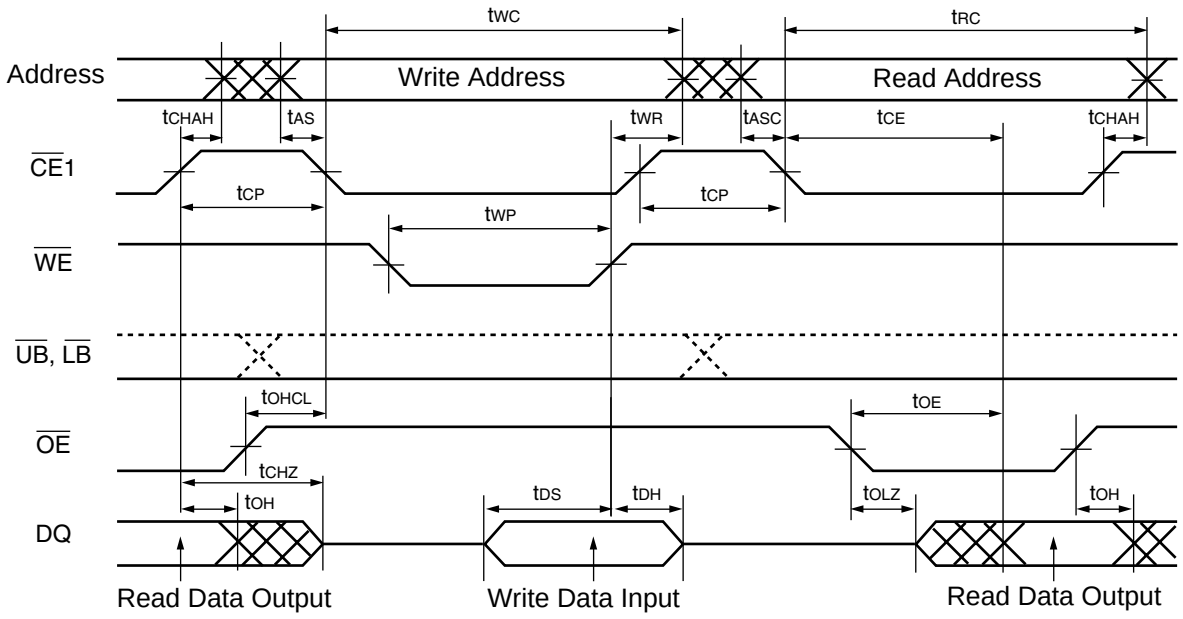
Note : This timing diagram assumes CE2 = "H" and $\overline{OE}$ = "H".

10. READ/WRITE Timing 1-1 ($\overline{CE}$1 Control)



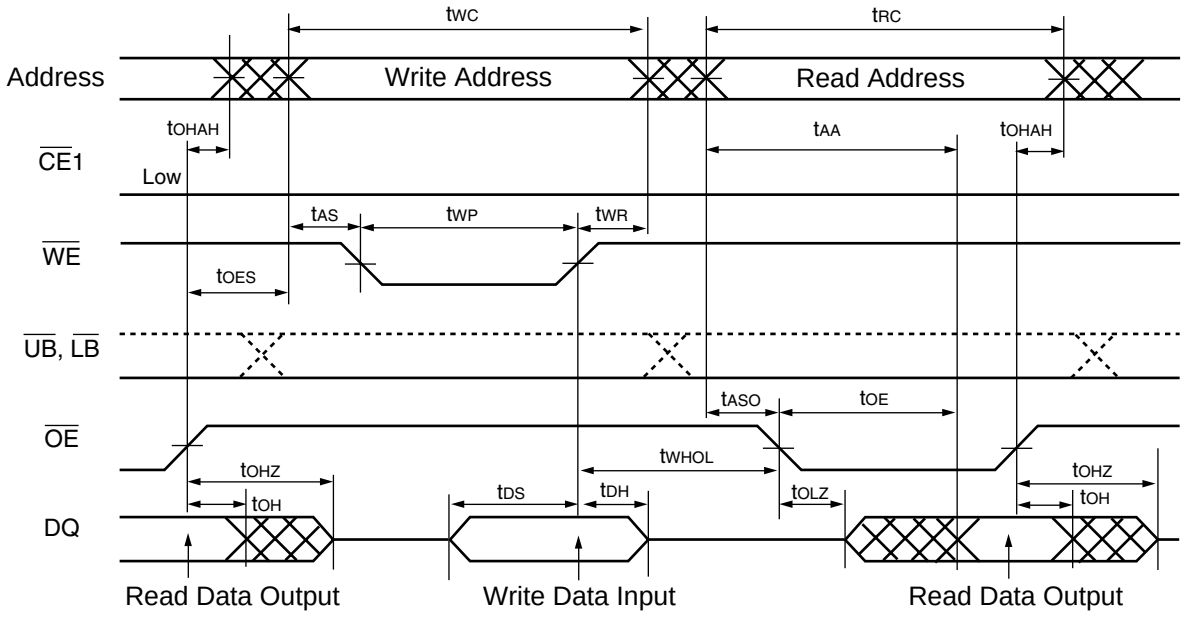
Note : This timing diagram assumes CE2 = "H".
Write address is valid from either $\overline{CE}$1 or $\overline{WE}$ of last falling edge.

11. READ/WRITE Timing 1-2 ($\overline{CE}$1, $\overline{WE}$, $\overline{OE}$ Control)



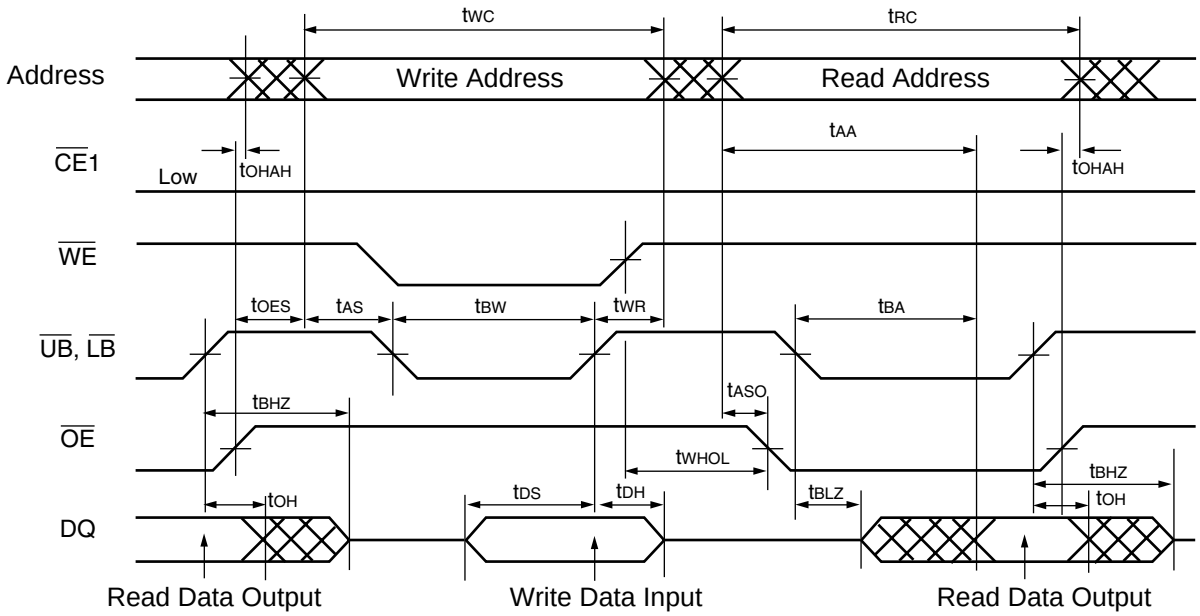
Note : This timing diagram assumes CE2 = "H".
$\overline{OE}$ can be fixed Low during write operation if it is $\overline{CE}$1 controlled write at Read-Write-Read sequence.

12. READ/WRITE Timing 2 ($\overline{OE}$, $\overline{WE}$ Control)



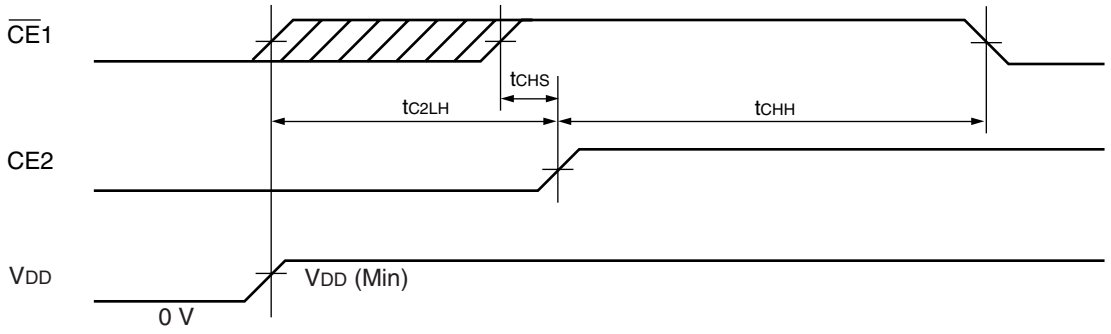
Note : This timing diagram assumes CE2 = "H".
$\overline{CE}$1 can be tied to Low for $\overline{WE}$ and $\overline{OE}$ controlled operation.

13. READ/WRITE Timing 3 ($\overline{OE}$, $\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Control)



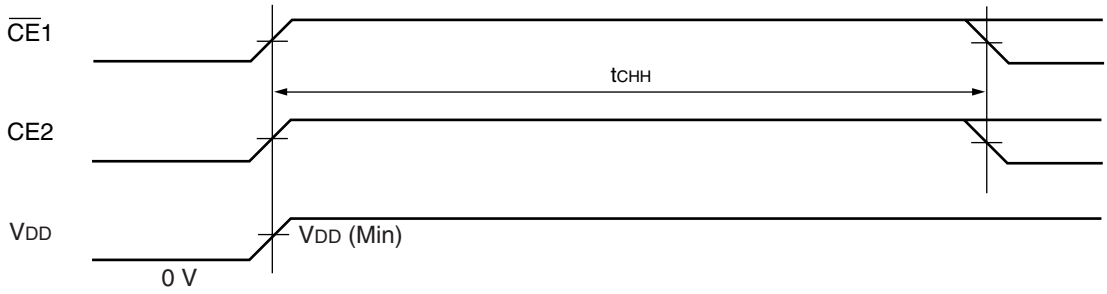
Note : This timing diagram assumes CE2 = "H".
$\overline{CE}$1 can be tied to Low for $\overline{WE}$ and $\overline{OE}$ controlled operation.

14. POWER-UP Timing 1



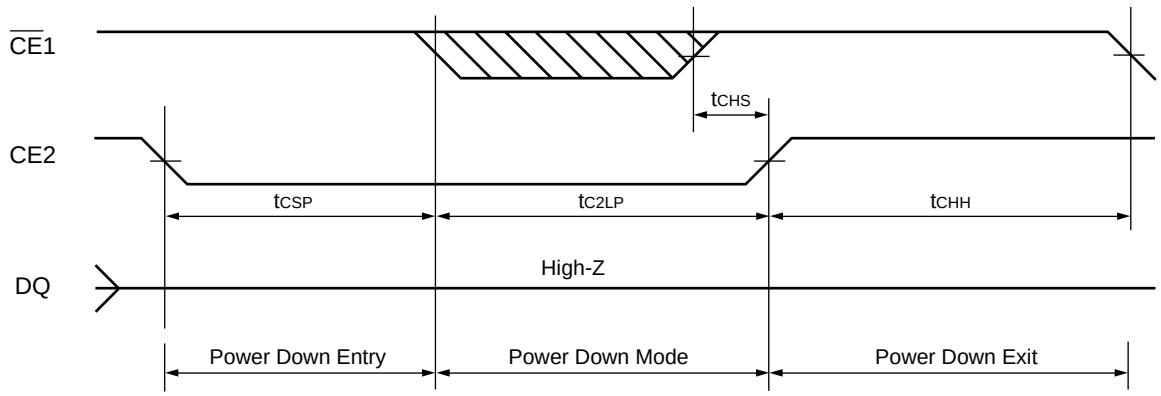
Note : t_{C2LH} specifies after V_{DD} reaches specified minimum level.

15. POWER-UP Timing 2



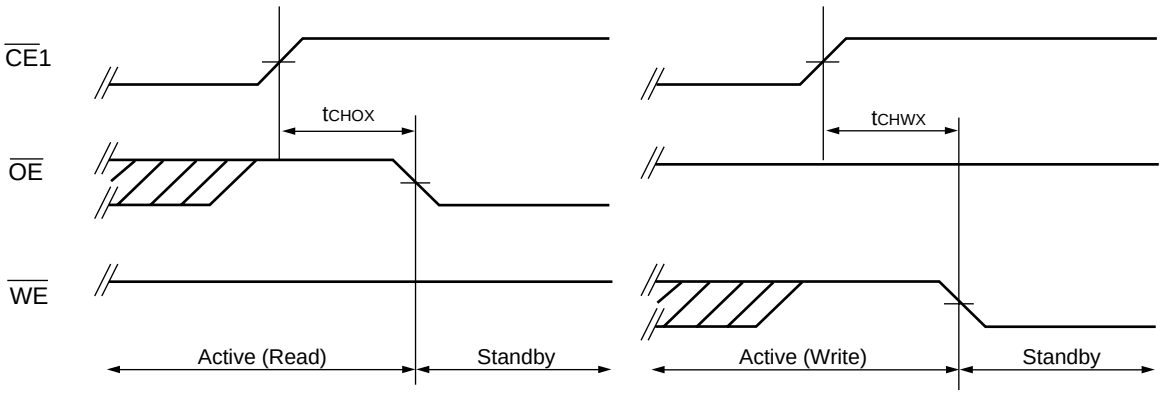
Note : t_{CHH} specifies after V_{DD} reaches specified minimum level and applicable to both $\overline{CE}1$ and CE2.
If transition time of V_{DD} (from 0 V to V_{DD} Min) is longer than 100 ms, POWER-UP Timing#1 must be applied.

16. POWER DOWN Entry and Exit Timing



Note : This Power Down mode can be also used as a reset timing if POWER-UP timing could not be satisfied.

17. Standby Entry Timing after Read or Write



Note : Both t_{CHOX} and t_{CHWX} define the earliest entry timing for Standby mode.
If either of timing is not satisfied, it takes t_{RC} (Min) period for Standby mode from $\overline{CE}1$ Low to High transition.

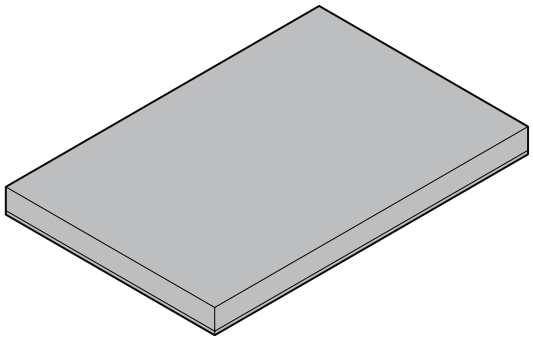
■ BONDING PAD INFORMATION

Please contact local FUJITSU representative for pad layout and pad coordinate information.

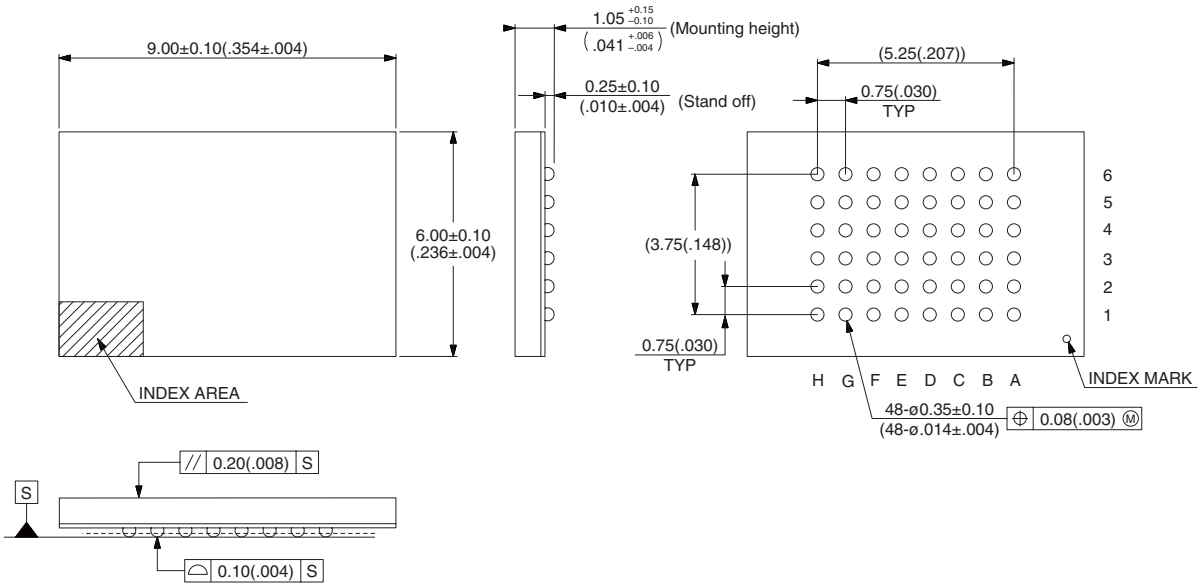
■ ORDERING INFORMATION

Part No.	Shipping Form/Package	Remarks
MB82D01181E-60LWT	Wafer	
MB82D01181E-60LPBN	48-pin plastic FBGA (BGA-48P-M18)	SRAM compatible FBGA package t_{CE} = 60 ns Max

■ PACKAGE DIMENSION

48-pin plastic FBGA		
	Ball pitch	0.75 mm
	Package width × package length	6.00 × 9.00 mm
	Lead shape	Fine pitch ball
	Sealing method	Plastic mold
	Mounting height	1.20 mm MAX
	Weight	0.10 g
(BGA-48P-M18)		

48-pin plastic FBGA
(BGA-48P-M18)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

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