

**Phase-out/Discontinued****NPN SILICON POWER TRANSISTOR ARRAY  
MEDIUM SWITCHING USE****DESCRIPTION**

The  $\mu$ PA1424 is NPN silicon epitaxial Power Transistor Array that built in resistance and 4 circuits designed for driving solenoid, relay, lamp and so on.

**FEATURES**

- Easy mount by 0.1 inch of terminal interval.
- Zener Diode built in, for Surge Absorbing.
- Bias Resistance built in.  
 $R_1 = 680 \Omega$ ,  $R_2 = 10 \text{ k}\Omega$
- Low Power loss when driving actuator.  
 $V_{OL} \leq 0.4 \text{ V}$  @  $V_{in} = 4.2 \text{ V}$ ,  $I_c = 0.8 \text{ A}$   
 $V_{OL} \leq 0.5 \text{ V}$  @  $V_{in} = 4.2 \text{ V}$ ,  $I_c = 1.0 \text{ A}$

**ORDERING INFORMATION**

Part Number	Package	Quality Grade
$\mu$ PA1424H	10 Pin SIP	Standard

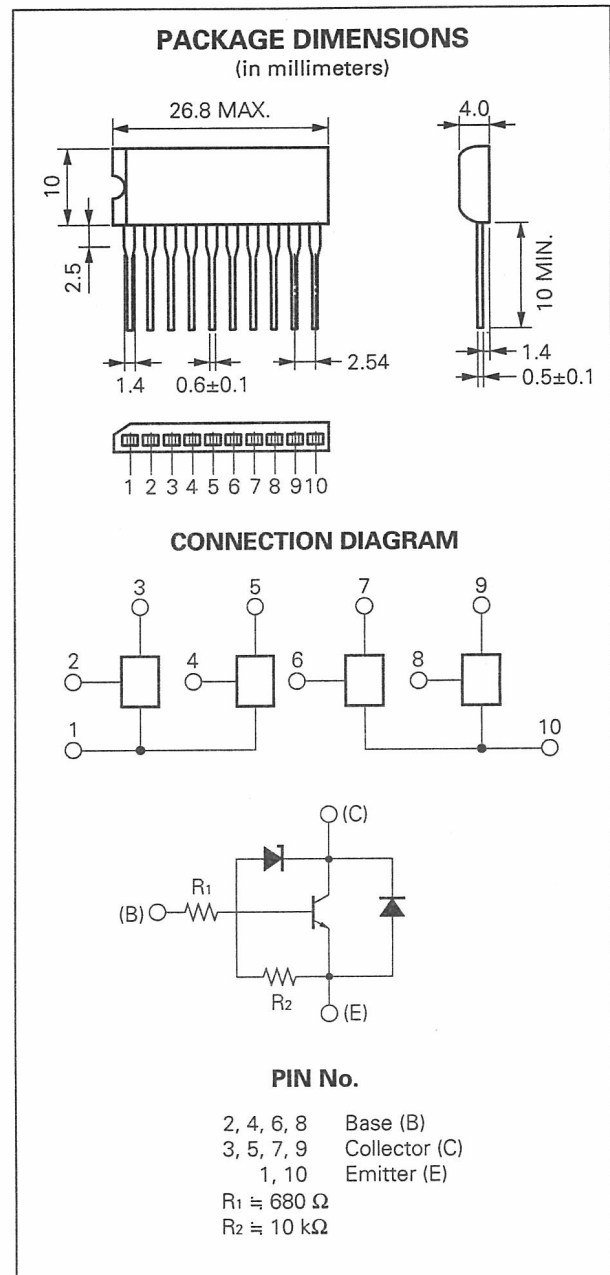
Please refer to "Quality grade on NEC Semiconductor Device" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

**ABSOLUTE MAXIMUM RATINGS ( $T_a = 25 \text{ }^\circ\text{C}$ )**

Collector to Base Voltage	$V_{CBO}$	$60 \pm 10$	V
Collector to Emitter Voltage	$V_{CEO}$	$60 \pm 10$	V
Emitter to Base Voltage	$V_{EBO}$	15	V
Collector Current (DC)	$I_{c(DC)}$	$\pm 2$	A/unit
Collector Current (pulse)	$I_{c(pulse)^*}$	$\pm 3$	A/unit
Base Current (DC)	$I_{B(DC)}$	0.03	A/unit
Total Power Dissipation ( $T_a = 25 \text{ }^\circ\text{C}$ )	$P_{T1}^{**}$	3.5	W
Total Power Dissipation ( $T_c = 25 \text{ }^\circ\text{C}$ )	$P_{T2}^{**}$	28	W
Junction Temperature	$T_j$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

\*  $PW \leq 10 \text{ ms}$ , Duty Cycle  $\leq 50 \%$

\*\* 4 Circuits



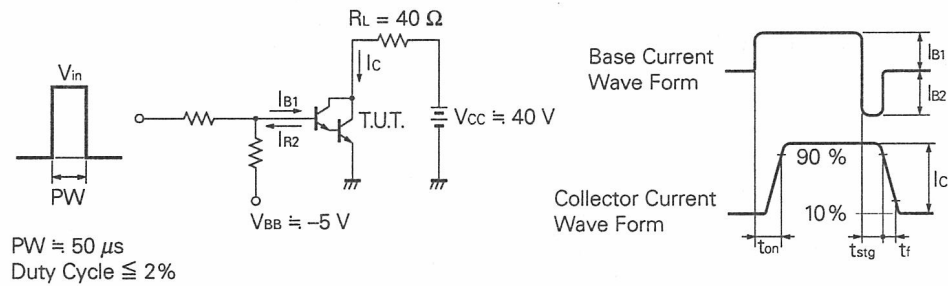
The information in this document is subject to change without notice.

**ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C)**

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Collector to Emitter Voltage	V <sub>CE0(sus)</sub>	50	60		V	I <sub>c</sub> = 2 A, I <sub>B</sub> = 5 mA, L = 6 mH
Collector Leakage Current	I <sub>CBO</sub>			100	nA	V <sub>CB</sub> = 40 V, I <sub>E</sub> = 0
DC Current Gain	h <sub>FE1</sub> *	700	1 200		-	V <sub>CE</sub> = 5 V, I <sub>c</sub> = 0.2 A
DC Current Gain	h <sub>FE2</sub> *	1 000	1 700	3 000	-	V <sub>CE</sub> = 5 V, I <sub>c</sub> = 1 A
DC Current Gain	h <sub>FE3</sub> *	500	1 300		-	V <sub>CE</sub> = 5 V, I <sub>c</sub> = 2 A
Low-Level Output Voltage	V <sub>OL1</sub> *			0.4	V	V <sub>in</sub> = 4.2 V, I <sub>c</sub> = 0.8 A
Low-Level Output Voltage	V <sub>OL2</sub> *			0.5	V	V <sub>in</sub> = 4.2 V, I <sub>c</sub> = 1 A
Low-Level Input Voltage	V <sub>IL</sub> *	400			mV	V <sub>CE</sub> = 12 V, I <sub>c</sub> = 0.1 mA
Input Resistance 1	R <sub>1</sub>	476	680	884	Ω	
Input Resistance 2	R <sub>2</sub>	7	10	13	kΩ	
Turn On Time	t <sub>on</sub>		0.4		μs	I <sub>c</sub> = 1 A, see Fig. 1
Storage Time	t <sub>stg</sub>		1.4		μs	I <sub>B1</sub> = -I <sub>B2</sub> = 10 mA
Fall Time	t <sub>f</sub>		0.5		μs	V <sub>CC</sub> ≅ 20 V, R <sub>L</sub> = 20 Ω

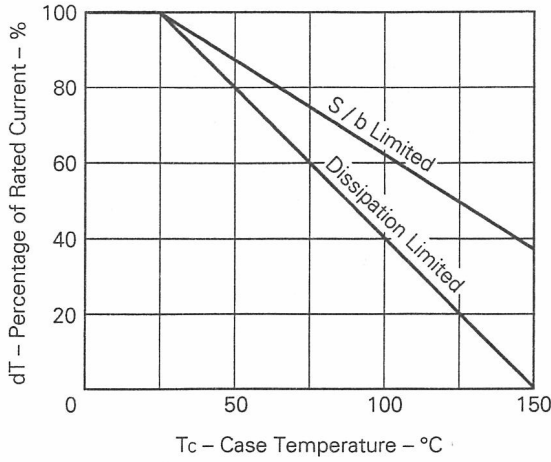
\* Pulsed : PW ≲ 350 μs, Duty Cycle ≲ 2 %

**Fig. 1. SWITCHING TIME TEST CIRCUIT**

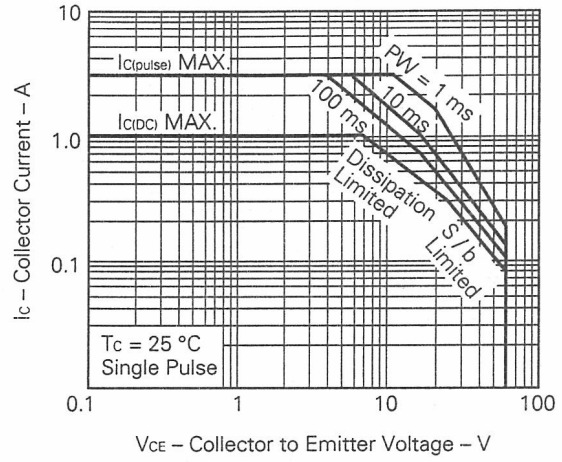


TYPICAL CHARACTERISTICS ( $T_a = 25\text{ }^\circ\text{C}$ )

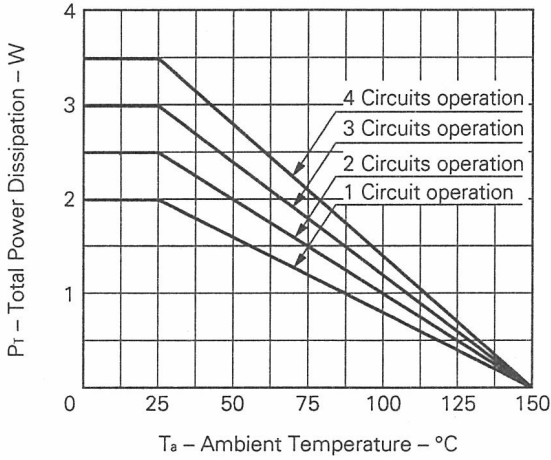
DERATING CURVE OF SAFE OPERATING AREA



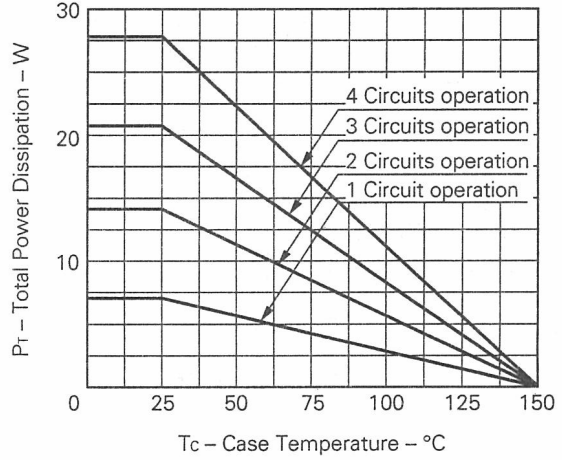
SAFE OPERATING AREA



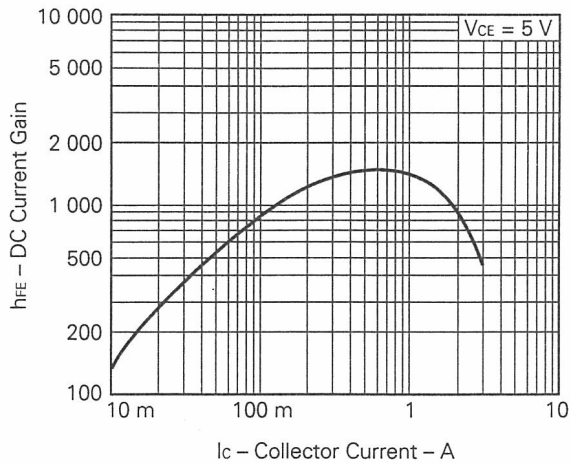
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



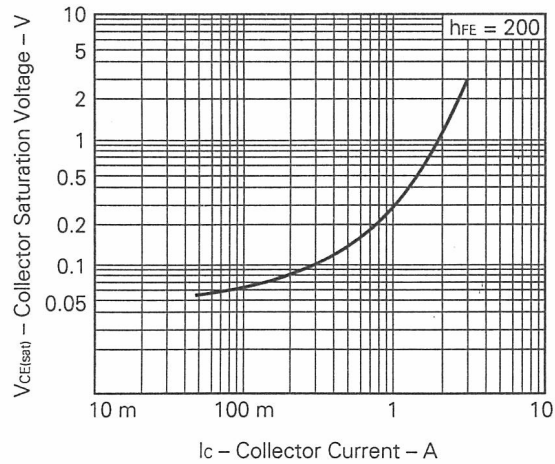
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



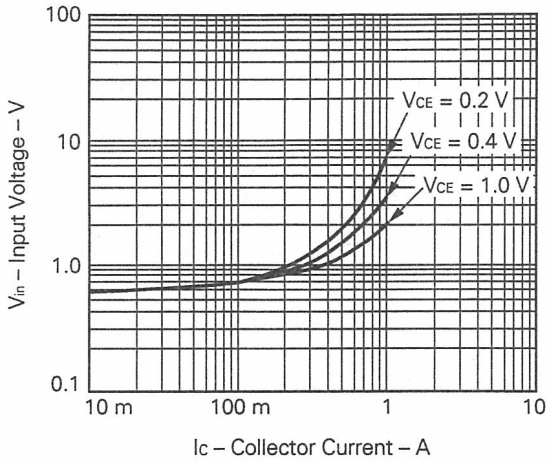
DC CURRENT GAIN vs. COLLECTOR CURRENT



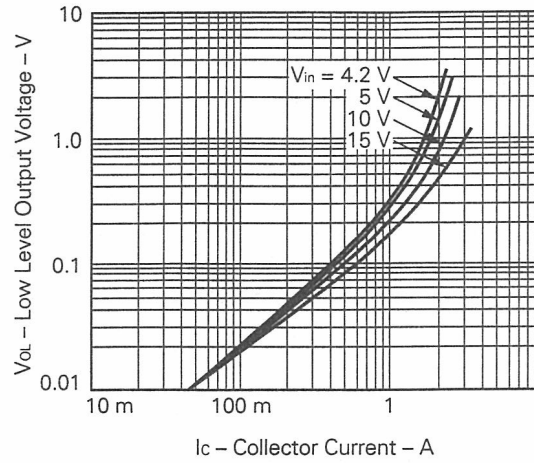
COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT



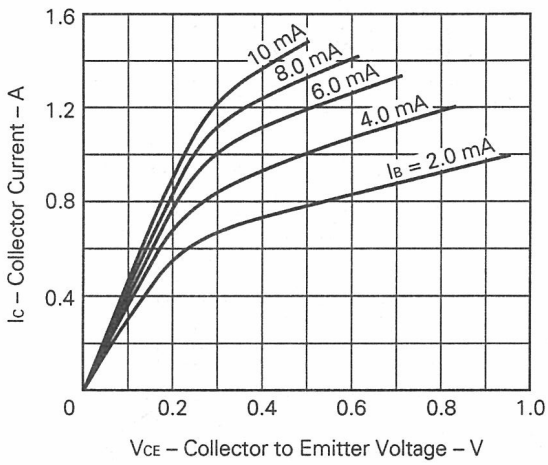
INPUT VOLTAGE vs. COLLECTOR CURRENT



LOW LEVEL OUTPUT VOLTAGE vs. COLLECTOR CURRENT



COLLECTOR CURRENT vs. COLLECTOR TO EMITTER VOLTAGE



## REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134

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