

# SILICON TRANSISTOR ARRAY

# $\mu$ PA1454

### NPN SILICON POWER TRANSISTOR ARRAY

### LOW SPEED SWITCHING USE

### INDUSTRIAL USE

#### DESCRIPTION

The  $\mu$ PA1454 is NPN silicon epitaxial Power Transistor Array that built in 4 circuits designed for driving solenoid, relay, lamp and so on.

#### FEATURES

- Easy mount by 0.1 inch of terminal interval.
- High  $h_{FE}$ . Low  $V_{CE(sat)}$ .  
 $h_{FE} = 800$  to  $3200$  (at  $I_c = 1$  A)  
 $V_{CE(sat)} = 1.0$  V MAX. (at  $I_c = 3$  A)

#### ORDERING INFORMATION

Part Number	Package	Quality Grade
$\mu$ PA1454H	10 Pin SIP	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

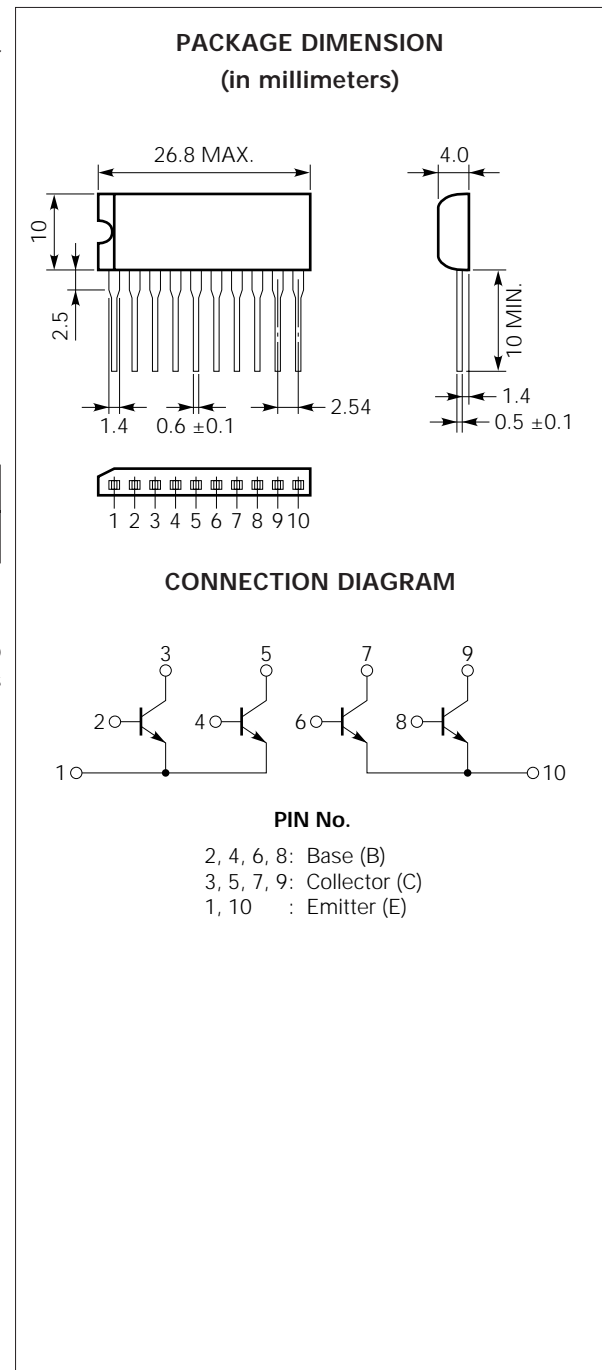
#### ABSOLUTE MAXIMUM RATINGS ( $T_a = 25$ °C)

Collector to Base Voltage	$V_{CBO}$	100	V
Collector to Emitter Voltage	$V_{CEO}$	100	V
Emitter to Base Voltage	$V_{EBO}$	7	V
Collector Current (DC)	$I_{C(DC)}$	5	A/unit
Collector Current (pulse)	$I_{C(pulse)^*}$	10	A/unit
Base Current (DC)	$I_{B(DC)}$	1.0	A/unit
Total Power Dissipation	$P_{T1}^{**}$	3.5	W
Total Power Dissipation	$P_{T2}^{***}$	28	W
Junction Temperature	$T_j$	150	°C
Storage Temperature	$T_{stg}$	-55 to +150	°C

\*  $PW \leq 300 \mu s$ , Duty Cycle  $\leq 10$  %

\*\* 4 Circuits,  $T_a = 25$  °C

\*\*\* 4 Circuits,  $T_c = 25$  °C



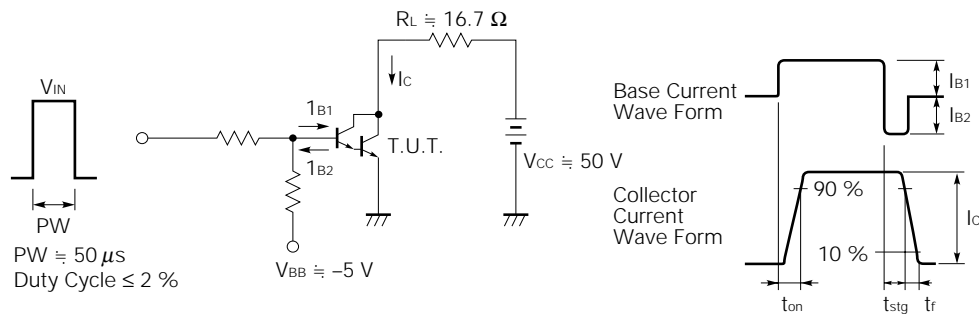
The information in this document is subject to change without notice.

**ELECTRICAL CHARACTERISTICS (Ta = 25 °C)**

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Collector Leakage Current	$I_{CBO}$			10	μA	$V_{CB} = 100 V, I_E = 0$
Emitter Leakage Current	$I_{EBO}$			10	μA	$V_{EB} = 7 V, I_C = 0$
DC Current Gain	$h_{FE1}$ *	800	1300	3200	—	$V_{CE} = 5 V, I_C = 1 A$
DC Current Gain	$h_{FE2}$ *	500	1000		—	$V_{CE} = 5 V, I_C = 3 A$
Collector Saturation Voltage	$V_{CE(sat)}$ *			1.0	V	$I_C = 3 A, I_B = 30 mA$
Base Saturation Voltage	$V_{BE(sat)}$ *			1.2	V	$I_C = 3 A, I_B = 30 mA$
Turn On Time	$t_{on}$		1		μS	$I_C = 3 A$
Storage Time	$t_{stg}$		3		μS	$I_{B1} = -I_{B2} = 30 mA$
Fall Time	$t_f$		1.5		μS	$V_{CC} \cong 50 V, R_L \cong 16.7 \Omega$ See test circuit

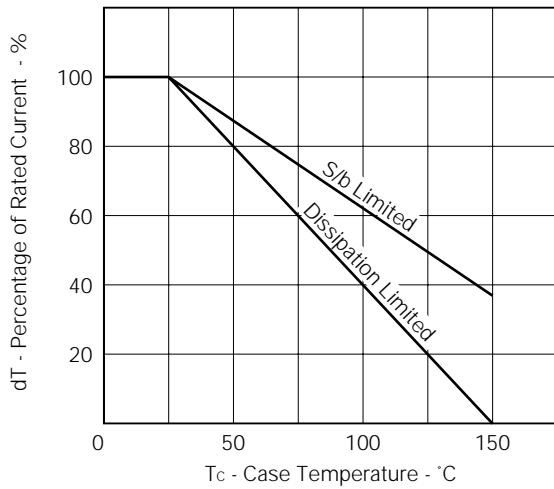
\*  $PW \leq 350 \mu s$ , Duty Cycle  $\leq 2\%$  / pulsed

**SWITCHING TIME TEST CIRCUIT**

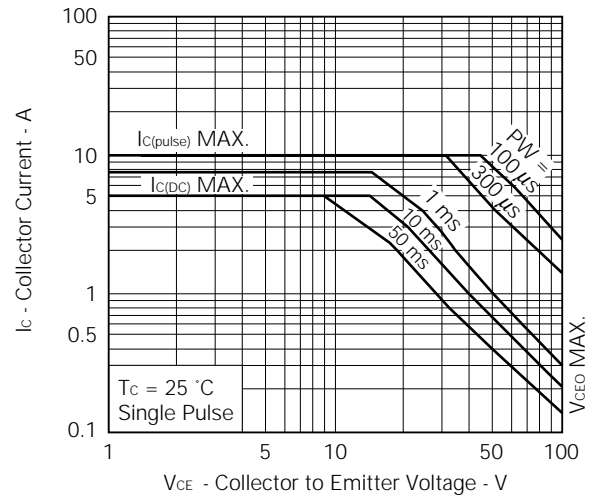


TYPICAL CHARACTERISTICS ( $T_a = 25^\circ\text{C}$ )

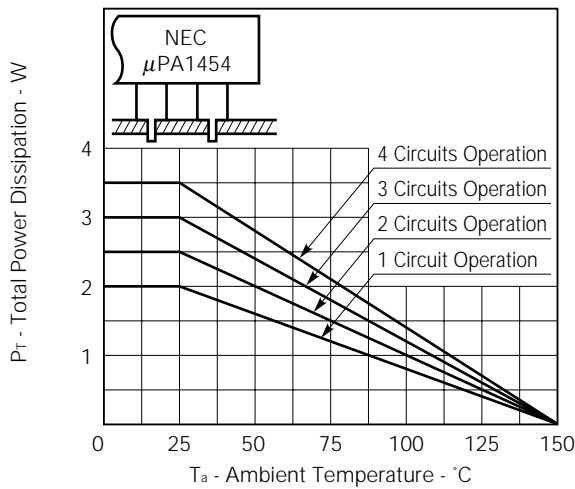
DERATING CURVE OF SAFE OPERATING AREA



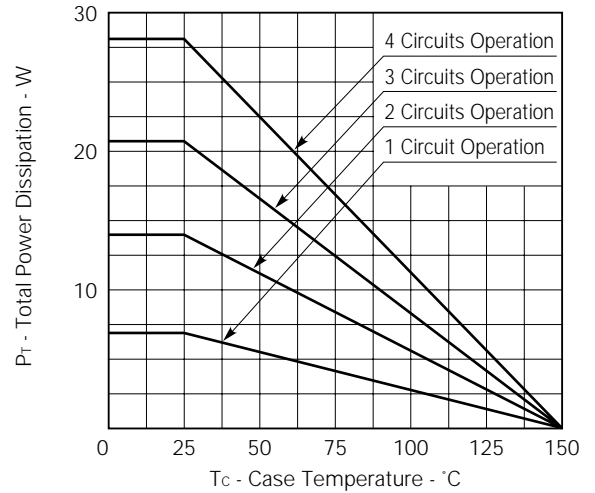
SAFE OPERATING AREA



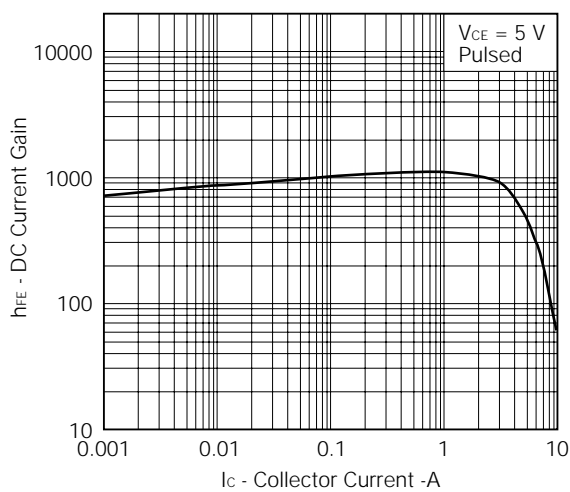
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



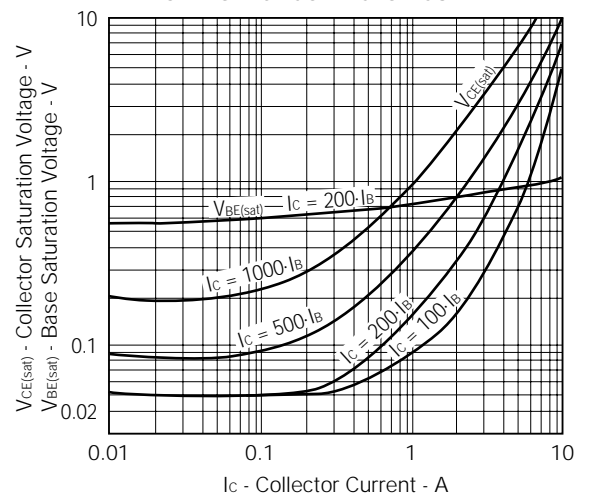
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

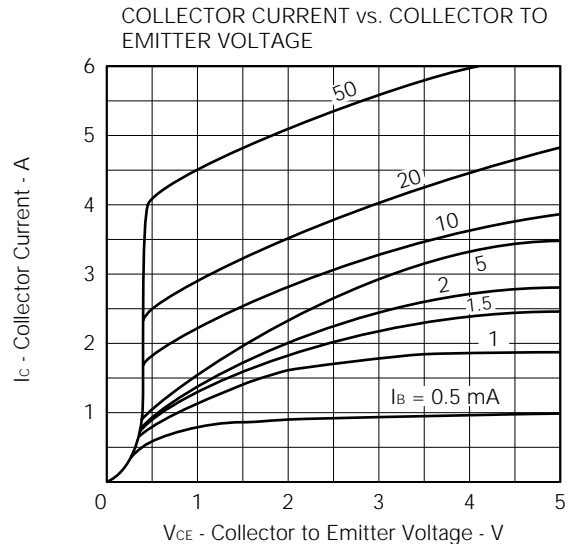
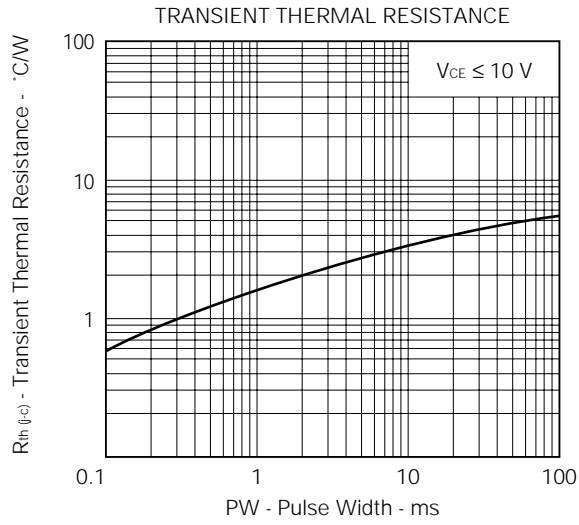


DC CURRENT GAIN vs. COLLECTOR CURRENT



BASE AND COLLECTOR SATURATION VOLTAGE vs. COLLECTOR CURRENT





## REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134

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