NEC

COMPOUND FIELD EFFECT POWER TRANSISTOR

Phase-out/Discontinued

μPA1570

N–CHANNEL POWER MOS FET ARRAY SWITCHING TYPE

DESCRIPTION

The μPA1570 is N-channel Power MOS FET Array that built in 4 circuits designed for solenoid, motor and lamp driver.

FEATURES

- 4 V driving is possible
- Large Current and Low On-state Resistance
  $I_{D(pulse)}$ = ±8 A
  $R_{DS(on)} \leqq 0.35\ \Omega$ MAX. (V_{GS} = 10 V)
  $R_{DS(on)} \leqq 0.50\ \Omega$ MAX. (V_{GS} = 4 V)
- 2.54 mm Pitch (0.1 inch)

ORDERING INFORMATION

Part Number	Package	Quality Grade
μPA1570H	10 pin SIP	Standard

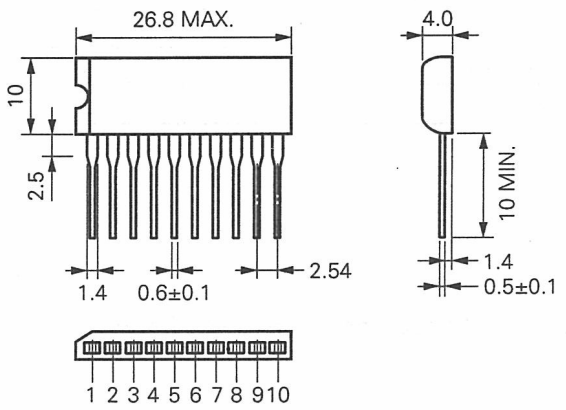
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

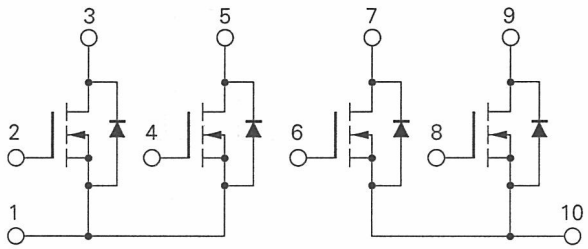
Drain to Source Voltage	V_{DSS}	30	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current (DC)	$I_{D(DC)}$	±2.0	A/unit
Drain Current (pulse)	$I_{D(pulse)}$*	±8.0	A/unit
Total Power Dissipation (4 circuits) <T_c = 25 °C>	P_{T1}	28	W
Total Power Dissipation (4 circuits) <T_a = 25 °C>	P_{T2}	3.5	W
Storage Temperature	T_{stg}	–55 to +150	°C
Junction Temperature	T_j	150	°C

* PW ≦ 300 μs, Duty Cycle ≦ 10 %

PACKAGE DIMENSIONS
(in millimeters)

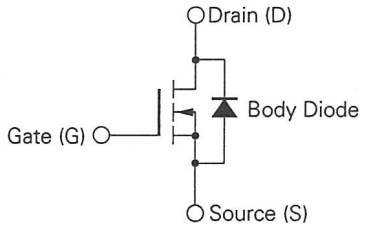


CONNECTION DIAGRAM



PIN No.

2, 4, 6, 8	Gate (G)
3, 5, 7, 9	Drain (D)
1, 10	Source (S)



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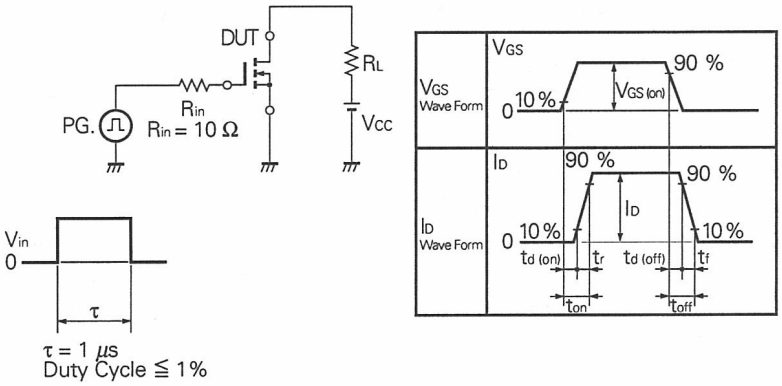
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain Leakage Current	I_{DSS}			10	μA	V_{DS} = 30 V, V_{GS} = 0
Gate to Source Leakage Current	I_{GSS}			±100	nA	V_{GS} = ±20 V, V_{DS} = 0
Gate to Source Cutoff Voltage	$V_{GS(off)}$	1.0		2.5	V	V_{DS} = 10 V, I_D = 1 mA
Forward Transfer Admittance	$\|y_{fs}\|$	1.0	1.6		S	V_{DS} = 10 V, I_D = 1 A
Drain to Source On-state Resistance	$R_{DS(on)1}$		0.2	0.35	Ω	V_{GS} = 10 V, I_D = 1 A
Drain to Source On-state Resistance	$R_{DS(on)2}$		0.35	0.50	Ω	V_{GS} = 4 V, I_D = 1.0 A
Input Capacitance	C_{iss}		270		pF	V_{DS} = 10 V V_{GS} = 0 f = 1.0 MHz
Output Capacitance	C_{oss}		150		pF	
Reverse Transfer Capacitance	C_{rss}		40		pF	
Turn-On Delay Time	$t_{d(on)}$		30		ns	I_D = 1 A V_{GS} = 10 V V_{CC} = 15 V R_L = 15 Ω, R_{in} = 10 Ω See Fig. 1
Rise Time	t_r		90		ns	
Turn-Off Delay Time	$t_{d(off)}$		400		ns	
Fall Time	t_f		250		ns	

Fig. 1 Switching Time Test Circuit



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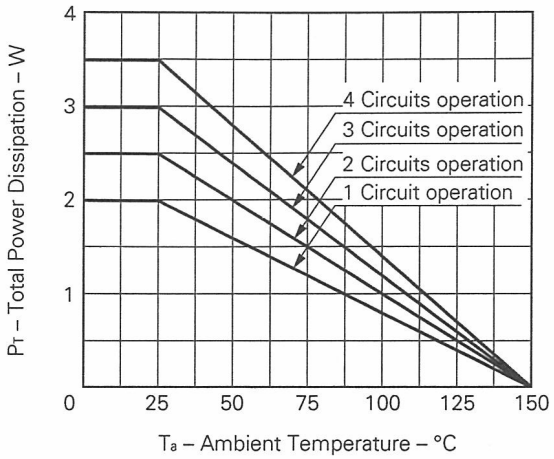
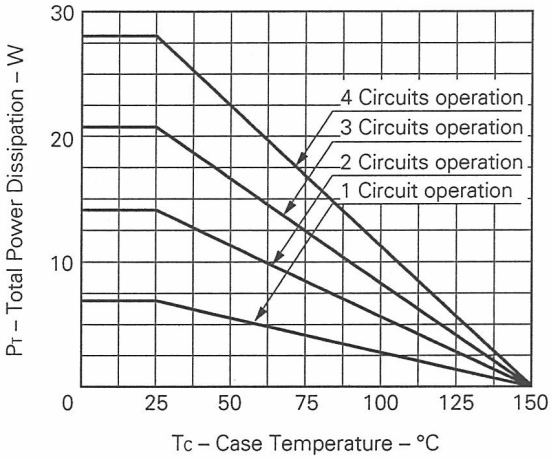
TYPICAL CHARACTERISTICS (T_a = 25 °C)

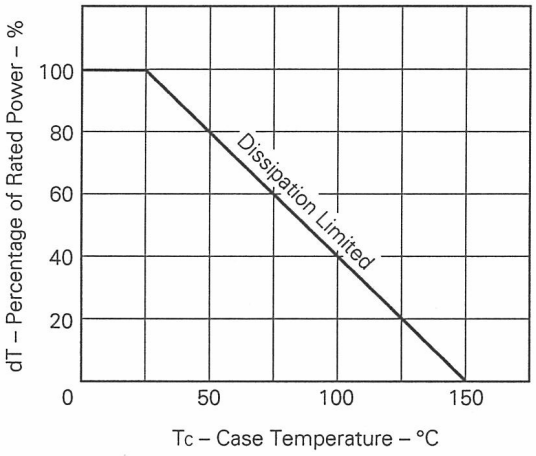
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



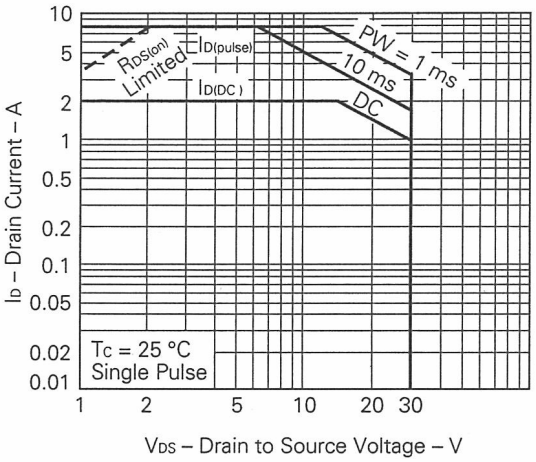
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



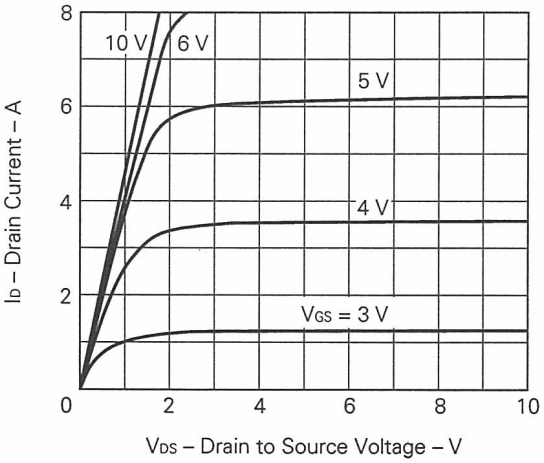
DERATING CURVE OF SAFE OPERATING AREA



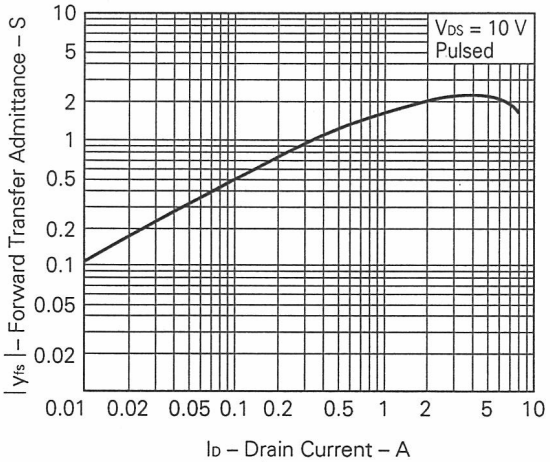
FORWARD BIAS SAFE OPERATING AREA



DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



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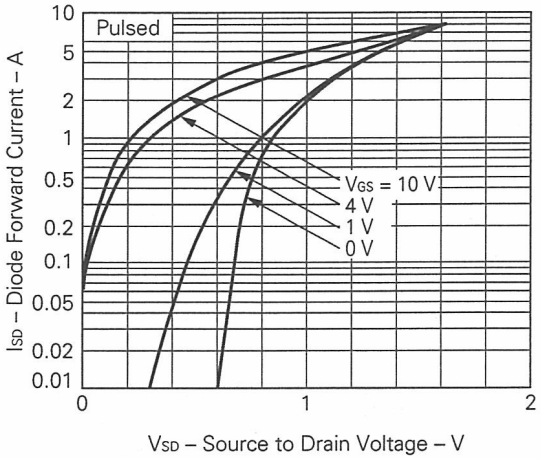
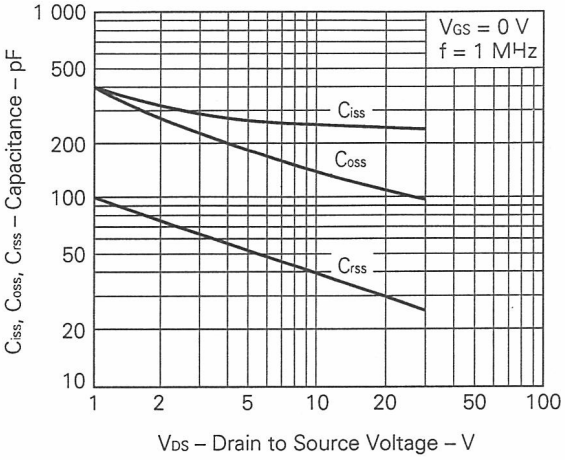
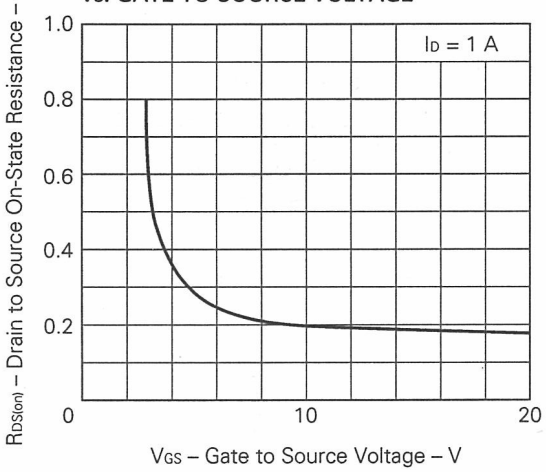
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



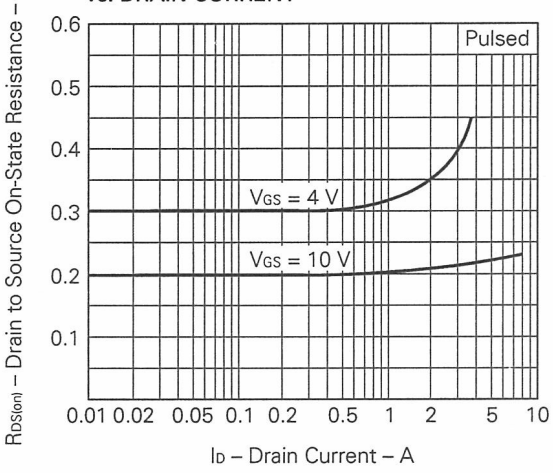
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



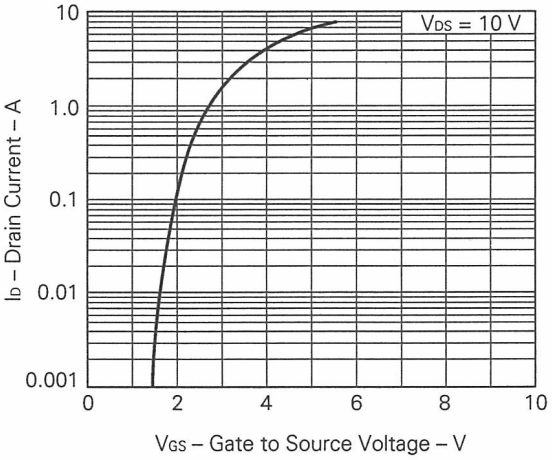
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



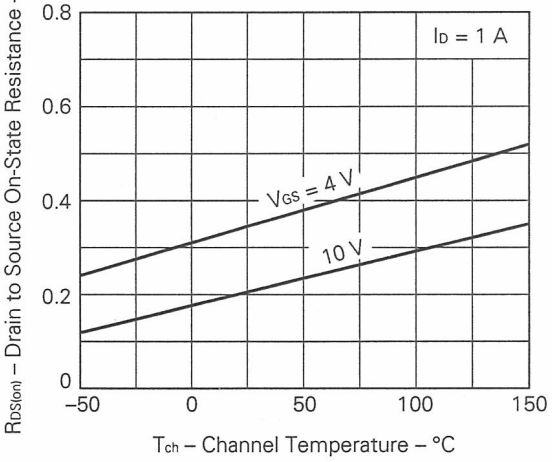
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



TRANSFER CHARACTERISTICS



DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



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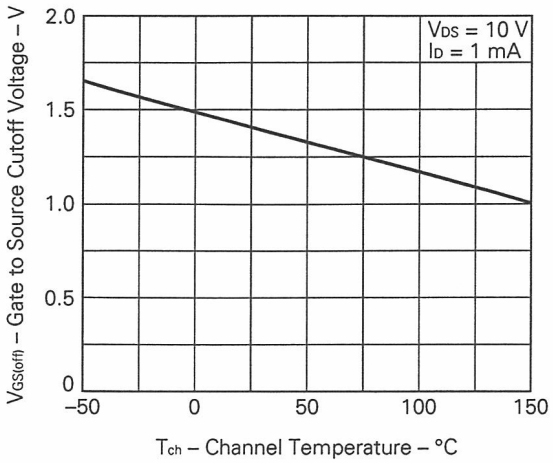
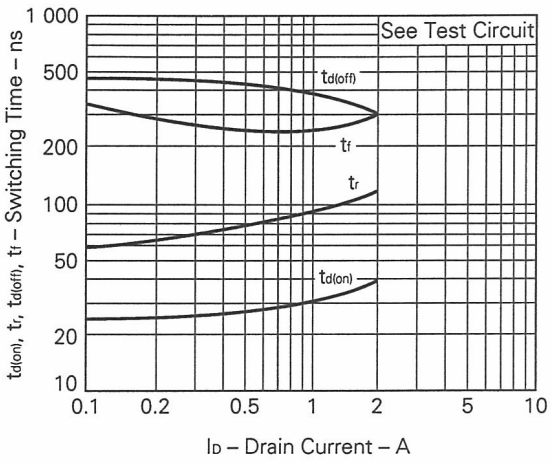
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



SWITCHING TIME vs. DRAIN CURRENT



Reference

Document name	Document No.
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207
Safe operating area of Power MOS FET	TEA-1034
Appication circuit using Power MOS FET	TEA-1035

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