

MOS FIELD EFFECT TRANSISTOR μ PA1772

SWITCHING P-CHANNEL POWER MOS FET

DESCRIPTION

The μ PA1772 is Dual P-Channel MOS Field Effect Transistor designed for power management applications of portable machines.

FEATURES

- · Dual chip type
- · Low on-state resistance

 $R_{DS(on)1}$ = 20.0 $m\Omega$ MAX. (Vgs = -10 V, Ip = -4 A)

 $R_{DS(on)2} = 29.5 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = -4.5 \text{ V, ID} = -4 \text{ A)}$

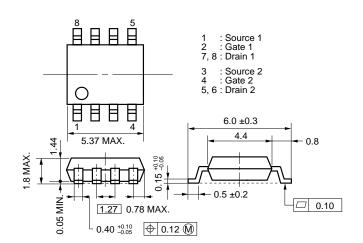
RDS(on)3 = 34.0 m Ω MAX. (VGS = -4.0 V, ID = -4 A)

- Low Ciss: Ciss = 1500 pF TYP. (VDS = -10 V, VGS = 0 V)
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA1772G	Power SOP8

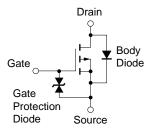
PACKAGE DRAWING (Unit: mm)



ABSOLUTE MAXIMUM RATINGS (TA = 25°C, All terminals are connected.)

Drain to Source Voltage (Vgs = 0 V)	Voss	-30	V
Gate to Source Voltage (Vps = 0 V)	Vgss	∓20	V
Drain Current (DC)	ID(DC)	∓8	Α
Drain Current (pulse) Note1	ID(pulse)	∓32	Α
Total Power Dissipation (2 unit) Note2	Рт	2.0	W
Total Power Dissipation (1 unit) Note2	Рт	1.7	W
Channel Temperature	Tch	150	°C
Storage Temperature	T_{stg}	-55 to + 150	°C

EQUIVALENT CIRCUIT (1/2 circuit)



- **Notes 1.** PW \leq 10 μ s, Duty cycle \leq 1%
 - **2.** T_A = 25° C, Mounted on ceramic substrate of 2000 mm² x 2.2 mm

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD.

When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device..

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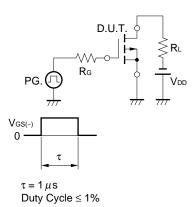


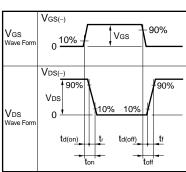
ELECTRICAL CHARACTERISTICS (TA = 25°C, All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	loss	V _{DS} = -30 V, V _{GS} = 0 V			-1	μΑ
Gate Leakage Current	Igss	V _G S = ∓20 V, V _D S = 0 V			∓10	μΑ
Gate Cut-off Voltage Note	V _{GS(off)}	$V_{DS} = -10 \text{ V}, I_{D} = -1 \text{ mA}$	-1.0	-1.7	-2.5	V
Forward Transfer Admittance Note	yfs	V _{DS} = -10 V, I _D = -4 A	6	12		S
Drain to Source On-state Resistance Note	RDS(on)1	V _G S = -10 V, I _D = -4 A		17.4	20.0	mΩ
	RDS(on)2	Vgs = -4.5 V, lb = -4 A		23.5	29.5	mΩ
	RDS(on)3	Vgs = -4.0 V, Ib = -4 A		25.8	34.0	mΩ
Input Capacitance	Ciss	V _{DS} = -10 V		1500		pF
Output Capacitance	Coss	Vgs = 0 V		550		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		240		pF
Turn-on Delay Time	td(on)	V _{DD} = -15 V, I _D = -4 A		13		ns
Rise Time	tr	Vgs = -10 V		11		ns
Turn-off Delay Time	td(off)	R _G = 10 Ω		120		ns
Fall Time	tr			70		ns
Total Gate Charge	Q _G	V _{DD} = -24 V		34		nC
Gate to Source Charge	Qgs	Vgs = -10 V		5		nC
Gate to Drain Charge	Q _{GD}	Ib = -8 A		9		nC
Body Diode Forward Voltage	V _F (S-D)	IF = 8 A, VGS = 0 V		0.84	1.2	V
Reverse Recovery Time	trr	IF = 8 A, VGS = 0 V		50		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		37		nC

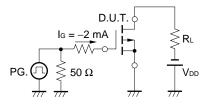
Note Pulsed: PW \leq 350 μ s, Duty cycle \leq 2%

TEST CIRCUIT 1 SWITCHING TIME

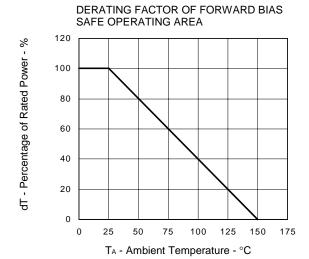




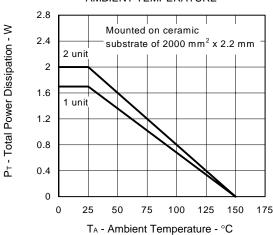
TEST CIRCUIT 2 GATE CHARGE



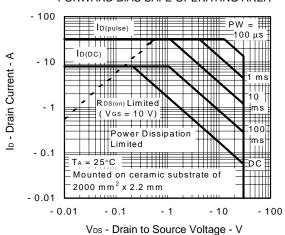
TYPICAL CHARACTERISTICS (TA = 25°C)



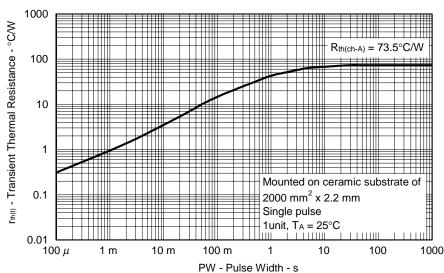
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE

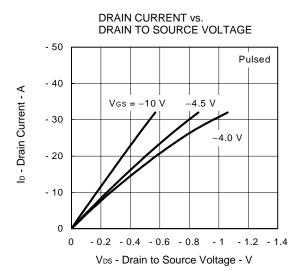


FORWARD BIAS SAFE OPERATING AREA

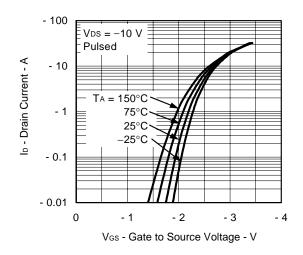


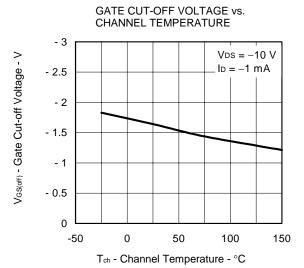
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



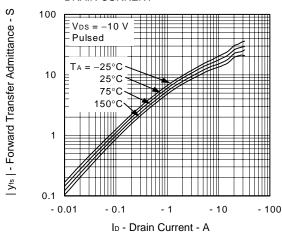


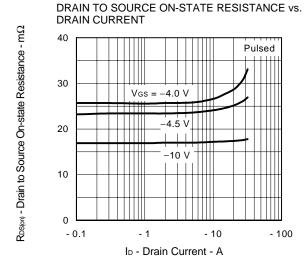
FORWARD TRANSFER CHARACTERISTICS



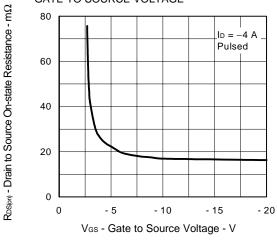


FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT





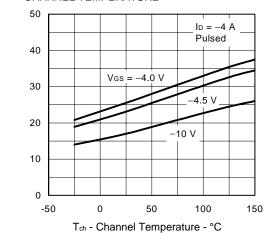
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



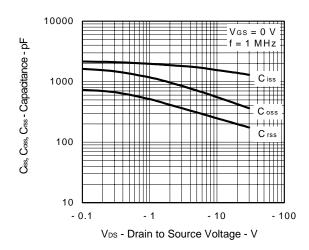


RDS(m) - Drain to Source On-state Resistance - mΩ

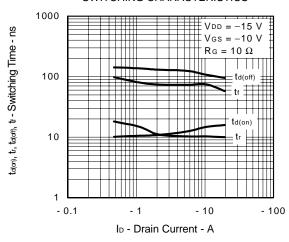
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



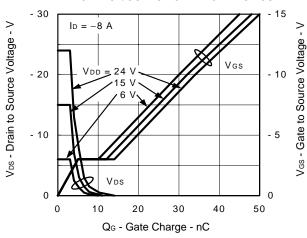
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



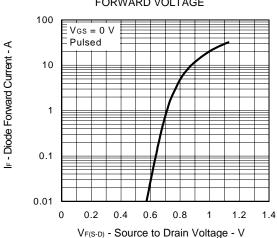
SWITCHING CHARACTERISTICS



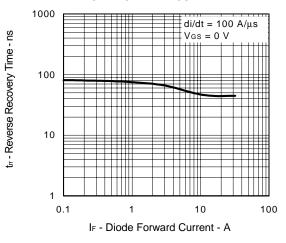
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



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