DATA SHEET



MOS FIELD EFFECT TRANSISTOR Phase-out/Discontinued μ **ΡΑ1710Α**

SWITCHING P-CHANNEL POWER MOS FET **INDUSTRIAL USE**

DESCRIPTION

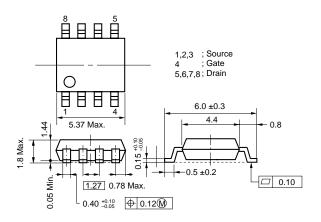
This product is P-Channel MOS Field Effect Transistor designed for DC/DC converter and power management applications of notebook computers.

FEATURES

- · Low on-resistance
- $R_{DS(on)1} = 70 \text{ m}\Omega \text{ (MAX.)} (V_{GS} = -10 \text{ V}, \text{ ID} = -2.5 \text{ A})$ $R_{DS(on)2} = 160 \text{ m}\Omega \text{ (MAX.)} (V_{GS} = -4 \text{ V}, \text{ ID} = -2.0 \text{ A})$
- Low Ciss : Ciss = 840 pF (TYP.)
- · Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μ PA1710AG	Power SOP8



PACKAGE DRAWING (Unit : mm)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, All terminals are connected.)

ABSOLUTE MAXIMUM RATINGS (TA	= 25°C, All	l terminals are co	onnected.)	EQUIVARENT CIRCUIT
Drain to Source Voltage (Vgs = 0 V)	Vdss	-30	V	
Gate to Source Voltage (Vps = 0 V)	Vgss	±20	V	Drain
Drain Current (DC)	ID(DC)	±5.0	А	. 🗖
Drain Current (pulse) Note1	D(pulse)	±20	А	Gate ⊢ Body
Total Power Dissipation $(T_A = 25^{\circ}C)^{Note2}$	P⊤	2.0	W	
Channel Temperature	Tch	150	°C	Gate
Storage Temperature	Tstg	–55 to + 150	°C	Protection Source Diode

Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1 %

- 2. Mounted on ceramic substrate of 1200 mm² x 1.1 mm
- **Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

The information in this document is subject to change without notice.

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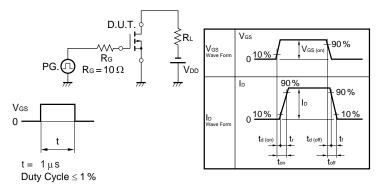
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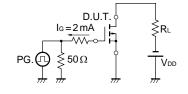
ELECTRICAL CHARACTERISTICS (TA = 25 °C, All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	RDS(on)1	Vgs = −10 V, Id = −2.5 A		45	70	mΩ
	RDS(on)2	$V_{GS} = -4 V$, $I_D = -2.0 A$		91	160	mΩ
Gate to Source Cut-off Voltage	VGS(off)	$V_{DS} = -10 V$, $I_{D} = -1 mA$	-1.0	-1.8	-2.5	V
Forward Transfer Admittance	yfs	Vds = -10 V, Id = -2.5 A	3.0	5.6		S
Drain Leakage Current	loss	$V_{DS} = -30 V$, $V_{GS} = 0 V$			-10	μA
Gate to Source Leakage Current	lgss	$V_{GS} = \pm 20 \text{ V}, \text{ V}_{DS} = 0 \text{ V}$			±10	μA
Input Capacitance	Ciss	Vbs = -10 V		840		pF
Output Capacitance	Coss	V _{GS} = 0 V		570		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		190		pF
Turn-on Delay Time	td(on)	I⊳ = −2.5 A		13		ns
Rise Time	tr	$V_{GS(on)} = -10 V$		66		ns
Turn-off Delay Time	td(off)	VDD = -15 V		82		ns
Fall Time	tr	$R_G = 10 \Omega$		52		ns
Total Gate Charge	QG	I⊳ = −5.0 A		27.3		nC
Gate to Source Charge	QGS	$V_{DD} = -24 V$		2.7		nC
Gate to Drain Charge	Qgd	$V_{GS} = -10 V$		8.2		nC
Body Diode Forward Voltage	VF(S-D)	IF = 5.0 A, VGS = 0 V		0.81		V
Reverse Recovery Time	trr	IF = 5.0 A, VGS = 0 V		61		ns
Reverse Recovery Charge	Qrr	di/dt = 50 A/ μ s		71		nC

TEST CIRCUIT 1 SWITCHING TIME



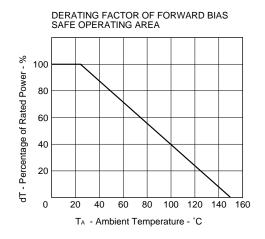
TEST CIRCUIT 2 GATE CHARGE



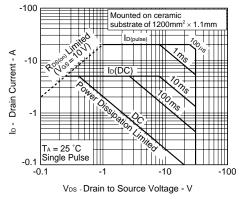
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Phase-out/Discontinued

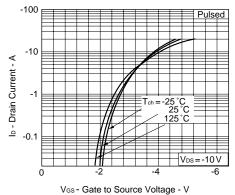
TYPICAL CHARACTERISTICS (TA = 25 °C)

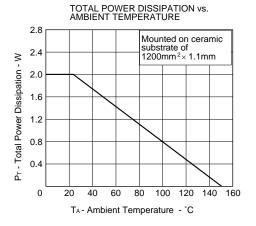




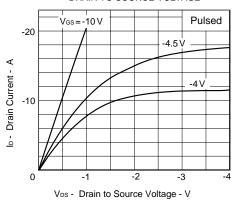


FORWARD TRANSFER CHARACTERISTICS





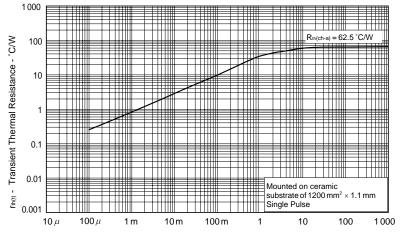




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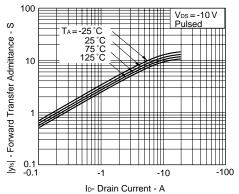
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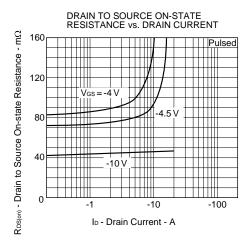
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



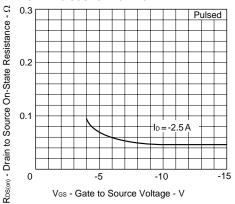




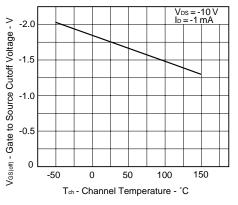




DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



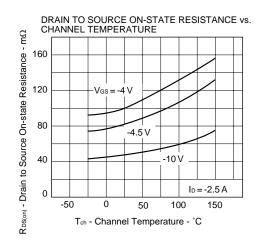
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

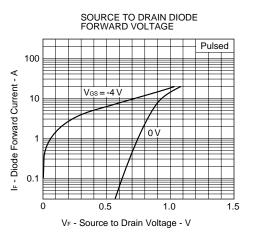


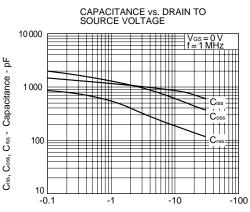
μ PA1710A

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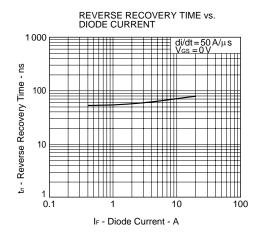
Phase-out/Discontinued



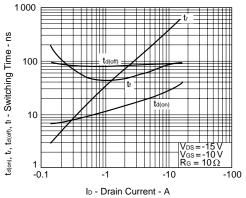


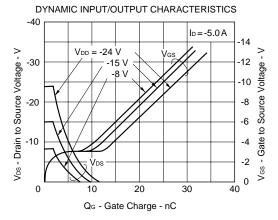






SWITCHING CHARACTERISTICS





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Phase-out/Discontinued

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Phase-out/Discontinued

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Anti-radioactive design is not implemented in this product.

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