DATA SHEET

NEC

MOS FIELD EFFECT TRANSISTOR

Phase-out/Discontinued

μPA1754

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

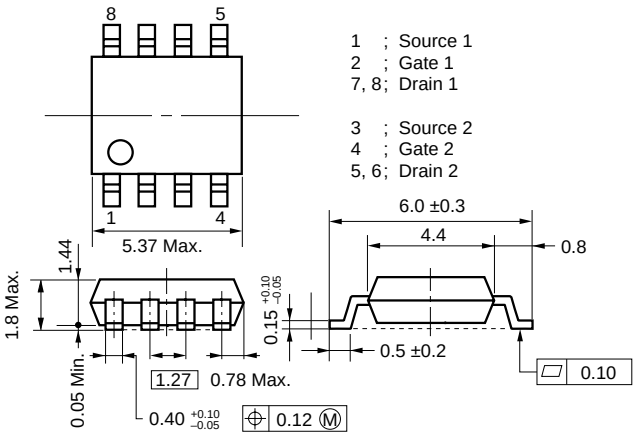
DESCRIPTION

This product is Dual N-channel MOS Field Effect Transistor designed for Li-ion battery applications and power management applications of notebook computers.

FEATURES

- Dual chip type
- Low on-resistance
  $R_{DS(on)1}$ = 32 mΩ MAX. (V_{GS} = 10 V, I_D = 3.5 A)
  $R_{DS(on)2}$ = 53 mΩ MAX. (V_{GS} = 4 V, I_D = 3.5 A)
- Low input capacitance C_{iss} = 780 pF TYP.
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

PACKAGE DRAWING (Unit : mm)

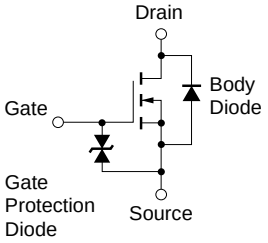


ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA1754G	Power SOP8

EQUIVALENT CIRCUIT

(1/2 Circuit)



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, All terminals are connected.)

Drain to Source Voltage (V_{GS} = 0)	V_{DSS}	30	V
Gate to Source Voltage (V_{DS} = 0)	V_{GSS}	±20	V
Drain Current (DC)	$I_{D(DC)}$	±7.0	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±28	A
Total Power Dissipation (1 unit) Note2	P_T	1.7	W
Total Power Dissipation (2 unit) Note2	P_T	2.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to + 150	°C

Notes 1. PW ≤ 10 μs, Duty cycle ≤ 1 %

2. Mounted on ceramic substrate of 2000 mm^2 x 1.1 mm

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

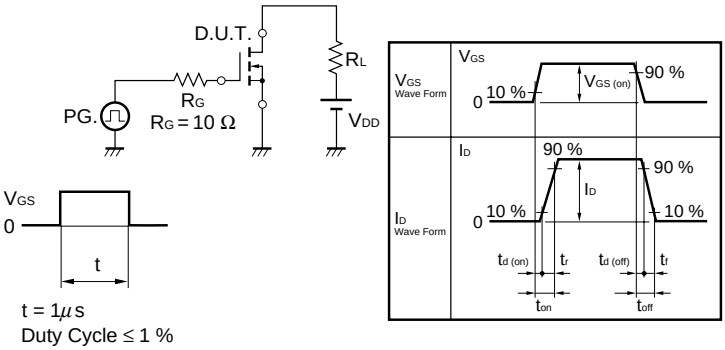
Document No. G12009EJ2V0DS00 (2nd edition)
Date Published May 2001 NS CP(K)
Printed in Japan

The mark ★ shows major revised points.

ELECTRICAL CHARACTERISTICS (T_A = 25 °C, All terminals are connected.)

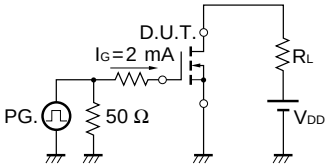
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 3.5 A		20	32	mΩ
	$R_{DS(on)2}$	V_{GS} = 4 V, I_D = 3.5 A		29	53	mΩ
Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.0	1.6	2.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 3.5 A	5.0	9.4		S
Drain Leakage Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0			10	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0			±10	μA
Input Capacitance	C_{iss}	V_{DS} = 10 V		780		pF
Output Capacitance	C_{oss}	V_{GS} = 0		310		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		110		pF
Turn-on Delay Time	$t_{d(on)}$	I_D = 3.5 A		7		ns
Rise Time	t_r	$V_{GS(on)}$ = 10 V		103		ns
Turn-off Delay Time	$t_{d(off)}$	V_{DD} = 15 V		103		ns
Fall Time	t_f	R_G = 10 Ω		86		ns
Total Gate Charge	Q_G	I_D = 7.0 A		17.9		nC
Gate to Source Charge	Q_{GS}	V_{DD} = 24 V		2.3		nC
Gate to Drain Charge	Q_{GD}	V_{GS} = 10 V		4.3		nC
Body Diode forward Voltage	$V_{F(S-D)}$	I_F = 7.0 A, V_{GS} = 0		0.80		V
Reverse Recovery Time	t_{rr}	I_F = 7.0 A, V_{GS} = 0		29		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		44		nC

TEST CIRCUIT 1 SWITCHING TIME



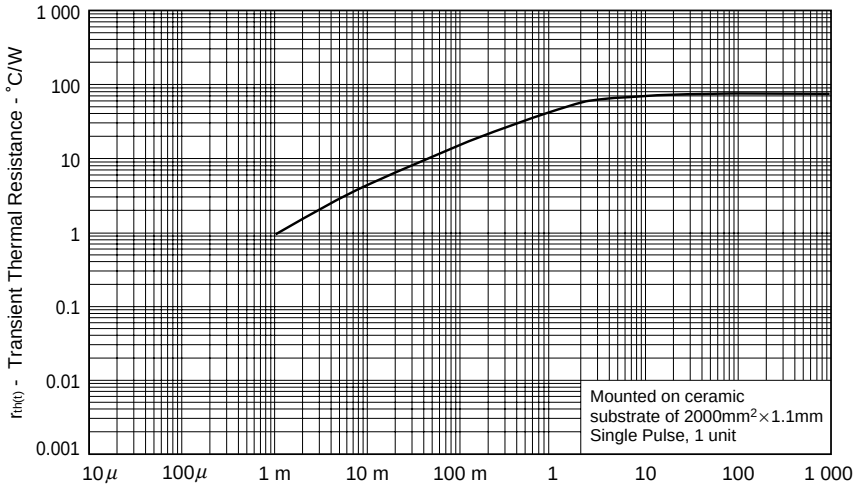
t = 1μs
Duty Cycle ≤ 1 %

TEST CIRCUIT 2 GATE CHARGE

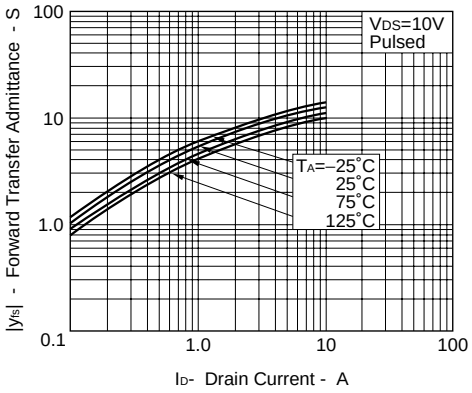


TYPICAL CHARACTERISTICS (T_A = 25 °C)

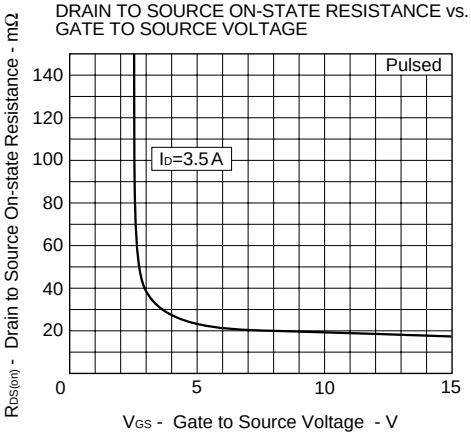
★ TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



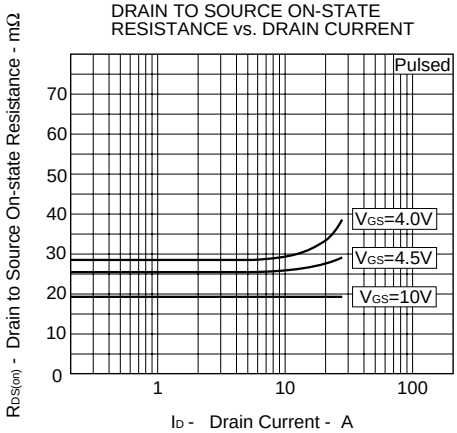
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



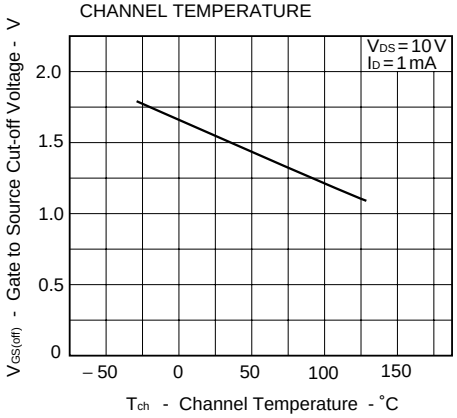
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



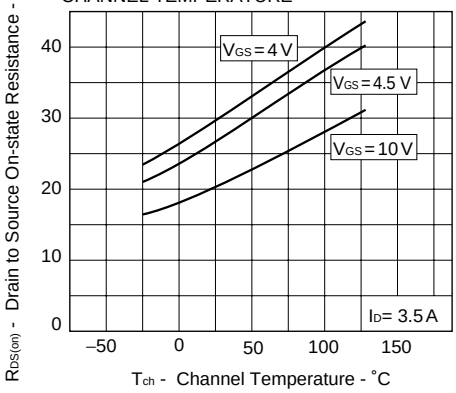
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



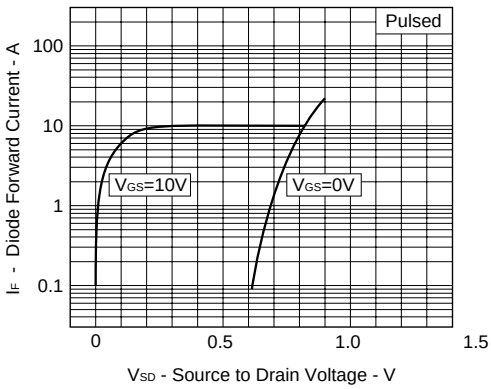
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



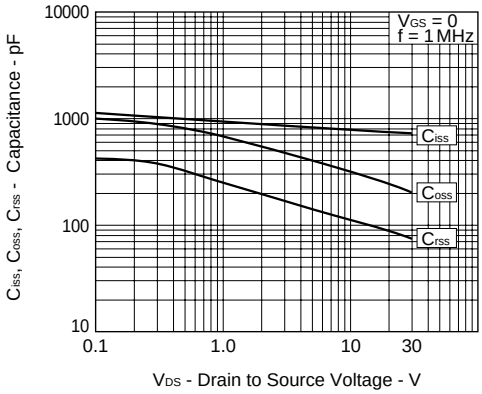
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



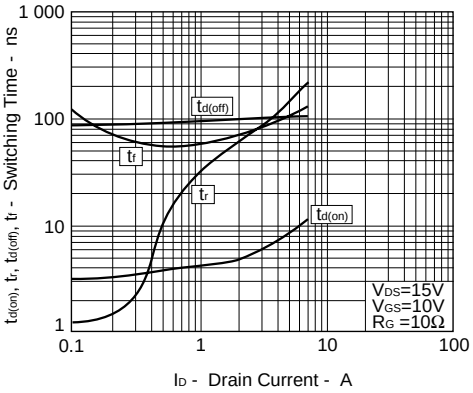
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



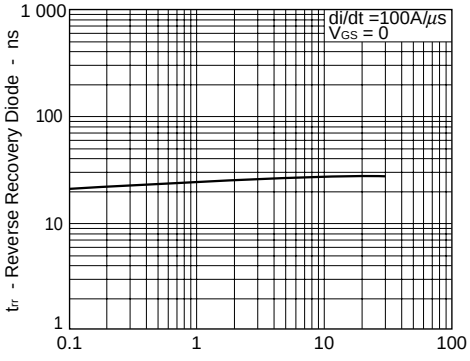
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



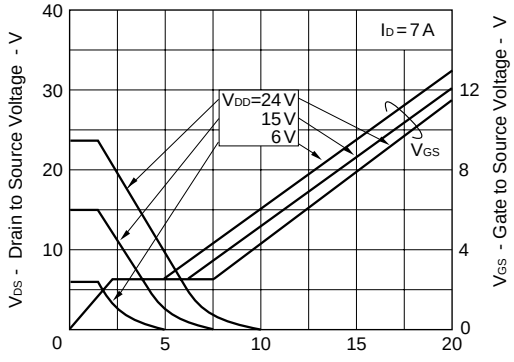
SWITCHING CHARACTERISTICS



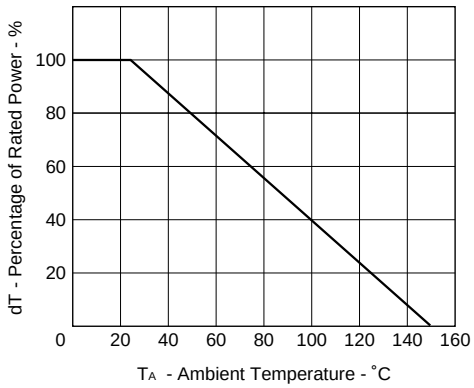
REVERSE RECOVERY TIME vs. DRAIN CURRENT



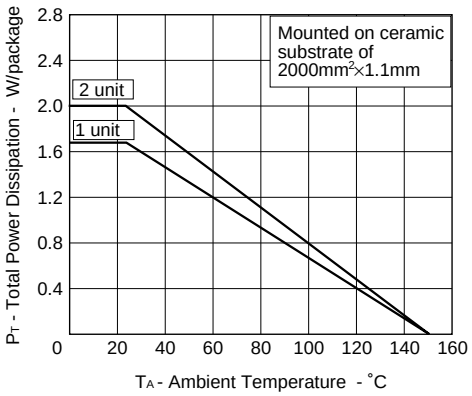
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



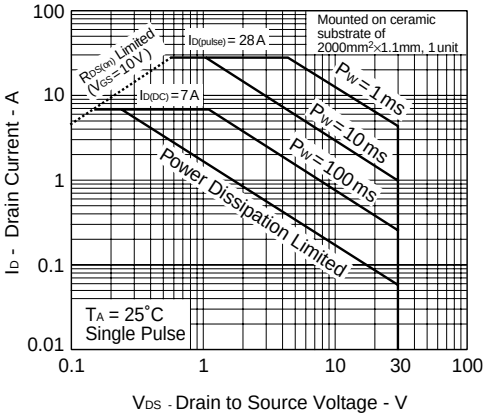
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



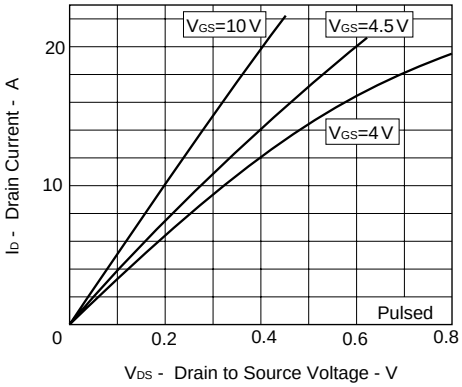
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



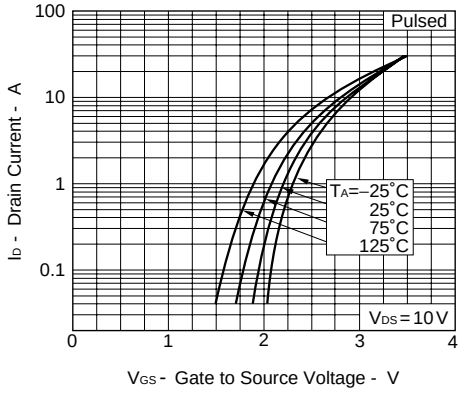
★ FORWARD BIAS SAFE OPERATING AREA



DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



FORWARD TRANSFER CHARACTERISTICS



[MEMO]

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