

MOS FIELD EFFECT POWER TRANSISTORS



 μ PA1751

SWITCHING DUAL N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

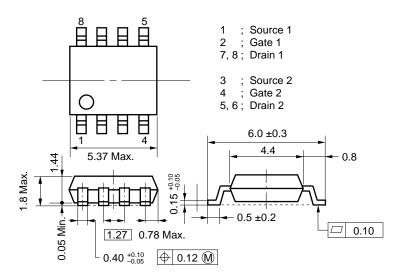
This product is Dual N-Channel MOS Field Effect Transistor designed for power management application of notebook computers, and Li-ion battery application.

FEATURES

- · Dual MOSFET chips in small package
- 4 V Gate Drive Type and Low On-Resistance $R_{DS(on)1}=37~m\Omega$ Max. (Vgs = 10 V, Ib = 2.5 A) $R_{DS(on)2}=64~m\Omega$ Max. (Vgs = 4 V, Ib = 2.5 A)
- Low Ciss Ciss = 510 pF Typ.
- Built-in G-S Protection Diode
- Small and Surface Mount Package (Power SOP8)

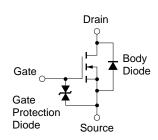
PACKAGE DIMENSIONS

(in: millimeter)



ABSOLUTE MAXIMUM RATINGS (TA = 25 °C, all terminals are connected)

Drain to Source Voltage	VDSS	30	V
Gate to Source Voltage	Vgss	±20	V
Drain Current (DC)	$I_{D(DC)}$	±5.0	Α
Drain Current (pulse)*	ID(pulse)	±20	Α
Total Power Dissipation (1 unit)**	Рт	1.7	W
Total Power Dissipation (2 unit)**	Рт	2.0	W
Channel Temperature	Tch	150	\mathbb{C}
Storage Temperature	Tstg	-55 to +150	С



The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device acutally used, an additional protection circuit is externally required if voltage exceeding the rated voltage may be applied to this device.

The information in this document is subject to change without notice.

^{*} PW \leq 10 μ s, Duty Cycle \leq 1 %

^{**} Mounted on ceramic substrate of 2000 mm² × 1.1 mm

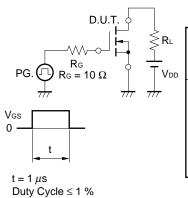


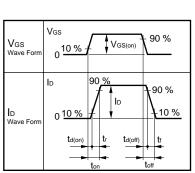


ELECTRICAL CHARACTERISTICS (T_A = 25 °C, all terminal are connected)

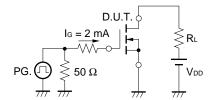
Characteristics	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Drain to Source On-state Resistance	RDS(on)1	Vgs = 10 V, ID = 2.5 A		27	37	mΩ
	RDS(on)2	Vgs = 4 V, ID = 2.5 A		44	64	mΩ
Gate to Source Cutoff Voltage	VGS(off)	V _{DS} = 10 V, I _D = 1 mA	1.0	1.5	2.0	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 2.5 A	3.0	6.0		S
Drain Leakage Current	IDSS	V _{DS} = 30 V, V _{GS} = 0			10	μΑ
Gate to Source Leakage Current	Igss	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0$			±10	μΑ
Input Capacitance	Ciss	V _{DS} = 10 V V _{GS} = 0 f = 1 MHz		510		pF
Output Capacitance	Coss			350		pF
Reverse Transfer Capacitance	Crss			150		pF
Turn-On Delay Time	td(on)	$I_D = 2.5 \text{ A}$ $V_{GS(on)} = 10 \text{ V}$ $V_{DD} = 15 \text{ V}$ $R_G = 10 \Omega$		10		ns
Rise Time	tr			95		ns
Turn-off Delay Time	td(off)			120		ns
Fall Time	tf			100		ns
Total Gate Charge	QG	ID = 5.0 A VDD = 24 V VGS = 10 V		19		nC
Gate to Source Charge	Qgs			1.5		nC
Gate to Drain Charge	Q _{GD}			6.6		nC
Body Diode Forward Voltage	V _{F(S-D)}	IF = 5.0 A, VGS = 0		0.8		V
Reverse Recovery Time	trr	$I_F = 5.0 \text{ A}, \text{ Vgs} = 0$ $di/dt = 100 \text{ A}/\mu\text{s}$		85		ns
Reverse Recovery Charge	Qrr			90		nC

Test Circuit 1 Switching Time

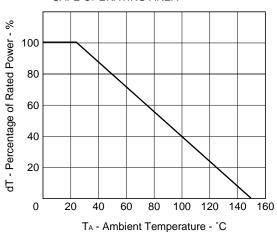




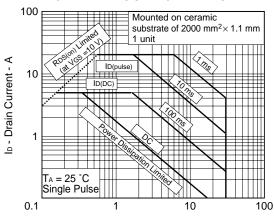
Test Circuit 2 Gate Charge



DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

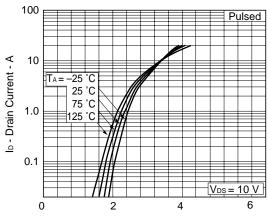


FORWARD BIAS SAFE OPERATING AREA



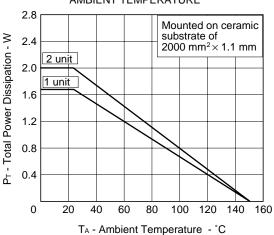
V_{DS} - Drain to Source Voltage - V

FORWARD TRANSFER CHARACTERISTICS

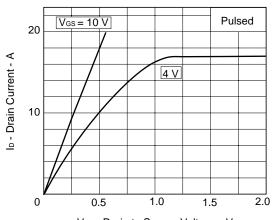


V_{GS} - Gate to Source Voltage - V

TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE

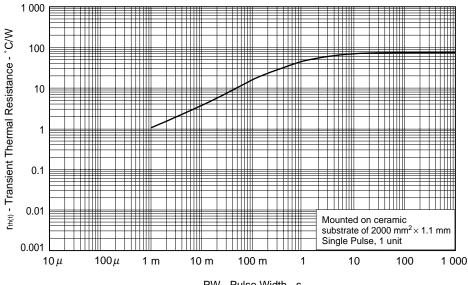


DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



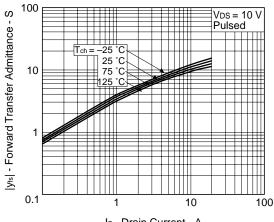
V_{DS} - Drain to Source Voltage - V

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

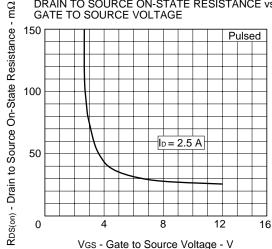


PW - Pulse Width - s

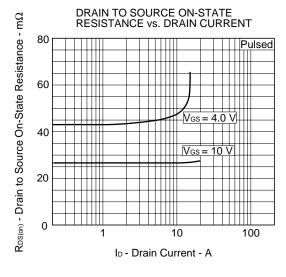
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



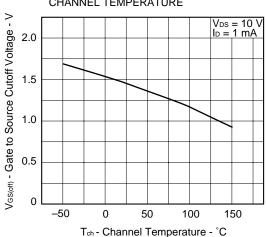
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



ID - Drain Current - A



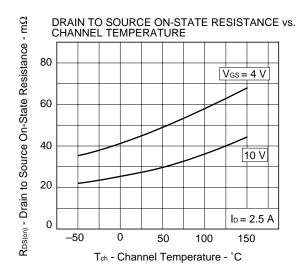
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

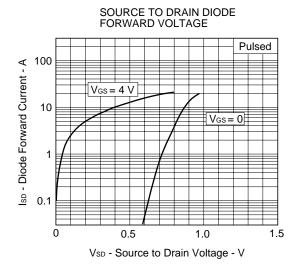


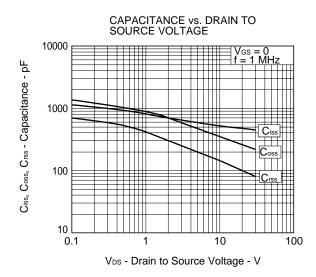
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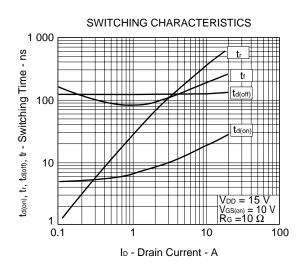


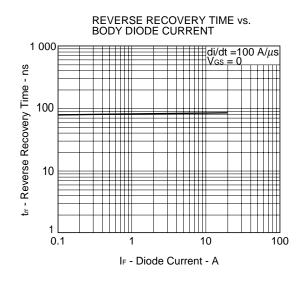


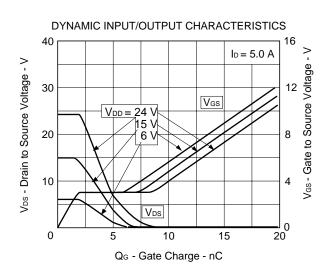
















REFERENCE

Document Name	Document No.	
NEC semiconductor device reliability/quality control system	TEI-1202	
Quality grade on NEC semiconductor devices	IEI-1209	
Semiconductor device mounting technology manual	C10535E	
Semiconductor device package manual	C10943X	
Guide to quality assurance for semiconductor devices	MEI-1202	
Semiconductor selection guide	X10679E	
Power MOS FET features and application switching power supply	TEA-1034	
Application circuits using Power MOS FET	TEA-1035	
Safe operating area of Power MOS FET	TEA-1037	

[MEMO]



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Anti-radioactive design is not implemented in this product.

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