DATA SHEET

NEC

MOS FIELD EFFECT TRANSISTOR

Phase-out/Discontinued

μPA1757

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

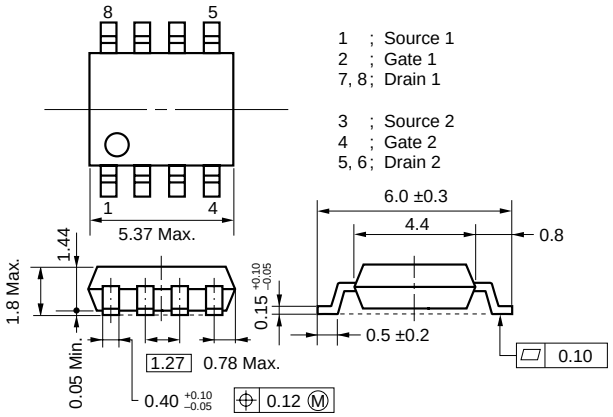
Description

This product is Dual N-Channel MOS Field Effect Transistor designed for power management application of notebook computers, and Li-ion battery application.

Features

- Dual MOS FET chips in small package
- 2.5 V gate drive type and low on-resistance
  $R_{DS(on)1}$ = 23 mΩ (MAX.) (V_{GS} = 4.5 V, I_D = 3.5 A)
  $R_{DS(on)2}$ = 32 mΩ (MAX.) (V_{GS} = 2.5 V, I_D = 3.5 A)
- Low C_{iss} C_{iss} = 750 pF Typ.
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

Package Drawing (Unit : mm)

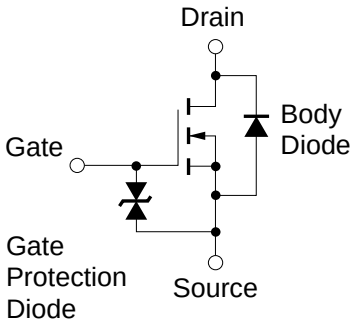


Ordering information

Part Number	Package
μPA1757G	Power SOP8

Absolute Maximum Ratings (T_A = 25 °C)

Drain to source voltage	V_{DSS}	20	V
Gate to source voltage	V_{GSS}	±12.0	V
Drain current (DC)	$I_{D(DC)}$	±7.0	A
Drain current (pulse)[Note1]	$I_{D(pulse)}$	±28	A
Total power dissipation (1 unit)[Note2]	P_T	1.7	W
Total power dissipation (2 unit)[Note2]	P_T	2.0	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	–55 to +150	°C



Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1 %

2. T_A = 25 °C, Mounted on ceramic substrate of 2000 mm^2 x 1.1 mm

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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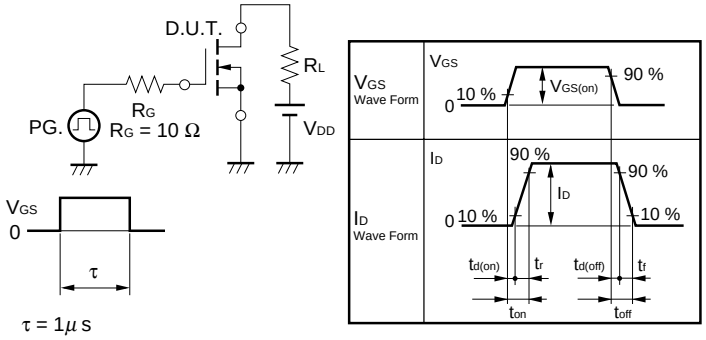
The mark ★ shows major revised points.

Electrical Characteristics (T_A = 25 °C)

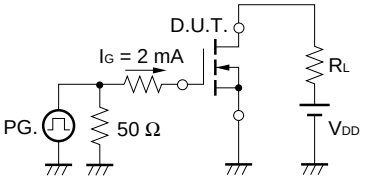
Characteristics	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Drain to source on-state resistance	$R_{DS(on)1}$	V_{GS} = 4.5 V, I_D = 3.5 A		16.2	23	mΩ
	$R_{DS(on)2}$	V_{GS} = 2.5 V, I_D = 3.5 A		22	32	mΩ
Gate to source cutoff voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1.0 mA	0.5	0.8	1.5	V
Forward transfer admittance	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 3.5 A	5.0	13		S
Drain leakage current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V			10	μA
Gate to source leakage current	I_{GSS}	V_{GS} = ±12.0 V, V_{DS} = 0 V			±10	μA
Input capacitance	C_{iss}	V_{DS} = 10 V V_{GS} = 0 V f = 1 MHz		750		pF
Output capacitance	C_{oss}			420		pF
Reverse transfer capacitance	C_{rss}			140		pF
Turn-on delay time	$t_{d(on)}$	I_D = 3.5 A $V_{GS(on)}$ = 4.0 V V_{DD} = 10 V R_G = 10 Ω		57		ns
Rise time	t_r			206		ns
Turn-off delay time	$t_{d(off)}$			593		ns
Fall time	t_f			815		ns
Total gate charge	Q_G	I_D = 7.0 A V_{DD} = 16 V V_{GS} = 4.0 V		13.0		nC
Gate to source charge	Q_{GS}			2.6		nC
Gate to drain charge	Q_{GD}			5.3		nC
Body diode forward voltage	$V_{F(S-D)}$	I_F = 7.0 A, V_{GS} = 0 V		0.75		V

Test circuit 1 Switching time



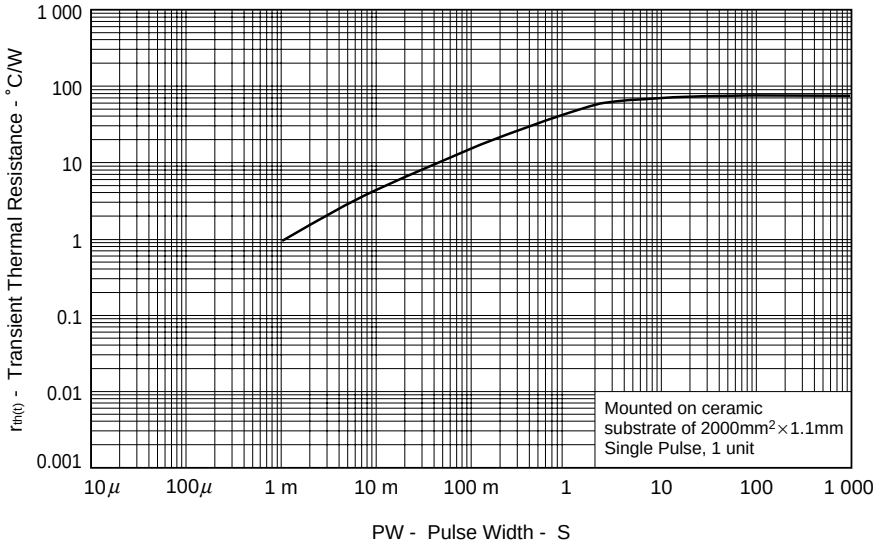
τ = 1μs
Duty Cycle ≤ 1 %

Test circuit 2 Gate charge

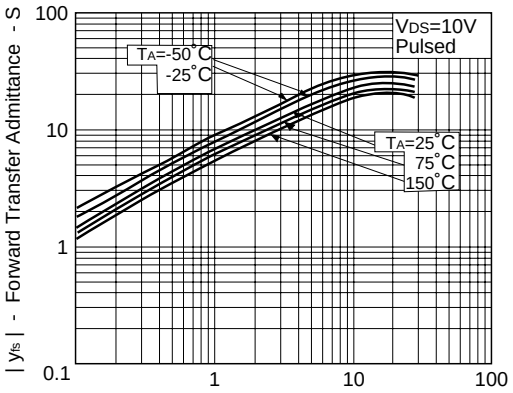


Typical Characteristics (T_A = 25 °C)

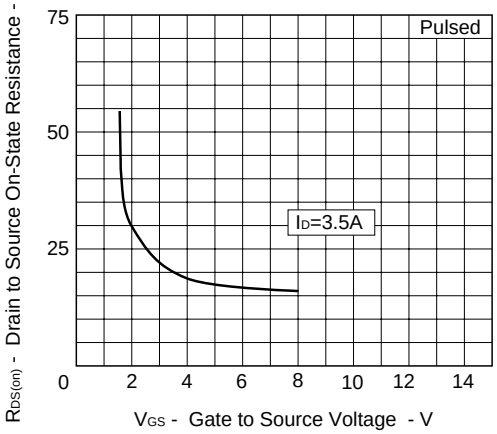
★ TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



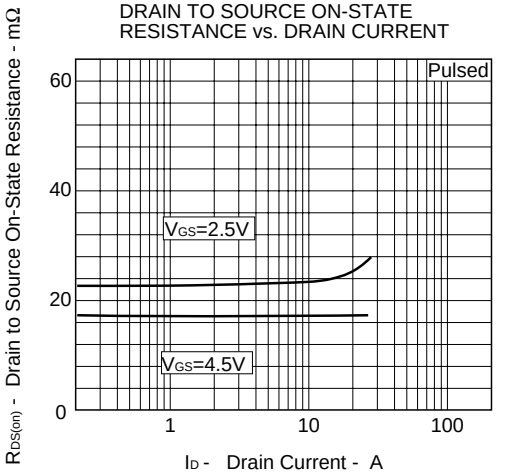
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



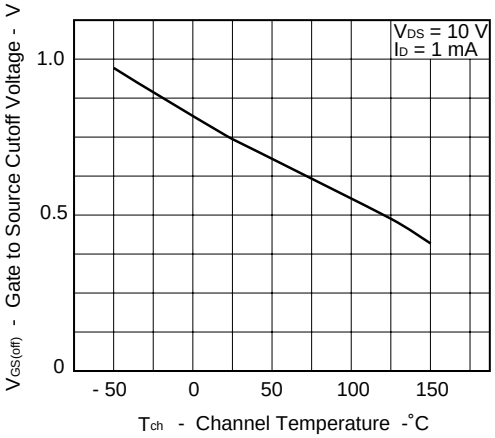
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



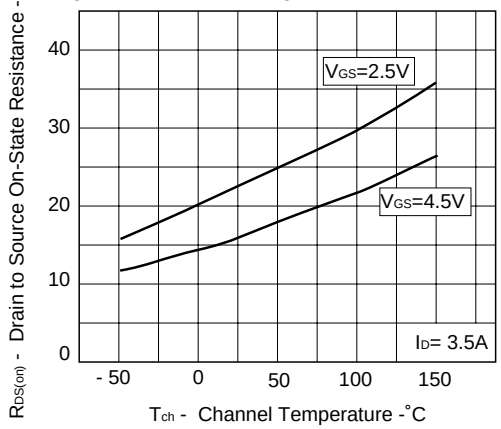
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



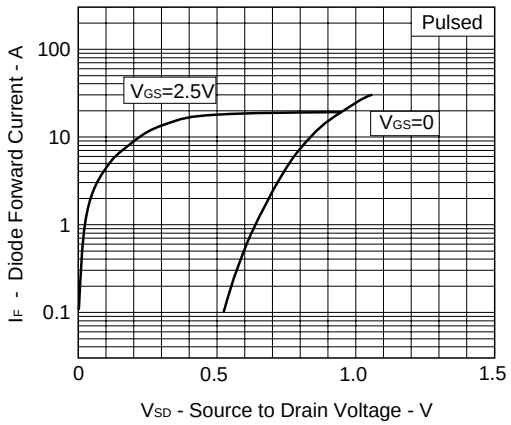
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



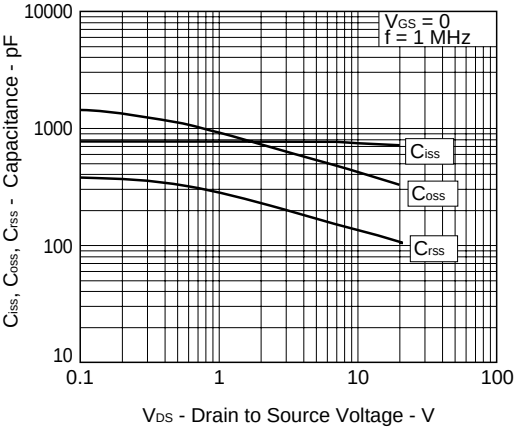
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



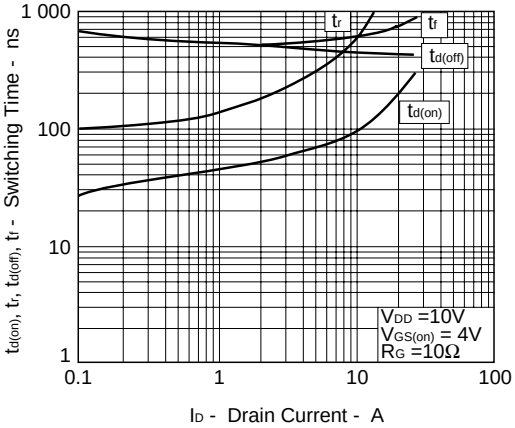
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



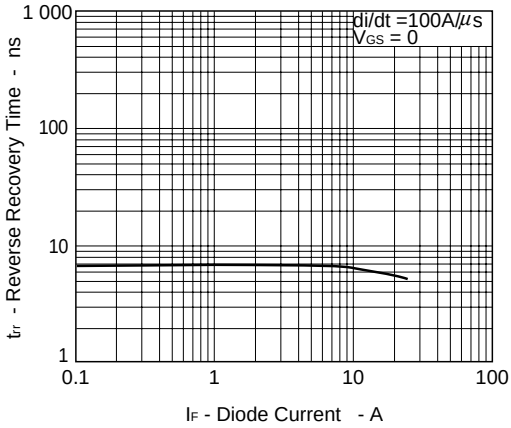
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



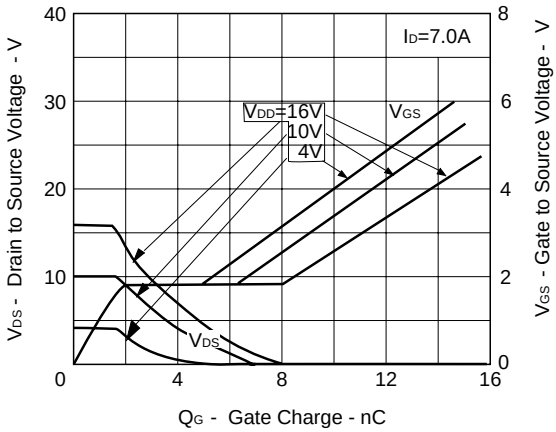
SWITCHING CHARACTERISTICS



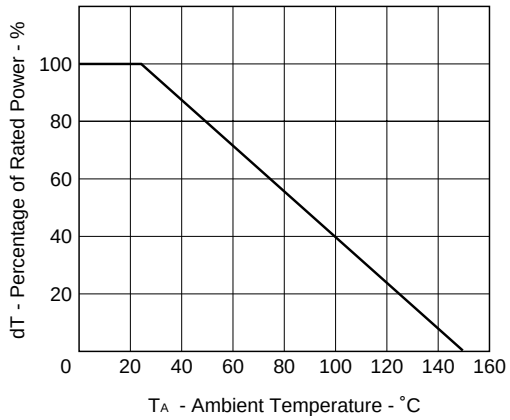
REVERSE RECOVERY TIME vs. DRAIN CURRENT



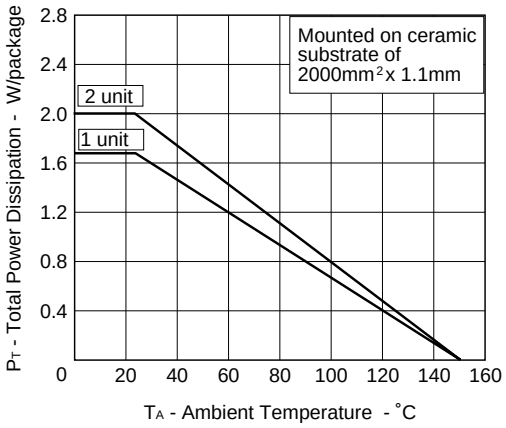
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



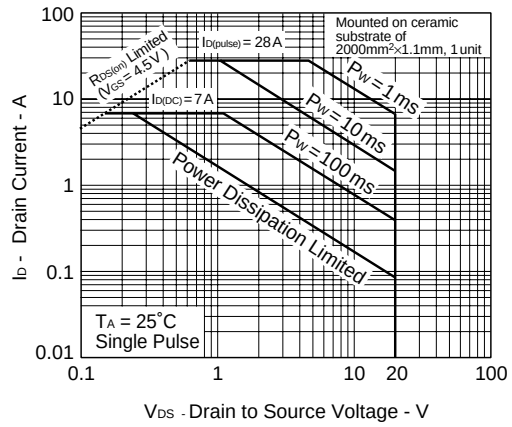
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



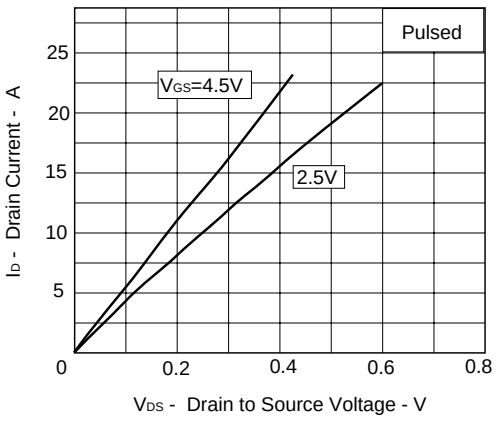
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



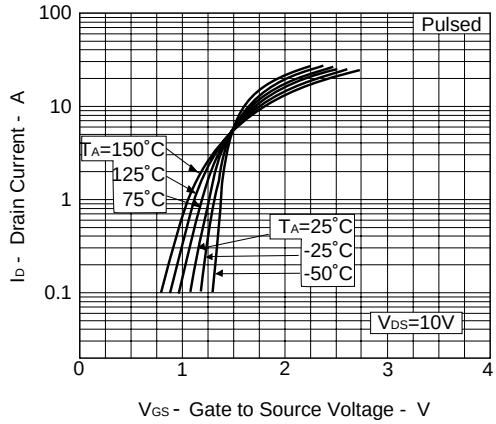
★ FORWARD BIAS SAFE OPERATING AREA



DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



FORWARD TRANSFER CHARACTERISTICS



[MEMO]

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