

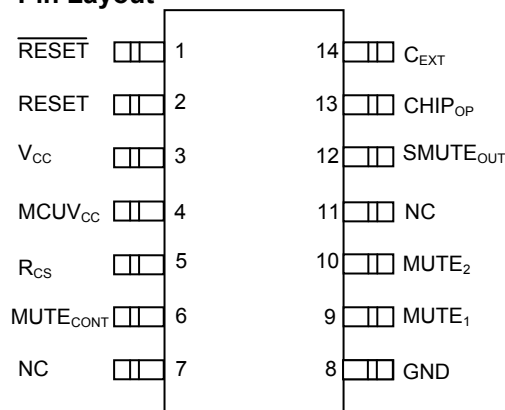
Features

- Precision supply voltage monitoring
- Reset Timeout Delay
- 36dB mute attenuation
- 2.7V to 5.5V single-supply operation
- ESD protected outputs
- Low supply current
- Soft Mute out for driving additional channels
- SOIC 14

Applications

- Set-top boxes
- Cell phones
- PDA's
- Portable DVD players
- Portable MP3 players
- Notebook Audio
- Critical μ P Power Monitoring

Pin Layout



General Description

The PA4101 is a low power monolithic CMOS mixed signal device. Its function is to control power supply transition noise in audio circuits and systems. It requires very few external components for its operation and works from low to medium power supply voltages of 2.7V to 5.5V. As the power supply ramps ON or OFF, the PA4101 ensures that audio inputs to succeeding amplifiers are switched to a convenient low impedance voltage rail. This causes the amplifiers to remain silent as the power supply changes state (from ON to OFF and vice versa).

Also included in the device is a digital control pin which can be used by a control device such as a micro controller or a micro-processor or any other digital controller to enable the audio mute function. This supervisory circuit provides maximum flexibility for monitoring power supplies and battery controlled functions in systems without backup batteries.

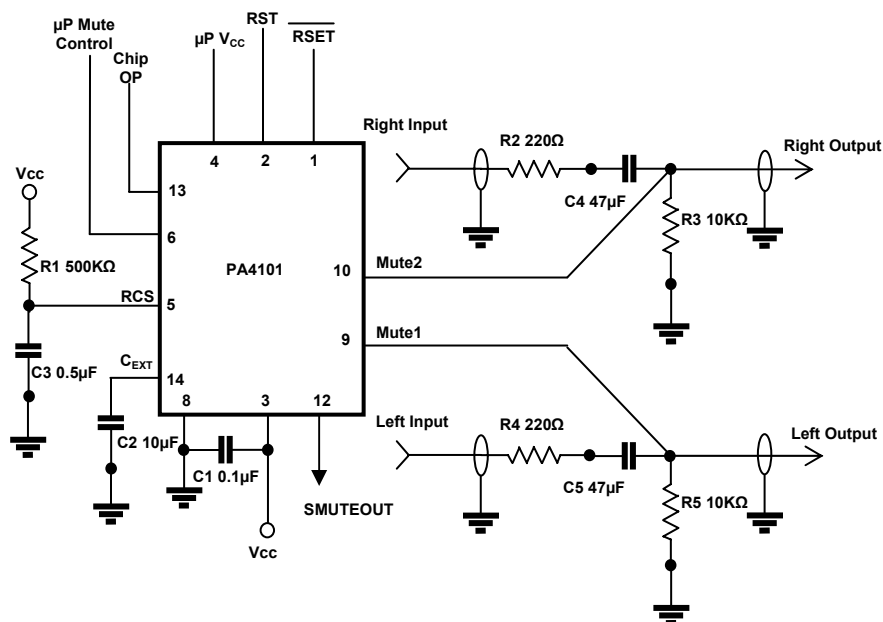
A Reset is asserted during power up, power down and brownout conditions. RESET is guaranteed down to V_{CC} of 1.0V.

Low line output. The early warning indicator goes low when the supply voltage drops to a value 2% higher than the reset threshold voltage

The PA4101 consumes less than 50 μ A of supply current while providing more than 36dB of mute attenuation at the audio lines. ESD (Human Body Model) protection circuitry on the outputs protects the PA4101 and devices further up the signal chain.

The PA4101 is available as a 14L SOIC package and is specified for operation over the -40°C to +85°C temperature range.

Functional Diagram Typical Application



Absolute Maximum Ratings

Sustained operation at or above the following ratings is not recommended. Catastrophic and irreversible damage will occur to the device at or above these ratings.

Symbol	Description	Rating
V_X	Voltage at any pin	-0.3 to 7.0+0.3 V
I_X	Current at any pin	500mA
T_A	Ambient Temperature	150 ° C
T_S	Storage Temperature	200 ° C
T_{SOL}	Soldering Temperature	270 ° C

Recommended Operating Conditions:

Unless otherwise specified, $V_{DD}=2.7\pm10\%$, T_A = Ambient Temperature = 25 deg C.

DC Operating Conditions

Symbol	Parameter	Condition	Limit			Unit
			Min	Typ	Max	
V_{DD}	Positive Power Supply	Operating	2.7		5.5	V
I_{DD}	VDD Current	Operating			1	mA
T_A	Ambient Temperature	Operating	-30		85	°C
V_{OH}	Logic High O/P Voltage	$I_{OH}=100\mu A$	$V_{DD}-0.1$			V
V_{OL}	Logic Low O/P Voltage	$I_{OL}=-100\mu A$			0.2	V
V_{IH}	Logic High I/P Voltage	$I_{IH}=1\mu A$	$V_{DD}-0.3$			V
V_{IL}	Logic Low I/P Voltage	$I_{IL}=1\mu A$			0.3	V
R_{ON}	FET ON Resistance	$V_{DD}=2.7V$, $V_{DFET}=0.4V$			1.5	Ω

Supervisor Operating Conditions

Symbol	Parameter	Condition	Limit			Unit
			Min	Typ	Max	
V_{RST}	Reset Voltage	Operating		2.5		V
V_{RSTH}	Reset Threshold	VDD falling -40 to 85 degC	-2.5		2.5	%
V_{HYS}	Reset Threshold hysteresis	$V_{DD}=2.7V$	17		29	mV
V_{HYS}	Reset Threshold hysteresis	$V_{DD}=5.5V$	36		60	mV
T_{RD}	VDD – Reset Delay	VDD falling at 1mv/ μ s			20	μ s
T_{RP}	Reset Time Out Period		44		75	ms

Mute Operating Conditions

Symbol	Parameter	Condition	Limit			Unit
			Min	Typ	Max	
M_{OFFD}	Mute release delay	Mute Control=VIL Set by ext. capacitor CM	10		300	mS
M_{STD}	Soft mute fall/rise time	Mute Control transitions to VIH. Set by ext. capacitor CEXT	1		300	mS
M_{PDEL}	Mute ON Delay	Power drops by 10%			5	μ S
NFETV	NFET open drain volt				12	V

Pin Out

Pin	Name	Function
1	RESET	Inverted Reset output from the voltage supervisor
2	RESET	Reset output from the voltage supervisory circuit.
3	VCC	Positive power supply. 2.7V to 5.5V $\pm 10\%$
4	MCUVCC	Microprocessor power supply
5	RCS	Power On mute delay resistor-capacitor connection.
6	MUTECONT	Mute control signal from microprocessor.
8	GND	Ground.
9	MUTE1	Open Drain output of NFET 1
10	MUTE2	Open Drain output of NFET 2
12	SMUTEOUT	Soft Mute OUT for multiple channels.
13	CHIPOP	Supply voltage selector. Connect to GND for 2.7V, VCC for 5.5V.
14	CEXT	Soft mute delay capacitor.

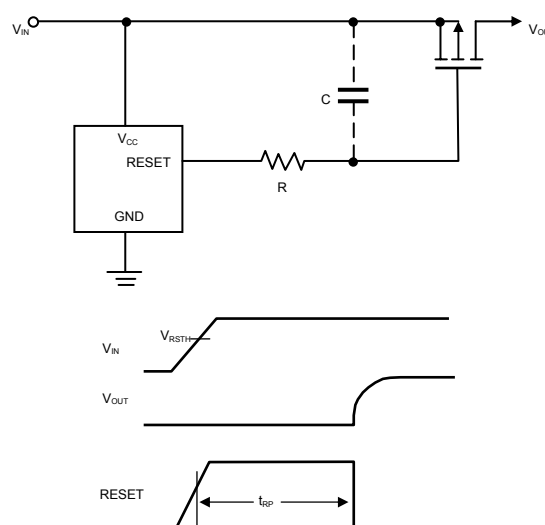
Operation Of Supervisor Circuit.

The reset input of a μ P initializes the device into a known state. The PA4101 supervisor circuitry asserts a forced reset output to prevent code execution errors during Power-up, power-down and brownout conditions.

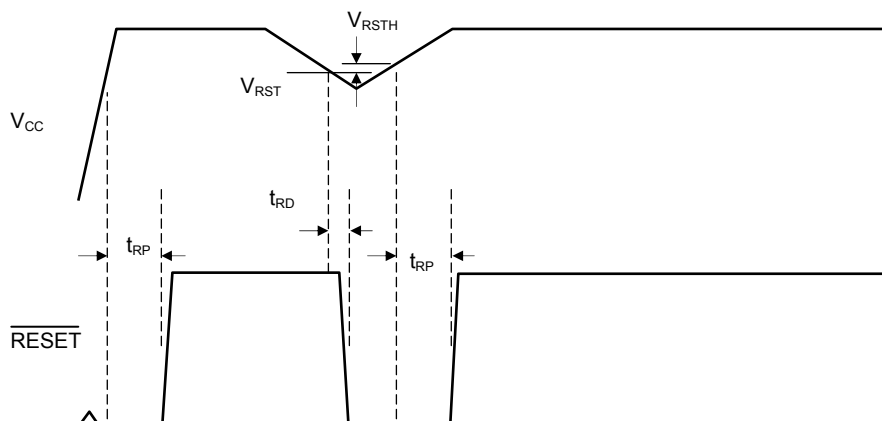
RESET is valid for $V_{CC} > 1$ Volt. Once V_{CC} exceeds the threshold, an internal timer maintains the output for the reset period timeout. After this interval, reset goes high.

Any time V_{CC} drops below the reset threshold, the reset activates. When V_{CC} again rises above the threshold, the internal timer starts. Reset holds until V_{CC} exceeds the reset threshold for longer than the reset timeout period. After this time the reset release

Supervisor Application



Timing Diagram Supervisor



THEORY OF OPERATION Audio Muting

STARTUP

During Startup, the Power supply ramps from 0V to V_{CC} . This time is usually in excess of 20ms. As soon as this change in voltage is sensed, PUNK latches the Mute Controller outputs to HIGH, thus "muting" the lines. This is the Startup Operation (figure 1). The duration for which the controller outputs are latched HIGH can be controlled by an external RC circuit. When the voltage at this RC pin reaches a certain threshold, the mute controller releases the lines (Gate voltage is LOW) and Normal Operation starts.

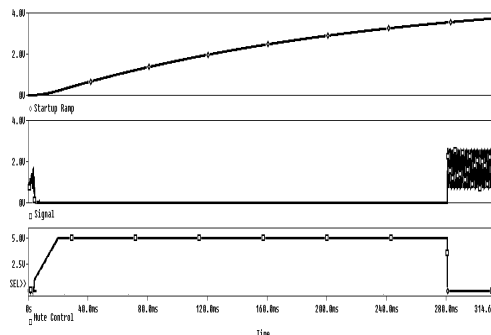


Figure 1: Startup Pop-Noise Reduction

SHUTDOWN

During Shutdown, the reverse process happens. As the power supply reaches the threshold on its way down, the mute controller again latches the outputs to HIGH, thus "muting" the lines (figure 2). This muting prevents unwanted signal spikes from getting to the power amplifiers. However, for optimal performance, it is suggested to mute the lines using the MUTECONT signal before power down. This process will ensure that the pop noise involved during shutdown is diminished.

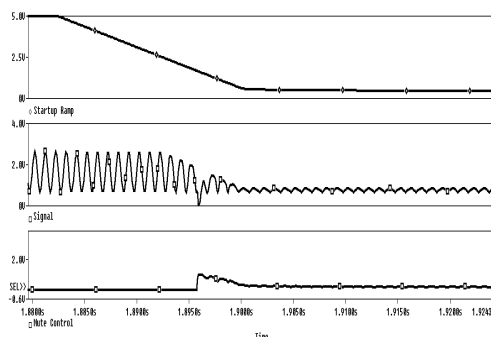


Figure 2: Shutdown Pop-Noise Reduction

SOFTMUTE

During normal operation, PUNK is in OFF state. But if there arises a situation when the audio lines need to be muted, the designer can do this by asserting the MUTECONT signal to HIGH. This will initiate a SOFTMUTE sequence (figure 3). When the MUTECONT signal is asserted, the mute controller gradually ramps the control voltages in a "SOFT" fashion so as to provide a soft mute operation. The mute delay is fully controllable by the designer by using an external capacitor at CEXT. Typical values of CEXT are between 0.1 μ F and 0.5 μ F. The reverse happens when the MUTECONT signal is released. This operation is explained in detail in the Application Circuit section.

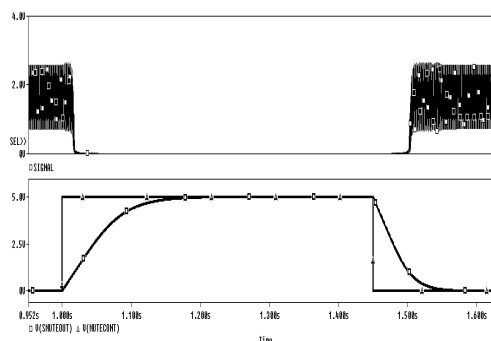
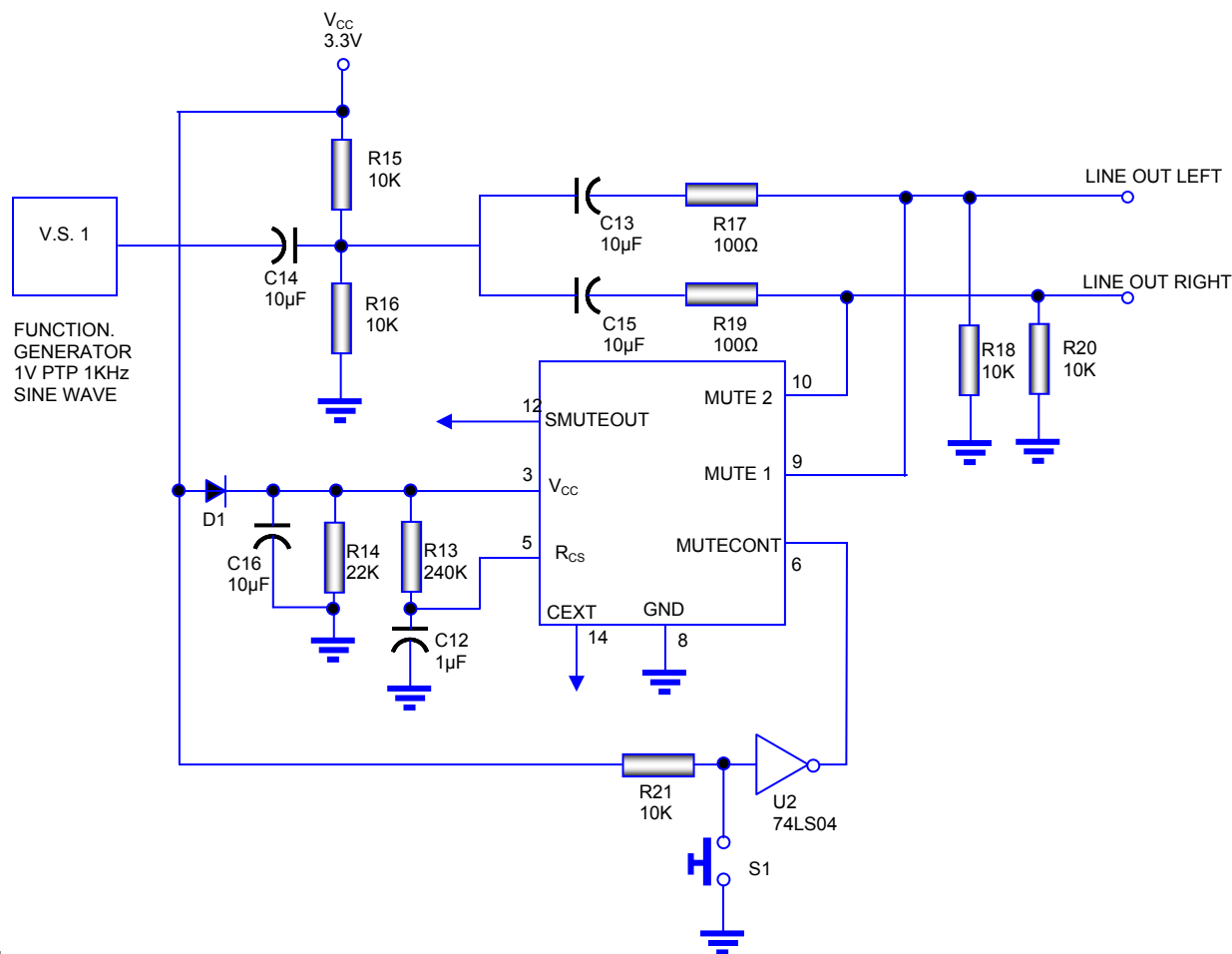


Figure 3: SOFT mute operation

Typical Application Audio Muting.



Notes:

1. A Set Top Box audio output is "simulated" using C14, R15, R16 and VS 1.
2. VS 1 is a signal generator having an output impedance of 50Ohm.
3. U2 is the IC 74LS04.
4. U2 runs off of PUNK Vcc (Output of D1, C16 and R14).
5. Input to U2 is the Set Top Box Vcc
6. Switch S1 serves as a manual "Audio Mute" to enable the muting function.
7. Scope probes were attached to Set Top Box Power Supply and Line Out.
8. Waveform shown in Figure 4 to Figure 9

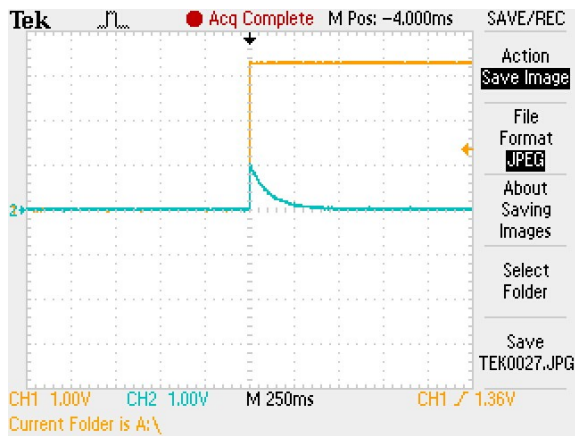


Figure 4: Startup Pop-Noise without PUNK

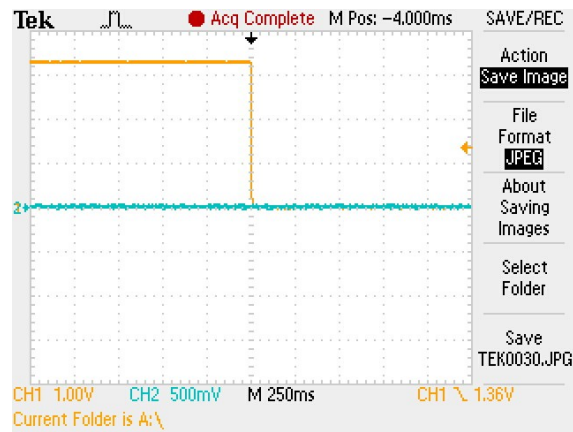


Figure 7: Shutdown Pop-Noise with PUNK



Figure 5: Shutdown Pop-Noise without PUNK

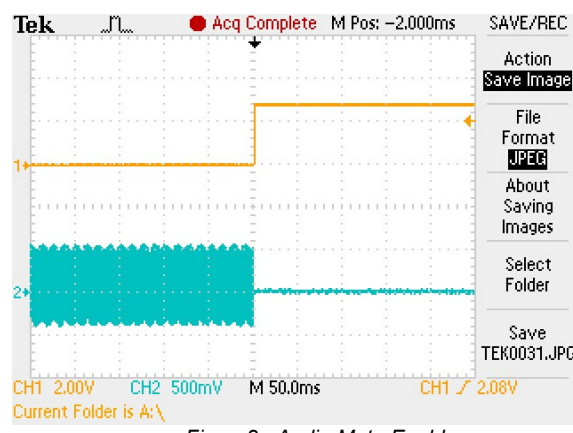


Figure 8: Audio Mute Enable



Figure 6: Startup Pop-Noise with PUNK

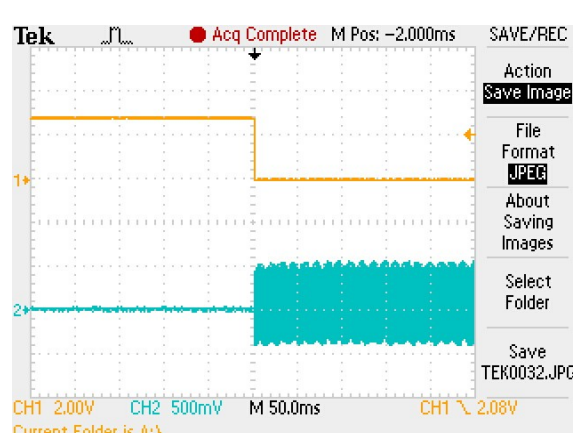
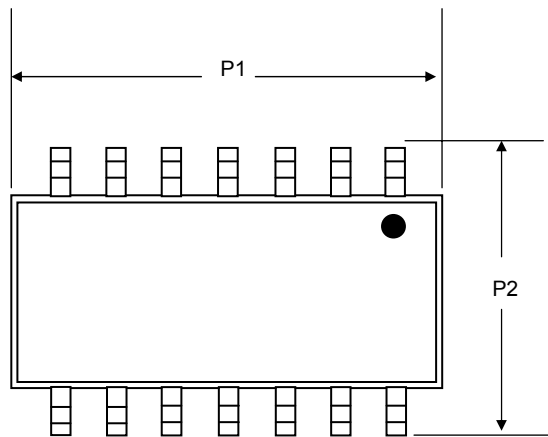
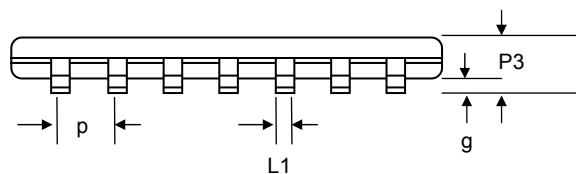


Figure 9: Audio Mute Disable

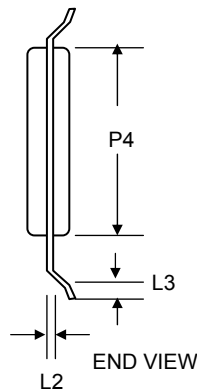
Package Layout and Dimensions



TOP VIEW

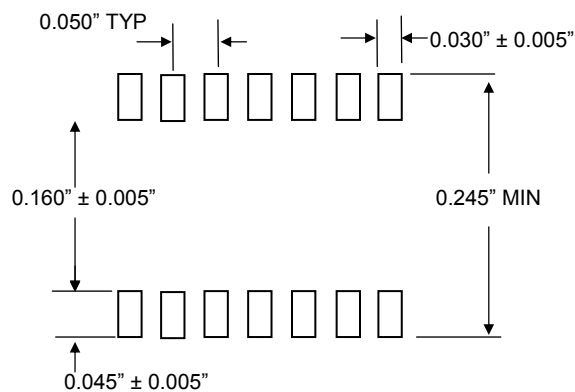


SIDE VIEW



END VIEW

Dim	Inches		
	MIN	TYP	MIN
P1	0.337	0.341	0.346
P2	0.230	0.238	0.244
P3	0.060	0.065	0.070
P4	0.150	0.155	0.157
L1	0.014	0.016	0.019
L2	0.007	0.009	0.010
L3	0.023	0.026	0.029
p	0.050	0.050	0.050
g	0.004	0.006	0.008



Recommended Pattern Layout

Life Support Policy

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