# CT2561
# Bus Controller, Remote Terminal and BUS Monitor
## FOR MIL-STD-1553B

## Features

- Second Source Compatible to the BUS-65610
- 16MHz CT2565 Replacement
- RTU implements all dual redundant mode codes
- Selective mode code illegalization available
- 16 bit microprocessor compatibility
- BC checks status word for correct address and set flags
- RTU illegal mode codes externally selectable
- 16 bit µProcessor compatibility
- DMA handshaking for subsystem message transfers
- Continuous On-Line and Initiated Built-In-Test
- MIL-PRF-38534 compliant circuits available
- Packaging – Hermetic Metal
  - 78 Pin, 2.1" x 1.87" x .25" Plug-In type package
  - 82 Lead, 2.2" x 1.61" x .18" Flat package

AEROFLEX CIRCUIT TECHNOLOGY
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## General Description

The CT2561 is a 16 MHz single chip dual redundant MIL-STD-1553 Bus Controller (BC), Remote Terminal Unit (RTU) and Bus Monitor (MT). Packaged in a hybrid plug-in or flatpack, the CT2561 performs all the functions required to interface a MIL-STD-1553 dual redundant serial data bus such as ACT4487 and a subsystem parallel three-state data bus.

Using a single Aeroflex custom monolithic ASIC design, the CT2561 features pin-for-pin and functional CT2565 compatibility, user initiated self-test, and low power consumption.

Compatible with most microprocessors the CT2561 provides a 16bit three-state parallel data bus and uses direct memory access (DMA type) handshaking for subsystem transfers. All message transfer timing, DMA and control lines are provided internally, thereby reducing the subsystem overhead associated with message transfers.

The CT2561 implements all dual redundant MIL-STD-1553 mode codes. In addition, any mode code may (Optionally) be legalized through the use of an external PROM. Complete error detection is provided by the CT2561 for BC and RTU operation. Error detection includes: response time-out, inter-message gaps, sync, parity, Manchester, word count and bit count.

The CT2561 is fully compliant with MIL-STD-1553, is available screened in accordance with the requirements of MIL-STD-883 and operates over the full military temperature range of -55°C to +125°C.

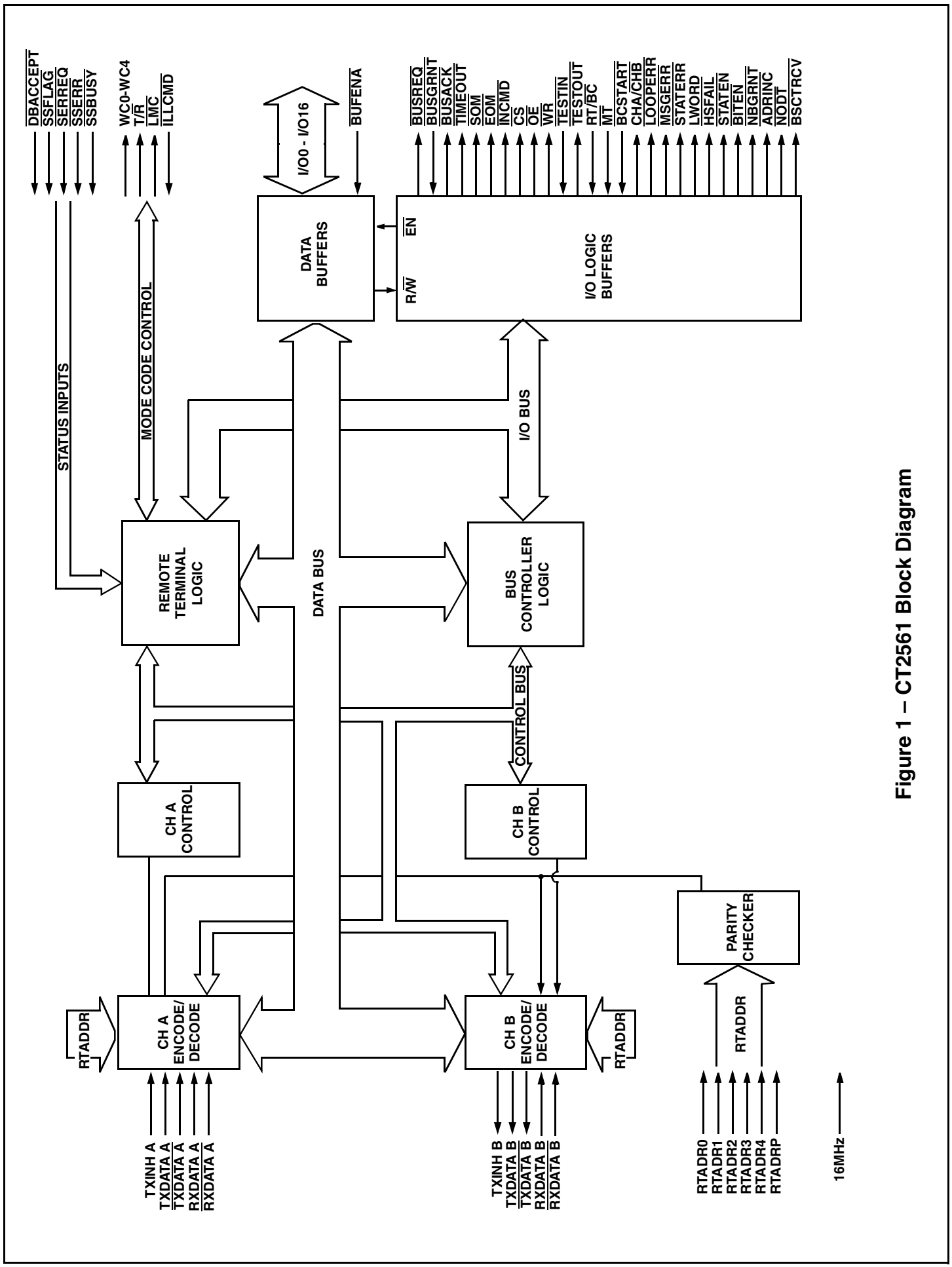


**Figure 1 – CT2561 Block Diagram**

## Table 1A – Pin Function Table (78 Pin Plug-In)

| Pin # | Symbol | I/O | Description |
|---|---|---|---|
| 1 | RT/$\overline{BC}$ | I | Mode Select input - logic "1" for RT mode, logic “0” for BC mode. |
| 2 | $\overline{MT}$ | I | Monitor mode enable. When unit is operating as a BC, a logic “0” will select monitor mode. |
| 3 | $\overline{STATEN}$ | O | Output signal in RT mode that indicates status word is being transferred on the internal bus. |
| 4 | $\overline{TIMEOUT}$ | O | Indicates No Response Timeout has occurred during BC and RTU (RT to RT transfer). |
| 5 | $\overline{HSFAIL}$ | O | Output in RT mode indicating the DMA transfer did not occur in time to allow proper operation on the 1553 bus. |
| 6 | $\overline{DBACCEPT}$ | I | Input signal used to set DBACCEPT bit in status register for response to a valid mode command on the 1553 bus. |
| 7 | $\overline{SSFLAG}$ | I | Input which controls the SSFLAG bit in the status register. |
| 8 | $\overline{SVCREQ}$ | I | Input which controls the service request bit in the status word. |
| 9 | $\overline{INCMD}$ | O | Output signal indicating the RT is currently in a message transfer sequence. |
| 10 | $\overline{SSER}$ | I | Input which controls the subsystem error bit in the status register. |
| 11 | $\overline{TESTOUT}$ | - | Factory test point. Do not connect. |
| 12 | WC1 | O | WC bit 1 - latched output of command word. |
| 13 | WC3 | O | WC bit 3 - latched output of command word. |
| 14 | TXINH B | O | Transmitter inhibit output for channel B. |
| 15 | T/$\overline{R}$ | O | Output indicating T/$\overline{R}$ bit of current command word in RT mode. |
| 16 | $\overline{CHA}$/CHB | O | Output indicating current selected channel (0 = Channel A). |
| 17 | $\overline{CS}$ | O | Chip Select output for subsystem memory control. |
| 18 | $\overline{OE}$ | O | Output Enable output for subsystem memory control. |
| 19 | $\overline{BUSREQ}$ | O | Output signal used to initiate transfer to/from subsystem. |
| 20 | +5V | I | +5 Volt DC input. |
| 21 | DB0(LSB) | I/O | Least significant bit - 16 bit parallel data bus. |
| 22 | DB2 | I/O | Bit 2 of data bus. |
| 23 | DB4 | I/O | Bit 4 of data bus. |
| 24 | DB6 | I/O | Bit 6 of data bus. |
| 25 | DB8 | I/O | Bit 8 of data bus. |
| 26 | DB10 | I/O | Bit 10 of data bus. |
| 27 | DB12 | I/O | Bit 12 of data bus. |
| 28 | DB14 | I/O | Bit 14 of data bus. |

## Table 1A – Pin Function Table (78 Pin Plug-In) (continued)

| Pin # | Symbol | I/O | Description |
|---|---|---|---|
| 29 | LWORD | - | Last word output during BC mode indicates last data word of the current message transfer has been transferred on the parallel bus. |
| 30 | $\overline{\text{MSGERR}}$ | O | Output signal which indicates an error occurred during the current message sequence. |
| 31 | TXDATA A | O | Bipolar serial data output to positive input of bus transceiver. |
| 32 | $\overline{\text{RXDATA A}}$ | I | Bipolar serial input from negative output of bus transceiver. |
| 33 | RTADP | I | Parity bit input for RT address. |
| 34 | RTAD1 | I | Bit 1 of RT address input. |
| 35 | RTAD3 | I | Bit 3 of RT address input. |
| 36 | $\overline{\text{RESET}}$ | I | System reset input - resets all inputs in module. |
| 37 | $\overline{\text{TXDATA B}}$ | O | Bipolar serial data output to negative input bus transceiver. |
| 38 | RXDATA B | I | Bipolar serial data input from positive output of bus transceiver. |
| 39 | 16MHz | I | 16MHz TTL clock input. |
| 40 | GROUND | - | Signal ground. |
| 41 | $\overline{\text{BCSTART}}$ | I | Cycle enable input Logic "0" initiates bus controller message transfer operation. |
| 42 | $\overline{\text{NBGRNT}}$ | O | New bus grant output from RT indicates beginning of message transfer sequence. |
| 43 | $\overline{\text{BITEN}}$ | O | Built in Test enable output indicates RT is transferring BIT word on internal 16 bit bus. |
| 44 | $\overline{\text{WR}}$ | O | Write enable output for control of subsystem memory. |
| 45 | $\overline{\text{BUSGRNT}}$ | I | Bus request input in response to DTREQ. Allows BC/$\overline{\text{RT}}$ to transfer data to subsystem. |
| 46 | $\overline{\text{LOOPERR}}$ | O | Loop error output. Logic "0" indicates failure of loop back transmitted data. |
| 47 | $\overline{\text{SSBUSY}}$ | I | Subsystem busy input for RT status word. |
| 48 | $\overline{\text{ILLCMD}}$ | I | Illegal command input to RT, used to block RT response to an illegal command. |
| 49 | $\overline{\text{ADRINC}}$ | O | Increment output pulse. Goes LOW at the completion of each word transfer to/from subsystem. Can increment external address counter. |
| 50 | CHASSIS | - | Frame ground electricity isolated from signal ground |
| 51 | WC0 | O | LSB of current command word count field. |
| 52 | WC2 | O | Bit 2 of word count field. |
| 53 | WC4 | O | Bit 4 of word count field. |
| 54 | TXINH A | O | Transmitter inhibit output signal for Channel A. |
| 55 | LMC | O | Latched Mode Command. Logic "1" indicates current word command is a mode code word, WC0-WC4. |
| 56 | $\overline{\text{TESTIN}}$ | - | Factory test point. Do not connect. |

## Table 1A – Pin Function Table (78 Pin Plug-In) (continued)

| Pin # | Symbol | I/O | Description |
|---|---|---|---|
| 57 | $\overline{\text{EOM}}$ | O | End of message output. Logic "0" occurs when BC/$\overline{\text{RT}}$ message is completed. |
| 58 | $\overline{\text{BUFENA}}$ | I | Buffer enable input, may be driven LOW by $\overline{\text{STATEN}}$ or $\overline{\text{BITEN}}$ if subsystem must read bit or Status words. Enables internal 16 bit bus onto subsystem bus. |
| 59 | $\overline{\text{BUSACK}}$ | O | Bus acknowledge output. LOW during DMA Handshake, in response to $\overline{\text{BUSGRNT}}$. |
| 60 | DB1 | I/O | Bit 1 of 16 bit parallel bus. |
| 61 | DB3 | I/O | Bit 3 of 16 bit parallel bus. |
| 62 | DB5 | I/O | Bit 5 of 16 bit parallel bus. |
| 63 | DB7 | I/O | Bit 7 of 16 bit parallel bus. |
| 64 | DB9 | I/O | Bit 9 of 16 bit parallel bus. |
| 65 | DB11 | I/O | Bit 11 of 16 bit parallel bus. |
| 66 | DB13 | I/O | Bit 13 of 16 bit parallel bus. |
| 67 | DB15(MSB) | I/O | Bit 15 of 16 bit parallel bus. |
| 68 | $\overline{\text{STATERR}}$ | O | BC output indicates one or more bits set or address mismatch in a received status word. |
| 69 | $\overline{\text{TXDATA A}}$ | O | Bipolar serial data output to negative input of bus transceiver. |
| 70 | RXDATA A | I | Bipolar serial data input from positive output of bus transceiver. |
| 71 | $\overline{\text{NODT}}$ | O | No data input. Logic "0" indicates the 1553 bus is idle; HIGH means device front end is active. |
| 72 | RTAD0 | I | LSB of 5 bit RT address. |
| 73 | RTAD2 | I | Bit 2 of RT address. |
| 74 | RTAD4 | I | Bit 4 of RT address. |
| 75 | $\overline{\text{BCSTRCV}}$ | O | Broadcast receive. Logic "0" means the current command was a broadcast command. |
| 76 | TXDATA B | O | Bipolar serial output to positive input of bus transceiver. |
| 77 | $\overline{\text{RXDATA B}}$ | I | Bipolar serial input from negative output of bus transceiver. |
| 78 | $\overline{\text{SOM}}$ | O | Start of message output indicates beginning of RT/$\overline{\text{BC}}$ message transfer sequence. |

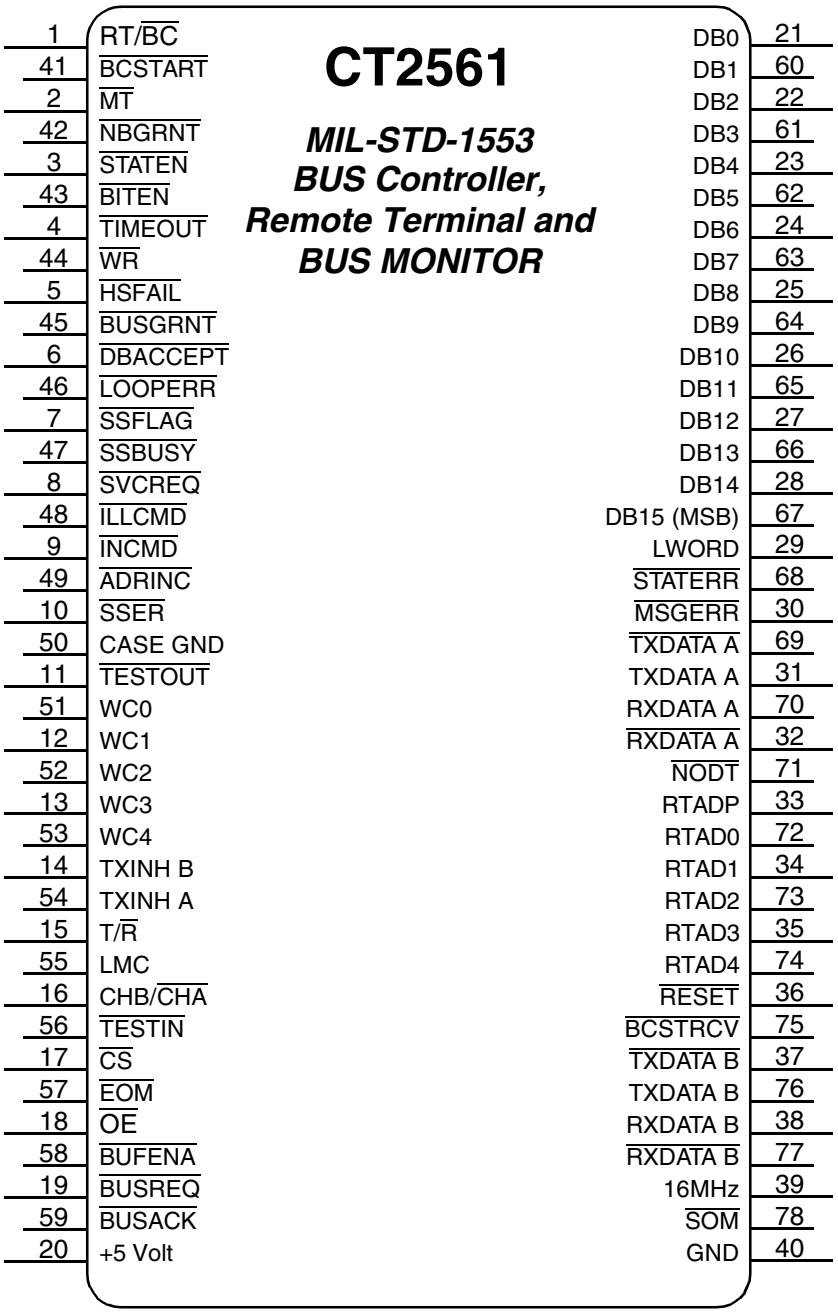


***Table 1B – CT2561 Pin Out Description (Plug-In)***

| Pin # | Function | Pin # | Function |
|---|---|---|---|
| 1 | RT/$\overline{BC}$ | 40 | GND |
| 2 | $\overline{MT}$ | 41 | $\overline{BCSTART}$ |
| 3 | $\overline{STATEN}$ | 42 | $\overline{NBGRNT}$ |
| 4 | $\overline{TIMEOUT}$ | 43 | $\overline{BITEN}$ |
| 5 | $\overline{HSFAIL}$ | 44 | $\overline{WR}$ |
| 6 | $\overline{DBACCEPT}$ | 45 | $\overline{BUSGRNT}$ |
| 7 | $\overline{SSFLAG}$ | 46 | $\overline{LOOPERR}$ |
| 8 | $\overline{SVCREQ}$ | 47 | $\overline{SSBUSY}$ |
| 9 | $\overline{INCMD}$ | 48 | $\overline{ILLCMD}$ |
| 10 | $\overline{SSER}$ | 49 | $\overline{ADRINC}$ |
| 11 | $\overline{TESTOUT}$ | 50 | CASE GND |
| 12 | WC1 | 51 | WC0 |
| 13 | WC3 | 52 | WC2 |
| 14 | TXINH B | 53 | WC4 |
| 15 | T/$\overline{R}$ | 54 | TXINH A |
| 16 | CHB/$\overline{CHA}$ | 55 | LMC |
| 17 | $\overline{CS}$ | 56 | $\overline{TESTIN}$ |
| 18 | $\overline{OE}$ | 57 | $\overline{EOM}$ |
| 19 | $\overline{BUSREQ}$ | 58 | $\overline{BUFENA}$ |
| 20 | + 5 Volt | 59 | $\overline{BUSACK}$ |
| 21 | DB0 (LSB) | 60 | DB1 |
| 22 | DB2 | 61 | DB3 |
| 23 | DB4 | 62 | DB5 |
| 24 | DB6 | 63 | DB7 |
| 25 | DB8 | 64 | DB9 |
| 26 | DB10 | 65 | DB11 |
| 27 | DB12 | 66 | DB13 |
| 28 | DB14 | 67 | DB15 (MSB) |
| 29 | LWORD | 68 | $\overline{STATERR}$ |
| 30 | $\overline{MSGERR}$ | 69 | $\overline{TXDATA\ A}$ |
| 31 | TXDATA A | 70 | RXDATA A |
| 32 | $\overline{RXDATA\ A}$ | 71 | $\overline{NODT}$ |
| 33 | RTADP | 72 | RTAD0 |
| 34 | RTAD1 | 73 | RTAD2 |
| 35 | RTAD3 | 74 | RTAD4 |
| 36 | $\overline{RESET}$ | 75 | $\overline{BCSTRCV}$ |
| 37 | $\overline{TXDATA\ B}$ | 76 | TXDATA B |
| 38 | RXDATA B | 77 | $\overline{RXDATA\ B}$ |
| 39 | 16MHz | 78 | $\overline{SOM}$ |

***Plug-In Pin Connection Diagram, CT2561 and Pinout***

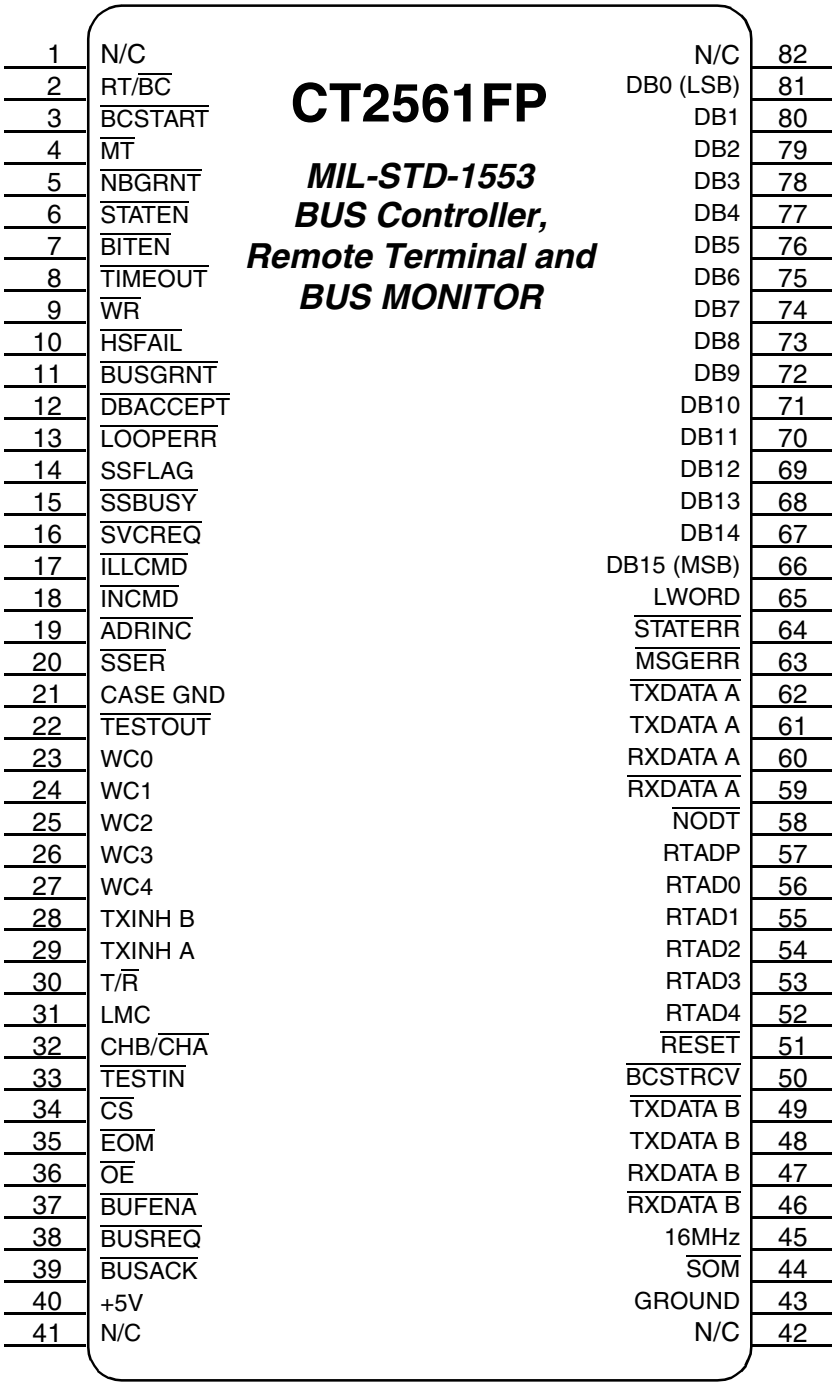


***Table 2 – CT2561 Pin Out Description (FP)***

| Pin # | Function | Pin # | Function |
|---|---|---|---|
| 1 | N/C | 42 | N/C |
| 2 | RT/$\overline{BC}$ | 43 | GROUND |
| 3 | $\overline{BCSTART}$ | 44 | $\overline{SOM}$ |
| 4 | $\overline{MT}$ | 45 | 16MHz |
| 5 | $\overline{NBGRNT}$ | 46 | $\overline{RXDATA\ B}$ |
| 6 | $\overline{STATEN}$ | 47 | RXDATA B |
| 7 | $\overline{BITEN}$ | 48 | TXDATA B |
| 8 | $\overline{TIMEOUT}$ | 49 | $\overline{TXDATA\ B}$ |
| 9 | $\overline{WR}$ | 50 | $\overline{BCSTRCV}$ |
| 10 | $\overline{HSFAIL}$ | 51 | $\overline{RESET}$ |
| 11 | $\overline{BUSGRNT}$ | 52 | RTAD4 |
| 12 | $\overline{DBACCEPT}$ | 53 | RTAD3 |
| 13 | $\overline{LOOPERR}$ | 54 | RTAD2 |
| 14 | SSFLAG | 55 | RTAD1 |
| 15 | $\overline{SSBUSY}$ | 56 | RTAD0 |
| 16 | $\overline{SVCREQ}$ | 57 | RTADP |
| 17 | $\overline{ILLCMD}$ | 58 | $\overline{NODT}$ |
| 18 | $\overline{INCMD}$ | 59 | $\overline{RXDATA\ A}$ |
| 19 | $\overline{ADRINC}$ | 60 | RXDATA A |
| 20 | $\overline{SSER}$ | 61 | TXDATA A |
| 21 | CASE GND | 62 | $\overline{TXDATA\ A}$ |
| 22 | $\overline{TESTOUT}$ | 63 | $\overline{MSGERR}$ |
| 23 | WC0 | 64 | $\overline{STATERR}$ |
| 24 | WC1 | 65 | LWORD |
| 25 | WC2 | 66 | DB15 (MSB) |
| 26 | WC2 | 67 | DB14 |
| 27 | WC4 | 68 | DB13 |
| 28 | TXINH B | 69 | DB12 |
| 29 | TXINH A | 70 | DB11 |
| 30 | T/$\overline{R}$ | 71 | DB10 |
| 31 | LMC | 72 | DB9 |
| 32 | CHB/$\overline{CHA}$ | 73 | DB8 |
| 33 | $\overline{TESTIN}$ | 74 | DB7 |
| 34 | $\overline{CS}$ | 75 | DB6 |
| 35 | $\overline{EOM}$ | 76 | DB5 |
| 36 | $\overline{OE}$ | 77 | DB4 |
| 37 | $\overline{BUFENA}$ | 78 | DB3 |
| 38 | $\overline{BUSREQ}$ | 79 | DB2 |
| 39 | $\overline{BUSACK}$ | 80 | DB1 |
| 40 | +5V | 81 | DB0 (LSB) |
| 41 | N/C | 82 | N/C |

***Flat Package Pin Connection Diagram, CT2561 and Pinout***

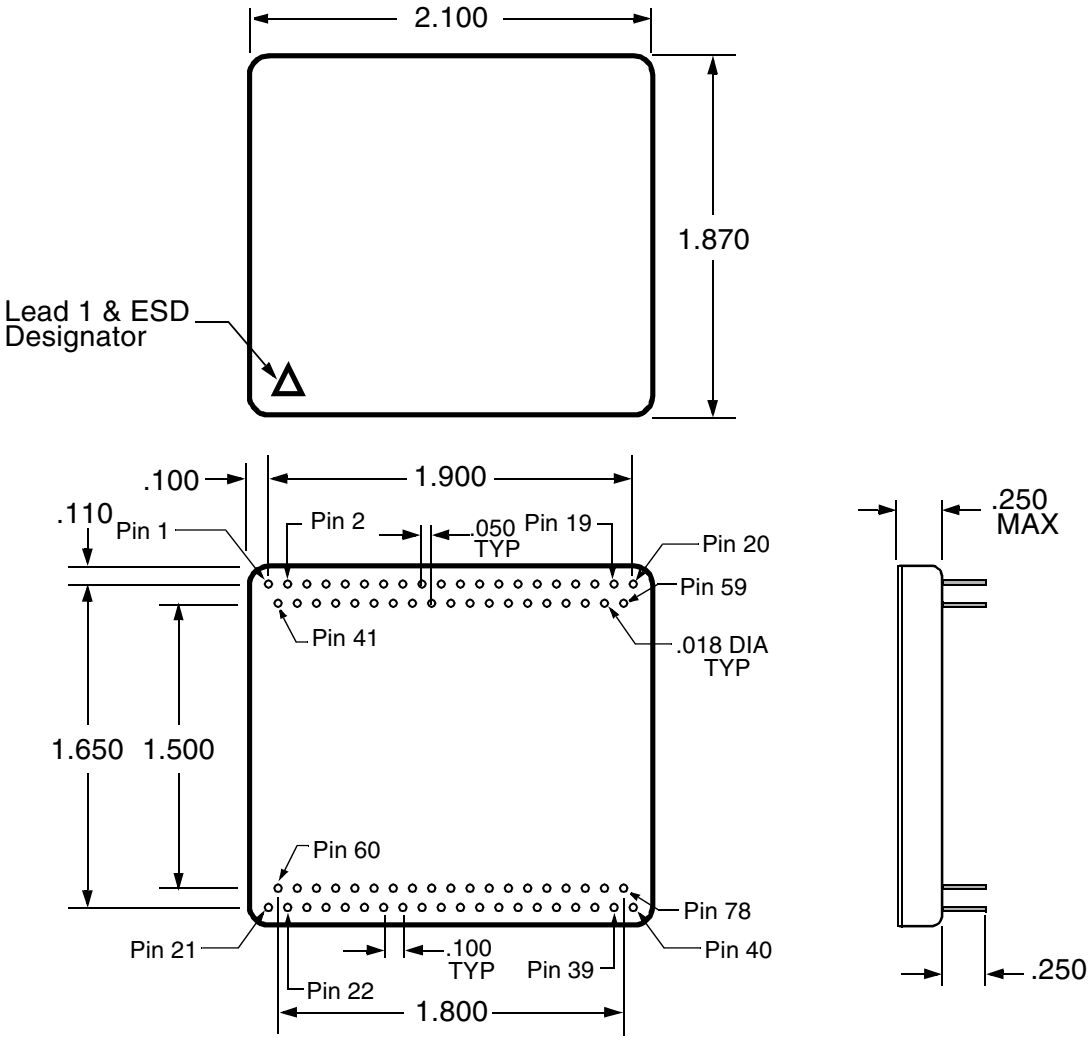


***Figure 2 – Plug In Package Outline***

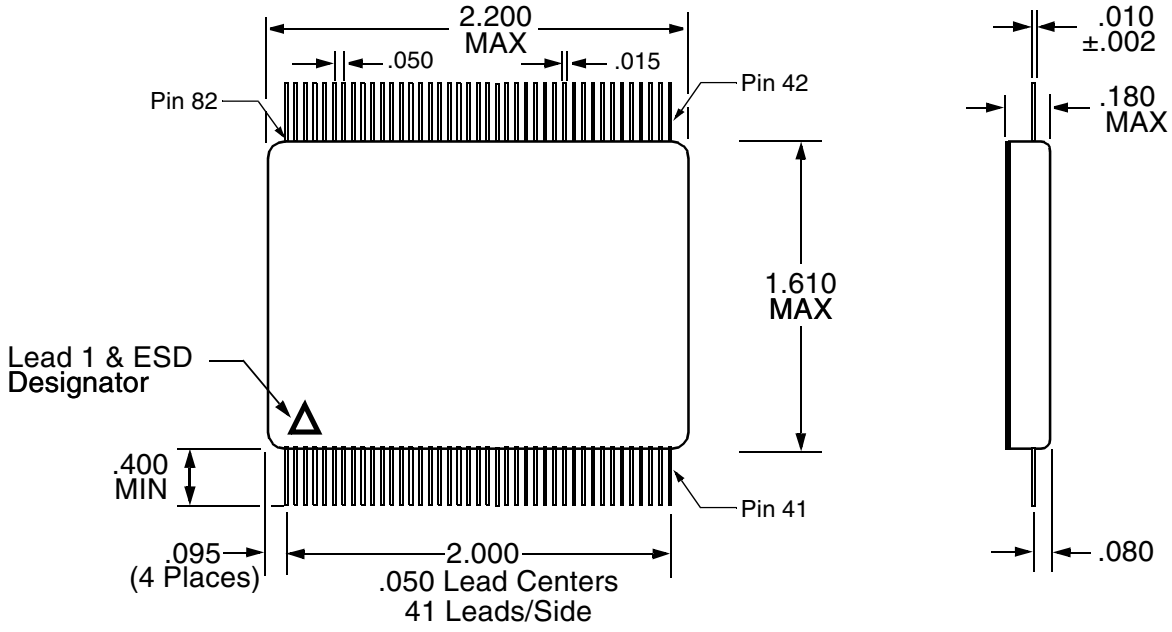


***Figure 3 – Flat Package Outline***

## Ordering Information

| Model Number | Screening | Package |
|---|---|---|
| CT2561 | Military Temperature, -55°C to +125°C, Screened to the individual test methods of MIL-STD-883 | Plug in |
| CT2561-FP | | Flat Package |

**Specifications subject to change without notice**


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