M62370GP

3V TYPE 8-BIT 36CH SELECTOR SW BUILT-IN D-A CONVERTER WITH BUFFER AMPLIFIERS

DESCRIPTION

The M62370GP is a CMOS semiconductor IC,containing 36 channels of 8-bit D-A converters.It is operable with a low supply voltage between 2.7~3.6V,and is easy to use due to serial data input,and 3-pin(DI,CLK,LD)connection with microcomputer.The IC also contains Do pin terminal,enabling cascade connection,and therefore is suitable for automatic control in combination with a microcomputer.

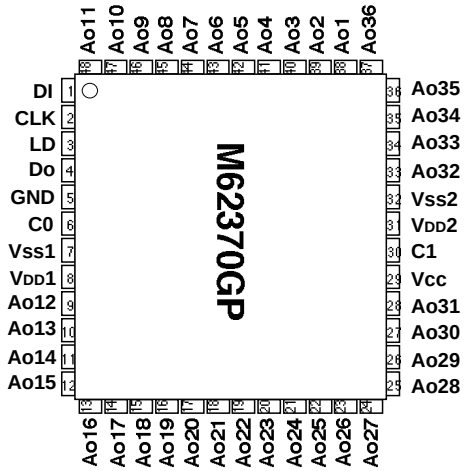
FEATURES

•Operable with a low voltage between 2.7~3.6V
•16-bit serial data input(connected via 3 pins:DI,CLK,LD)
•36 channels built-in of 8-bit D-A converter
•6 channels of D-A converters capable of selecting and outputting 4 data stored in each converter,through 2 control terminals

APPLICATION

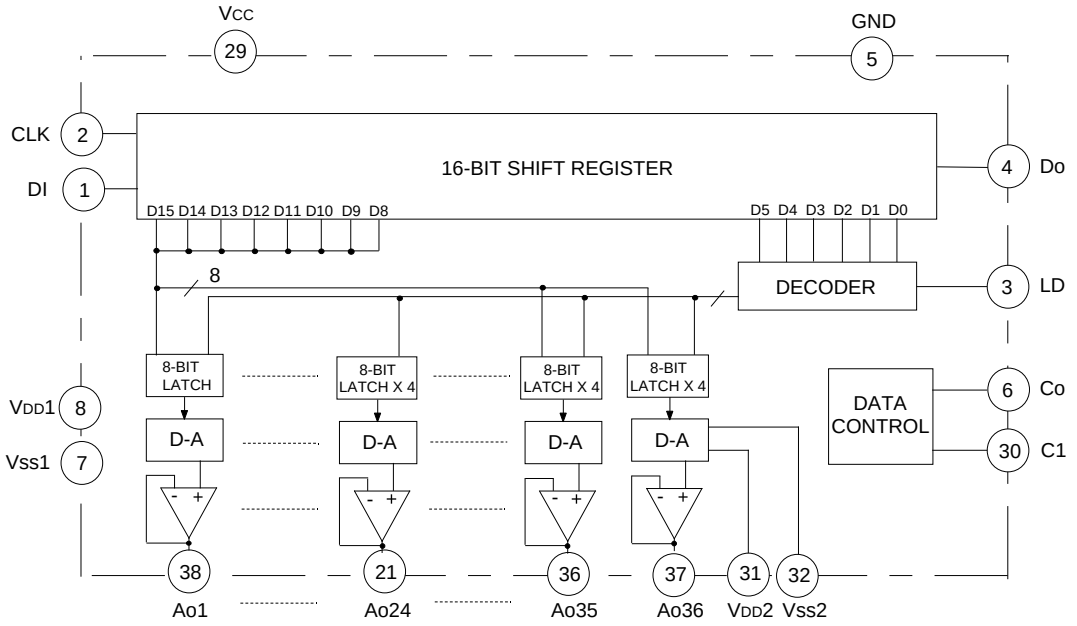
Digital-analog conversion in industrial or home-use electronic equipment.
Automatic control in combination with EEPROM and microcomputer(Substitute for conventional semi-fixed resistor)

PIN CONFIGURATION (TOP VIEW)



Outline 48P6D-A

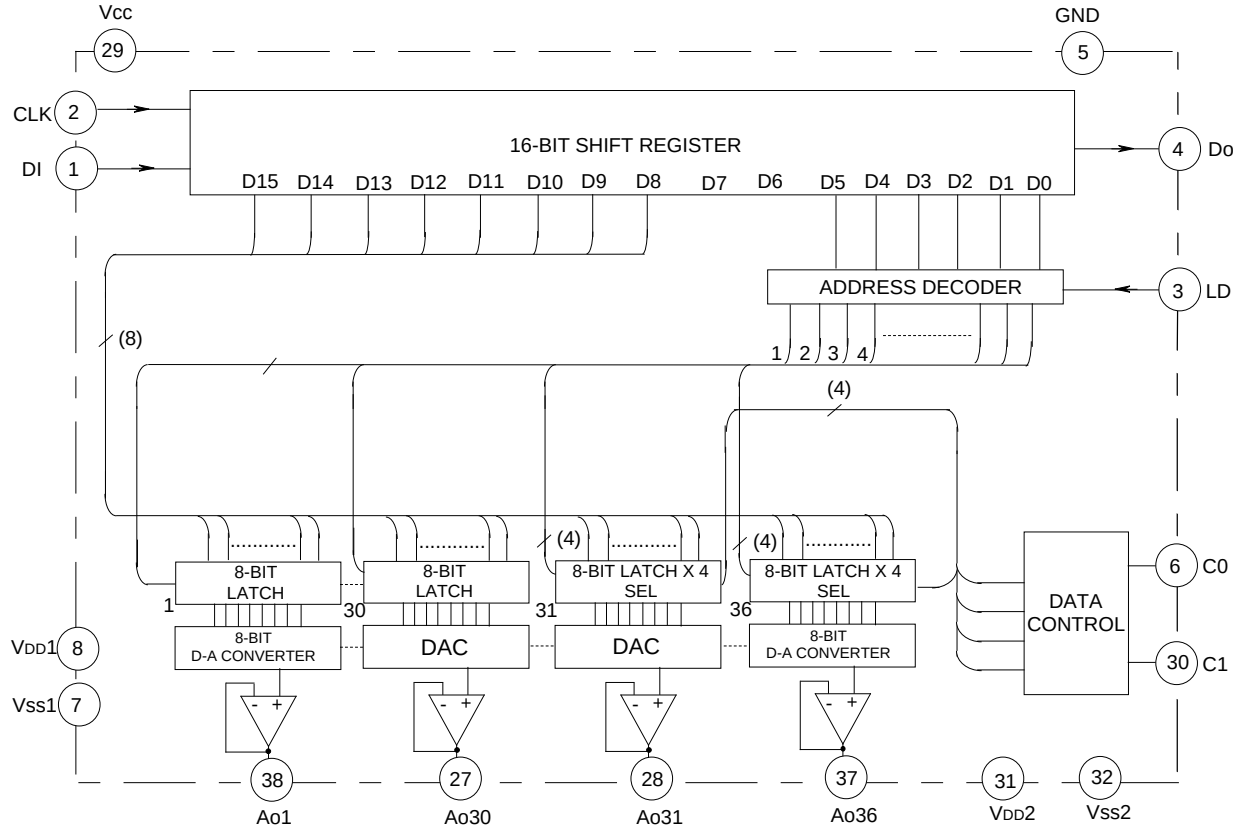
BLOCK DIAGRAM



EXPLANATION OF TERMINALS

Pin No.	Symbol	Function
①	DI	Serial data input terminal to input 16-bit long ssrial data
④	Do	Terminal to output MSB data of 16-bit shift register
②	CLK	Shift clock input terminal.Input signal at DI pin is input to 16-bit shift register at rise of shift clock pulse
③	LD	When H-level signal is input to this terminal,the value stored in 16-bit shift register is loaded in decoder and D-A converter output register
㊳ ≀ ㊽ ⑨ ≀ ㉘ ㉝ ≀ ㊲	Ao1 ≀ Ao11 Ao12 ≀ Ao31 Ao32 ≀ Ao36	8-bit D-A converter output terminal
㉙	V_{CC}	Power supply terminal
⑤	GND	GND terminal
⑥	C0	Data sslect signal input terminal 1 for channel No.31 through 36
㉚	C1	Data select signal input terminal 2 for channel No.31 through 36
⑧	V_{DD1}	Upper reference voltage input terminal and power supply to operational amplifier for channel No.1 through 24
⑦	V_{SS1}	Lower reference voltage input terminal for channel No.1 through 24
㉛	V_{DD2}	Upper reference voltage input terminal and power supply to operational amplifier for channel No.25 through 36
㉜	V_{SS2}	Lower reference voltage input terminal for channel No.25 through 36

BLOCK DIAGRAM FOR EXPLANATION OF TERMINALS



DIGITAL DATA FORMAT

FIRST LSB → LAST MSB

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15

DAC DATA | DAC SELECT DATA

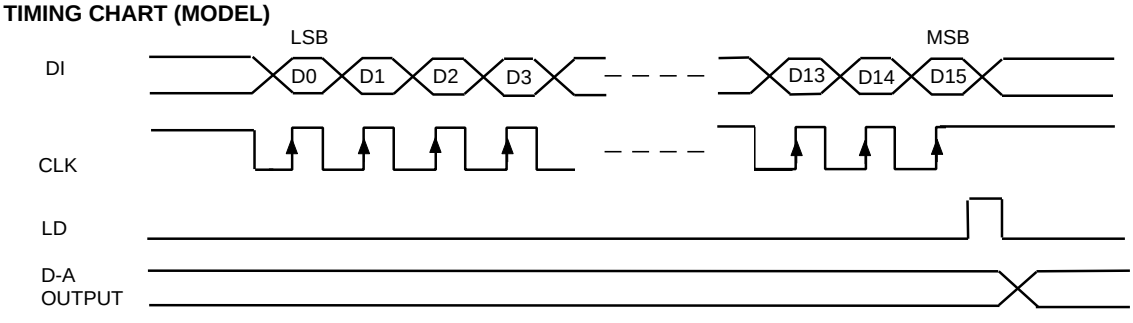
D8	D9	D10	D11	D12	D13	D14	D15	D-A output
0	0	0	0	0	0	0	0	(VrefU-VrefL) / 256 X 1 +VrefL
1	0	0	0	0	0	0	0	(VrefU-VrefL) / 256 X 2 +VrefL
0	1	0	0	0	0	0	0	(VrefU-VrefL) / 256 X 3 +VrefL
1	1	0	0	0	0	0	0	(VrefU-VrefL) / 256 X 4 +VrefL
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	1	1	1	1	1	1	(VrefU-VrefL) / 256 X 255 +VrefL
1	1	1	1	1	1	1	1	VrefU

D5	D4	D3	D2	D1	D0	DAC selection
0	0	0	0	0	0	Don't care
0	0	0	0	0	1	Ao1 selection
0	0	0	0	1	0	Ao2 selection
≀	≀	≀	≀	≀	≀	≀
0	1	1	1	1	0	Ao30 selection
0	1	1	1	1	1	Ao31(0) selection
1	0	0	0	0	0	Ao32(0) selection
≀	≀	≀	≀	≀	≀	≀
1	0	0	1	0	0	Ao36(0) selection
1	0	0	1	0	1	Ao31(1) selection
≀	≀	≀	≀	≀	≀	≀
1	0	1	0	1	0	Ao36(1) selection
1	0	1	0	1	1	Ao31(2) selection
≀	≀	≀	≀	≀	≀	≀
1	1	0	0	0	0	Ao36(2) selection
1	1	0	0	0	1	Ao31(3) selection
≀	≀	≀	≀	≀	≀	≀
1	1	0	1	1	0	Ao36(3) selection
1	1	0	1	1	1	Don't care
≀	≀	≀	≀	≀	≀	≀
1	1	1	1	1	1	Don't care

C0	C1	Ao31 through Ao36 data selected
0	0	Address 0 selected
0	1	Address 1 selected
1	0	Address 2 selected
1	1	Address 3 selected

* VrefU=V_{DD}1,V_{DD}2
VrefL=Vss1,Vss2

TIMING CHART (MODEL)



ABSOLUTE MAXIMUM RATINGS(Ta=25°C,unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		-0.3~+7.0	V
Vo	Output voltage		-0.3~Vcc+0.3	V
Pd	Power dissipation		400	mW
K_θ	Terminal derating	Ta≤25℃	4	mW/℃
Topr	Operating temperature		-20~+85	℃
Tstg	Storage temperature		-40~+125	℃

ELECTRICAL CHARACTERISTICS

Digital part(V_{CC}=+3V±10%, V_{CC}=V_{DD},Ta=-20 ~ +85°C,unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage		2.7	3.0	5.5	V
Icc	Circuit current	CLK=1MHz operation,Vcc=3V,I_{AO}=0μA		1.0		mA
I_{ILK}	Input leak current		-10		10	μA
V_{IL}	Input low voltage				0.6	V
V_{IH}	Input high voltage		2.4			V
V_{OL}	Output low voltage	I_{OL}=2.5mA			0.4	V
V_{OH}	Output high voltage	I_{OH}=-400μA	V_{CC}-0.4			V

Note.Standard value is at Ta=25°C

Analog part(V_{CC}=+3V±10%, V_{CC}=V_{DD},Ta=-20 ~ +85°C,unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{DD}	Current dissipation			5.0		mA
V_{DD}	D-A converter upper reference voltage range		2.7	3.0	5.5	V
Vss	D-A converter lower reference voltage range		GND		V_{DD}-2	V
V_{AO}	Buffer amplifier output voltage range	I_{AO}=±100μA	0.1		V_{DD}-0.1	V
		I_{AO}=+300μA -200μA	0.2		V_{DD}-0.2	
I_{AO}	Buffer amplifier output driving range	Upper saturation voltage=0.4V Lower saturation voltage=0.3V	-300		500	μA
S_{DL}	Differential nonlinearity error	Vcc=2.700V V_{DD}=2.700V Vss=0.050V No load(I_{AO}=±0)	-1.0		1.0	LSB
S_L	Nonlinearity error		-1.5		1.5	LSB
S_{ZERO}	Zero code error		-2		2	LSB
S_{FULL}	Full scale error		-2		2	LSB
Co	Output capacitative load				0.1	μF
Ro	Buffer amplifier output impedance			50		Ω

AC CHARACTERISTICS(V_{CC}=V_{DD},Ta=-20 ~ +85°C,unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{CKL}	Clock "L"pulse width		200			ns
t_{CKH}	Clock "H"pulse width		200			ns
t_{CR}	Clock rise time				200	ns
t_{CF}	Clock fall time				200	ns
t_{DCH}	Data set up time		30			ns
t_{CHD}	Data hold time		60			ns
t_{CHL}	LD set up time		200			ns
t_{LDC}	LD hold time		100			ns
t_{LDH}	LD "H" pulse duration		100			ns
t_{Do}	Data output delay time	C_L=100pF	70		350	ns
t_{LDD}	D-A converter output setting time	CL≤100pF,V_{AO}:0.3⇄2.7V The time until the output becomes the final value of ±2 LSB			100	µs

TIMING CHART