

# M62371GP

## 3 V Type 8-bit 36ch Selector SW Built-in D/A Converter with Buffer Amplifiers

REJ03D0880-0201

Rev.2.01

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### Description

The M62371GP is a CMOS semiconductor IC, containing 36 channels of 8-bit D/A converters. It is operable with a low supply voltage between 2.7 to 3.6 V, and is easy to use due to serial data input, and 3-pin (DI, CLK, LD) connection with microcomputer.

The IC also contains D<sub>O</sub> pin terminal, enabling cascade connection, and therefore is suitable for automatic control in combination with a microcomputer.

(M62371GP is an advanced product of M62370GP on its buffer amp. drivability.)

### Features

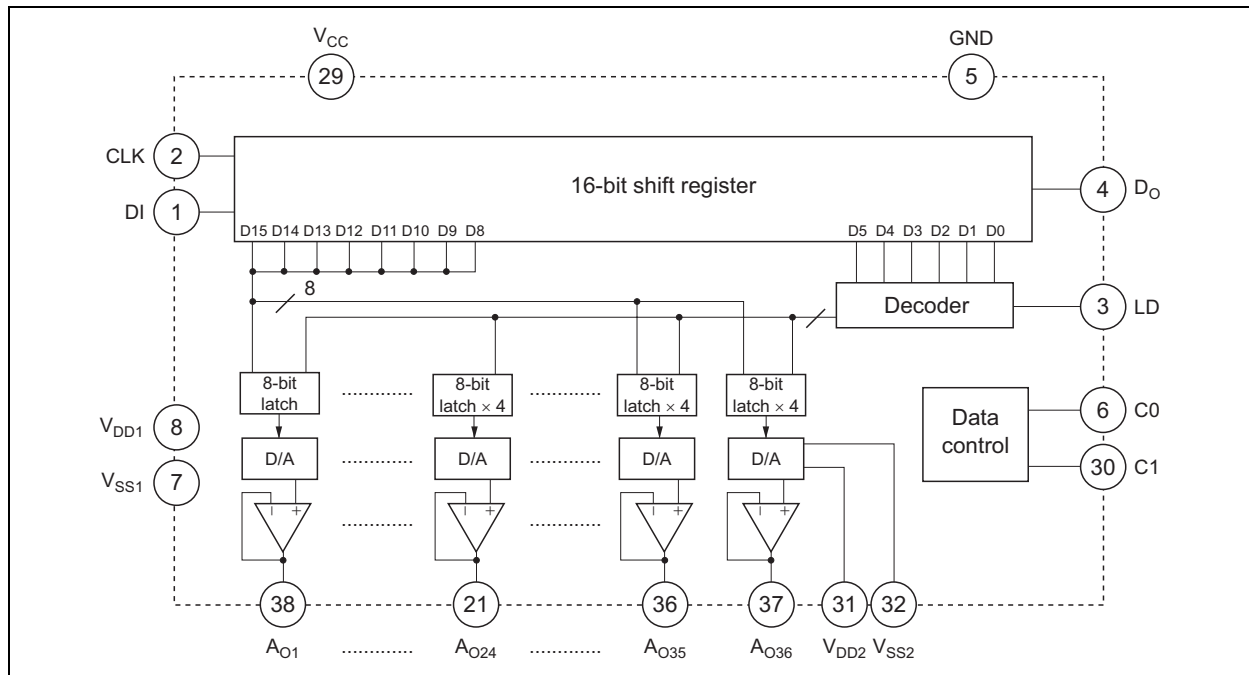
- Operable with a low voltage between 2.7 to 3.6 V
- 16-bit serial data input (connected via 3 pins: DI, CLK, LD)
- 36 channels built-in of 8-bit D/A converter
- 6 channels of D/A converters capable of selecting and outputting 4 data stored in each converter, through 2 control terminals

### Application

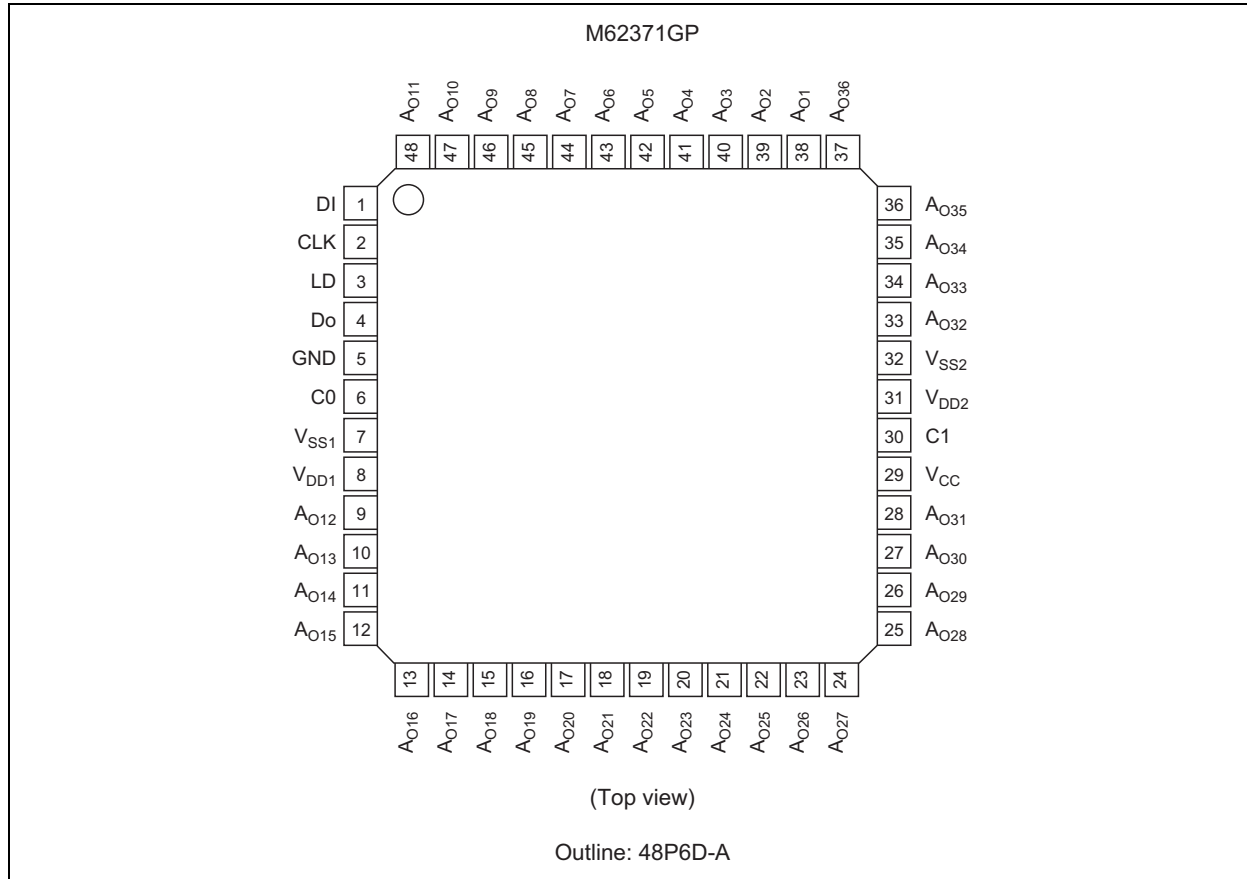
Digital/analog conversion in industrial or home-use electronic equipment.

Automatic control in combination with EEPROM and microcomputer (Substitute for conventional semi-fixed resistor).

### Block Diagram



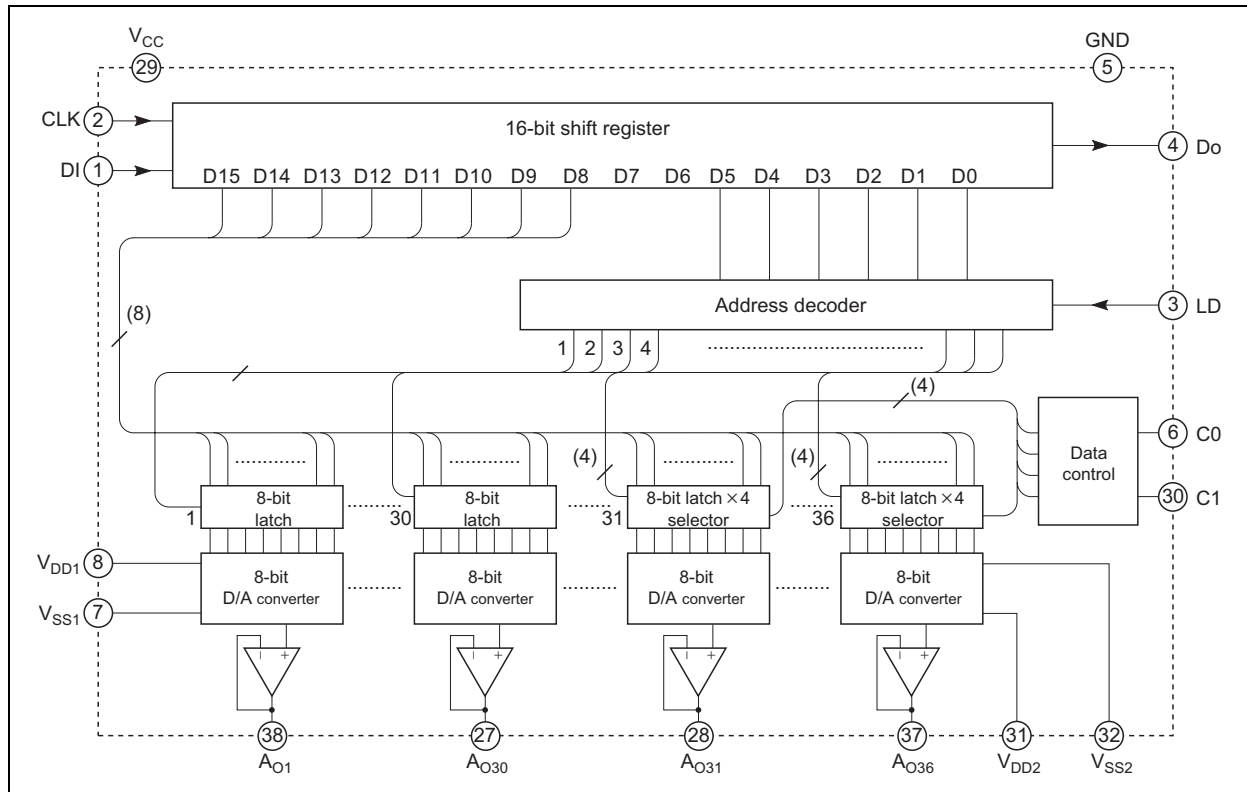
## Pin Arrangement



## Pin Description

Pin No.	Pin Name	Function
1	DI	Serial data input terminal to input 16-bit long serial data
4	Do	Terminal to output MSB data of 16-bit shift register
2	CLK	Shift clock input terminal. Input signal at DI pin is input to 16-bit shift register at rise of shift clock pulse
3	LD	When H-level signal is input to this terminal, the value stored in 16-bit shift register is loaded in decoder and D/A converter output register.
38 to 48	A <sub>O1</sub> to A <sub>O11</sub>	8-bit D/A converter output terminal
9 to 28	A <sub>O12</sub> to A <sub>O31</sub>	
33 to 37	A <sub>O32</sub> to A <sub>O36</sub>	
29	V <sub>CC</sub>	Power supply terminal
5	GND	GND terminal
6	C0	Data select signal input terminal 1 for channel No.31 through 36
30	C1	Data select signal input terminal 2 for channel No.31 through 36
8	V <sub>DD1</sub>	Upper reference voltage input terminal and power supply to operational amplifier for channel No.1 through 24
7	V <sub>SS1</sub>	Lower reference voltage input terminal for channel No.1 through 24
31	V <sub>DD2</sub>	Upper reference voltage input terminal and power supply to operational amplifier for channel No.25 through 36
32	V <sub>SS2</sub>	Lower reference voltage input terminal for channel No.25 through 36

## Block Diagram for Explanation of Terminals



## Absolute Maximum Ratings

(T<sub>a</sub> = 25°C, unless otherwise noted.)

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V <sub>CC</sub>	-0.3 to +7.0	V	
Output voltage	V <sub>O</sub>	-0.3 to V <sub>CC</sub> + 0.3	V	
Power dissipation	P <sub>d</sub>	400	mW	
Thermal derating	K <sub>θ</sub>	4	mW/°C	T <sub>a</sub> ≤ 25°C
Operating temperature	T <sub>opr</sub>	-20 to +85	°C	
Storage temperature	T <sub>stg</sub>	-40 to +125	°C	

## Electrical Characteristics

## &lt;Digital Part&gt;

(V<sub>CC</sub> = +3 V ± 10%, V<sub>CC</sub> = V<sub>DD</sub>, Ta = -20 to +85°C, unless otherwise noted.)

Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Supply voltage	V <sub>CC</sub>	2.7	3.0	5.5	V	
Circuit current	I <sub>CC</sub>	—	1.0	—	mA	CLK = 1 MHz operation, V <sub>CC</sub> = 3 V, I <sub>AO</sub> = 0 μA
Input leak current	I <sub>ILK</sub>	-10	—	10	μA	
Input low voltage	V <sub>IL</sub>	—	—	0.6	V	
Input high voltage	V <sub>IH</sub>	2.4	—	—	V	
Output low voltage	V <sub>OL</sub>	—	—	0.4	V	I <sub>OL</sub> = 2.5 mA
Output high voltage	V <sub>OH</sub>	V <sub>CC</sub> - 0.4	—	—	V	I <sub>OH</sub> = -400 μA

Note: Standard value is at Ta = 25°C

## &lt;Analog Part&gt;

(V<sub>CC</sub> = +3 V ± 10%, V<sub>CC</sub> = V<sub>DD</sub>, Ta = -20 to +85°C, unless otherwise noted.)

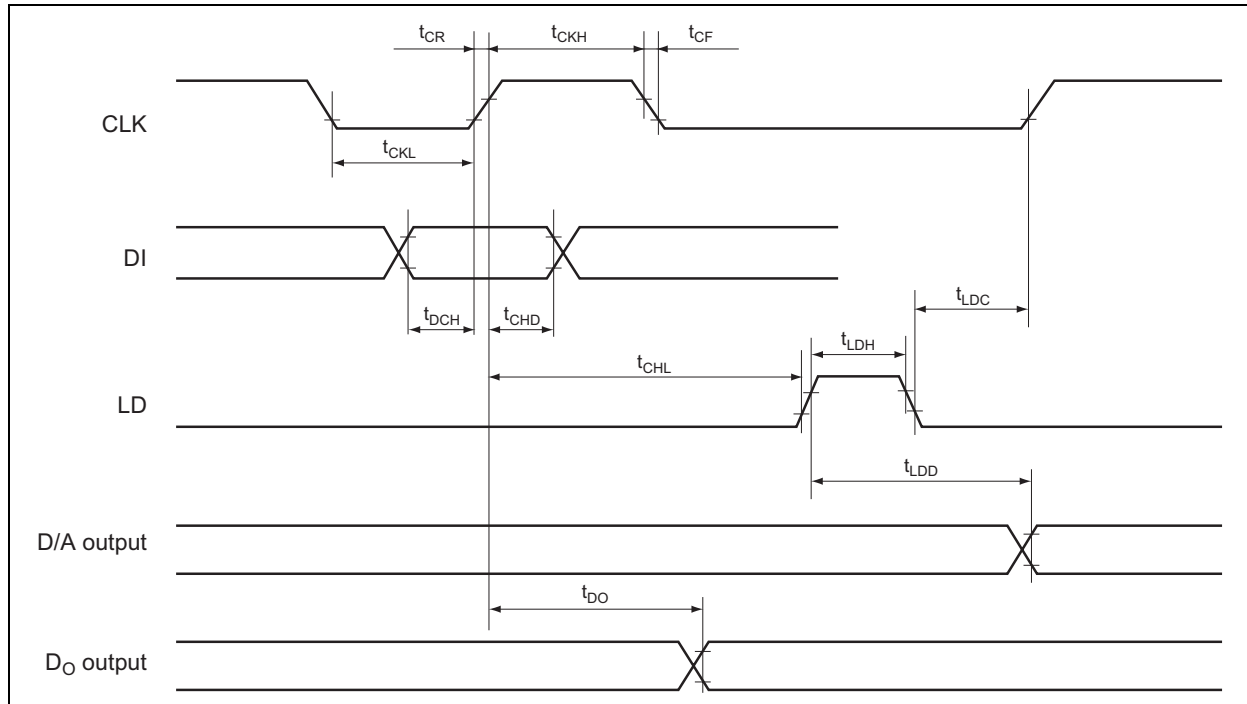
Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Current dissipation	I <sub>DD</sub>	—	8.0	12.0	mA	
D/A converter upper reference voltage range	V <sub>DD</sub>	2.7	3.0	5.5	V	
D/A converter lower reference voltage range	V <sub>SS</sub>	GND	—	V <sub>DD</sub> - 2	V	
Buffer amplifier output voltage range	V <sub>AO</sub>	0.1	—	V <sub>DD</sub> - 0.1	V	I <sub>AO</sub> = ±0.5 mA
		0.2	—	V <sub>DD</sub> - 0.2	V	I <sub>AO</sub> = ±1.0 mA
Buffer amplifier output driving range	I <sub>AO</sub>	-1.5	—	1.5	mA	Upper saturation voltage = 0.4 V Lower saturation voltage = 0.4 V
Differential nonlinearity error	S <sub>DL</sub>	-1.0	—	1.0	LSB	V <sub>CC</sub> = 2.700 V V <sub>DD</sub> = 2.700 V
Nonlinearity error	S <sub>L</sub>	-1.5	—	1.5	LSB	V <sub>SS</sub> = 0.050 V
Zero code error	S <sub>ZERO</sub>	-2	—	2	LSB	No load (I <sub>AO</sub> = ±0)
Full scale error	S <sub>FULL</sub>	-2	—	2	LSB	
Output capacitive load	C <sub>O</sub>	—	—	0.1	μF	
Buffer amplifier output impedance	R <sub>O</sub>	—	50	—	Ω	

## AC Characteristics

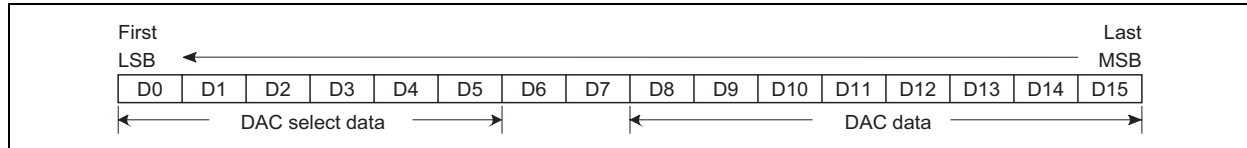
(V<sub>CC</sub> = V<sub>DD</sub>, T<sub>a</sub> = -20 to +85°C, unless otherwise noted.)

Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Clock "L" pulse width	t <sub>CKL</sub>	200	—	—	ns	
Clock "H" pulse width	t <sub>CKH</sub>	200	—	—	ns	
Clock rise time	t <sub>CR</sub>	—	—	200	ns	
Clock fall time	t <sub>CF</sub>	—	—	200	ns	
Data setup time	t <sub>DCH</sub>	30	—	—	ns	
Data hold time	t <sub>CHD</sub>	60	—	—	ns	
LD setup time	t <sub>CHL</sub>	200	—	—	ns	
LD hold time	t <sub>LDC</sub>	100	—	—	ns	
LD "H" pulse duration time	t <sub>LDH</sub>	100	—	—	ns	
Data output delay time	t <sub>DO</sub>	70	—	350	ns	C <sub>L</sub> = 100 pF
D/A converter output setting time	t <sub>LDD</sub>	—	—	100	μs	C <sub>L</sub> ≤ 100 pF, V <sub>AO</sub> : 0.3 V ↔ 2.7 V This time until the output becomes the final value of ±2 LSB

## Timing Chart



## Digital Data Format



### DAC Data

D8	D9	D10	D11	D12	D13	D14	D15	D/A Output
0	0	0	0	0	0	0	0	$(V_{refU} - V_{refL}) / 256 \times 1 + V_{refL}$
1	0	0	0	0	0	0	0	$(V_{refU} - V_{refL}) / 256 \times 2 + V_{refL}$
0	1	0	0	0	0	0	0	$(V_{refU} - V_{refL}) / 256 \times 3 + V_{refL}$
1	1	0	0	0	0	0	0	$(V_{refU} - V_{refL}) / 256 \times 4 + V_{refL}$
:	:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	1	$(V_{refU} - V_{refL}) / 256 \times 255 + V_{refL}$
1	1	1	1	1	1	1	1	$V_{refU}$

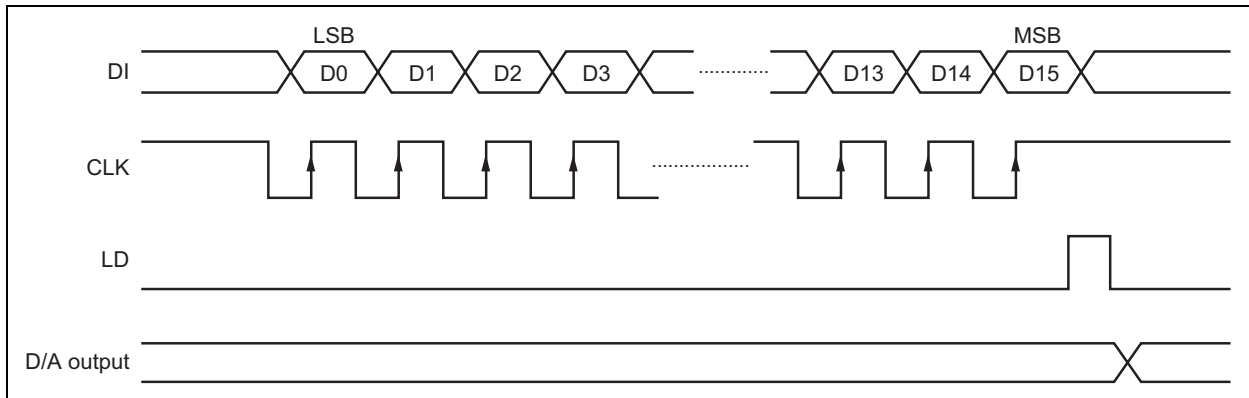
Note:  $V_{refU} = V_{DD1}, V_{DD2}, V_{refL} = V_{SS1}, V_{SS2}$

### DAC Select Data

D5	D4	D3	D2	D1	D0	DAC Selection
0	0	0	0	0	0	Don't care
0	0	0	0	0	1	A <sub>01</sub> selection
0	0	0	0	1	0	A <sub>02</sub> selection
:	:	:	:	:	:	:
0	1	1	1	1	0	A <sub>030</sub> selection
0	1	1	1	1	1	A <sub>031 (0)</sub> selection
1	0	0	0	0	0	A <sub>032 (0)</sub> selection
:	:	:	:	:	:	:
1	0	0	1	0	0	A <sub>036 (0)</sub> selection
1	0	0	1	0	1	A <sub>031 (1)</sub> selection
:	:	:	:	:	:	:
1	0	1	0	1	0	A <sub>036 (1)</sub> selection
1	0	1	0	1	1	A <sub>031 (2)</sub> selection
:	:	:	:	:	:	:
1	1	0	0	0	0	A <sub>036 (2)</sub> selection
1	1	0	0	0	1	A <sub>031 (3)</sub> selection
:	:	:	:	:	:	:
1	1	0	1	1	0	A <sub>036 (3)</sub> selection
1	1	0	1	1	1	Don't care
:	:	:	:	:	:	:
1	1	1	1	1	1	Don't care

C0	C1	A <sub>031</sub> Through A <sub>036</sub> Data Selected
0	0	Address 0 selected
0	1	Address 1 selected
1	0	Address 2 selected
1	1	Address 3 selected

### Timing Chart (Model)

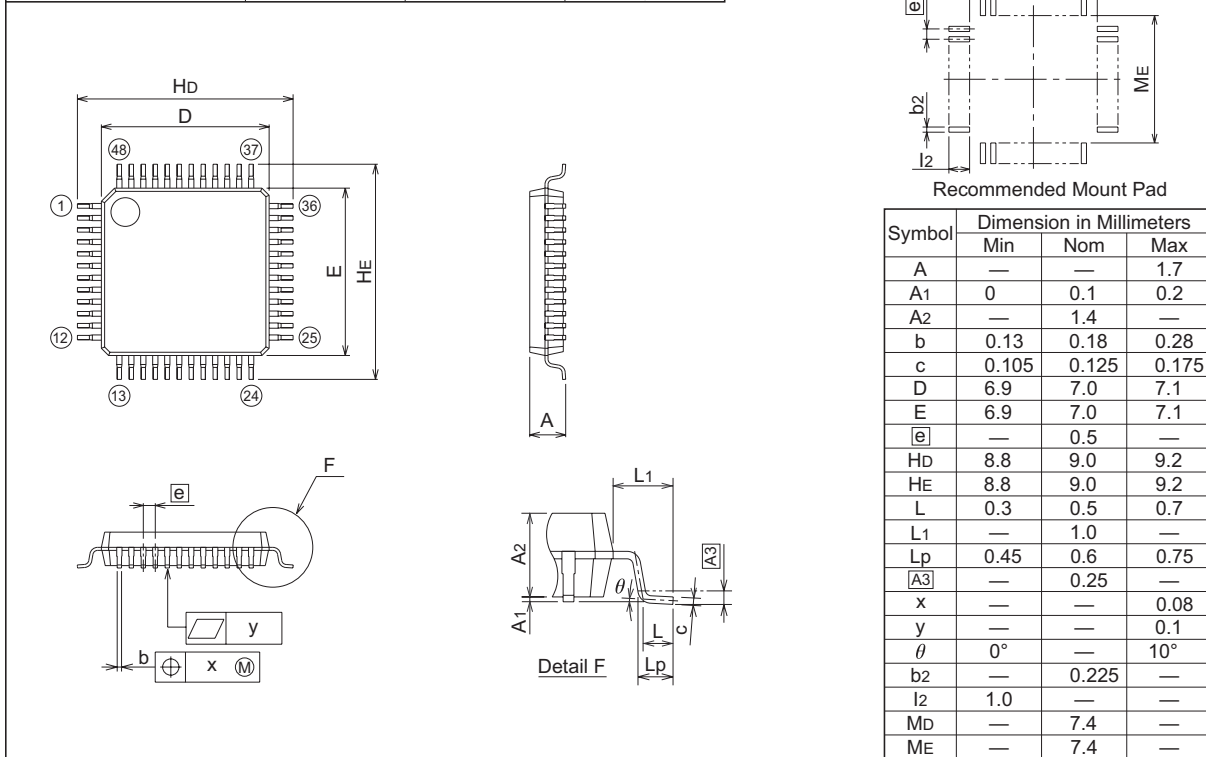


Package Dimensions

48P6D-A

Plastic 48pin 7 × 7mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP48-P-77-0.50	—	0.18	Alloy 42



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.7
A1	0	0.1	0.2
A2	—	1.4	—
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	6.9	7.0	7.1
E	6.9	7.0	7.1
e	—	0.5	—
Hd	8.8	9.0	9.2
HE	8.8	9.0	9.2
L	0.3	0.5	0.7
L1	—	1.0	—
Lp	0.45	0.6	0.75
A3	—	0.25	—
x	—	—	0.08
y	—	—	0.1
$\theta$	0°	—	10°
b2	—	0.225	—
l2	1.0	—	—
Md	—	7.4	—
ME	—	7.4	—



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7th Floor, North Tower, World Finance Centre, Harbour City, Canton Road, Tsimshatsui, Kowloon, Hong Kong  
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10th Floor, No.99, Fushing North Road, Taipei, Taiwan  
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**Renesas Technology Malaysia Sdn. Bhd**

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia  
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