

M62384FP

8-Bit, 4-Channel, 3 to 5 V D-A Converter (Buffered)

REJ03F0077-0100Z

Rev.1.0

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Description

The M62384 is a CMOS-structure semiconductor integrated circuit incorporating four 8-bit D-A converter channels with output buffer op-amps.

Serial data transfer type input can easily be used through a combination of three lines: DI, CLK, and LD. Outputs incorporate buffer op-amps that have a drive capacity of 1 mA or above for both sink and source, and can operate over the entire voltage range from almost ground to VCC (0 to 5 V), making peripheral elements unnecessary and enabling configuration of a system with few component parts.

Support of power supply voltages of 3 V to 5 V enables the M62384 to be used in a wide range of applications.

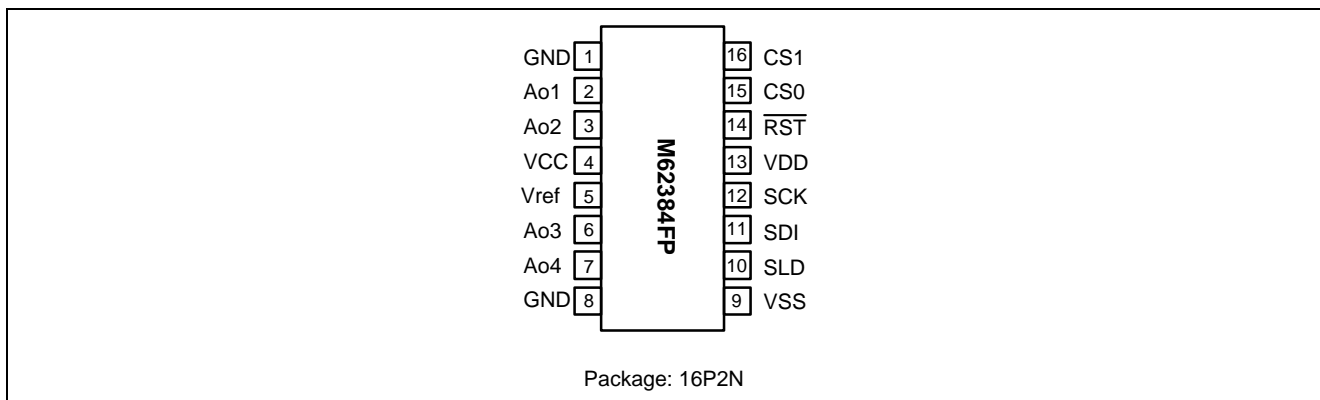
Features

- 12-bit serial data input (3-line type: SDI, SCK, SLD)
- Serial data transfer clock frequency: 10 MHz (max.)
- Output buffer op-amps
Operable over entire voltage range from almost ground to VCC
- Power-on reset and external reset functions
- Chip select function
Up to 4 chips connectable on the same bus
- Supported power supply voltage: 3 V to 5 V (2.7 V to 5.5 V)

Application

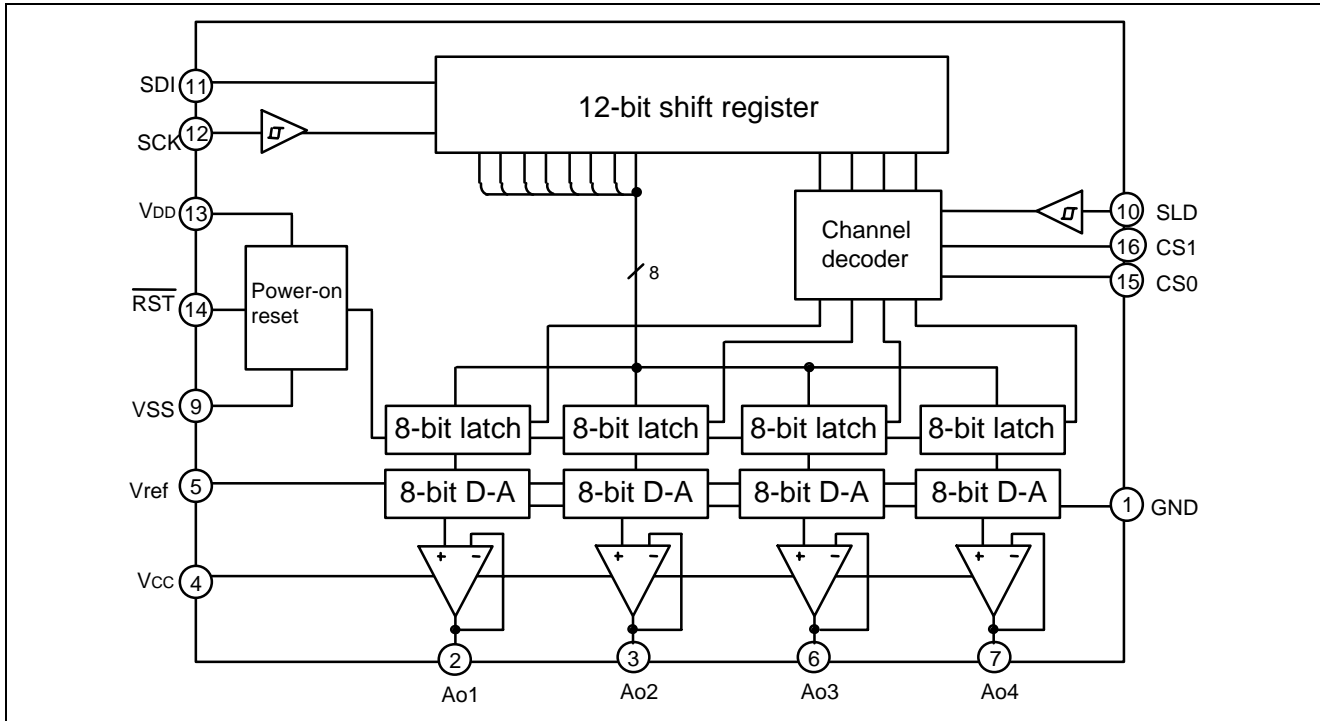
Signal gain setting and automatic adjustment in CTV and display monitors, conversion from digital data to analog data in consumer and industrial products

Pin Connection Diagram (Top View)



This product is currently under development, and specifications and other details may be modified at a future date.

Block Diagram



Pin Functions

Pin No.	Symbol	Function
1, 8	GND	Analog GND: analog circuit GND (D-A converter lower reference voltage)
2	Ao1	D-A converter output pins (ch1 to ch4): full-swing buffer output Output voltage: Ao (00)h = 0V, Ao (FF)h = 255/256 × VREF
3	Ao2	
6	Ao3	
7	Ao4	
4	Vcc	Analog power supply (3 V to 5 V) Must rise simultaneously with VDD or after VDD rise.
5	Vref	D-A converter upper reference voltage input pin
9	Vss	Digital GND
10	SLD	Serial load signal input pin (Schmitt trigger input: with input hysteresis) When SLD is high, data is loaded from shift register into 8-bit latch corresponding to address.
11	SDI	Serial data input pin (TTL input in case of 5 V power supply) Inputs serial data with a 12-bit data length (MSB-first).
12	SCK	Serial clock signal input pin (Schmitt trigger input: with input hysteresis) At rising edge, data is read into shift register one bit at a time.
13	VDD	Digital power supply pin (3 V to 5 V) When power supply rises, D-A output is reset (0 V output: power-on reset).
14	RST	Forced reset pin (TTL input in case of 5 V power supply) L: D-A output (AO1 to 4) = Fixed setting of 0 V H: Reset release (power-on reset operation)
15	CS0	Chip select pins (TTL input in case of 5 V power supply)
16	CS1	Access possible only when chip select data (D11, D10) and pin (CS1, CS0) logic match.

Absolute Maximum Ratings

(Unless specified otherwise, Ta = 25°C)

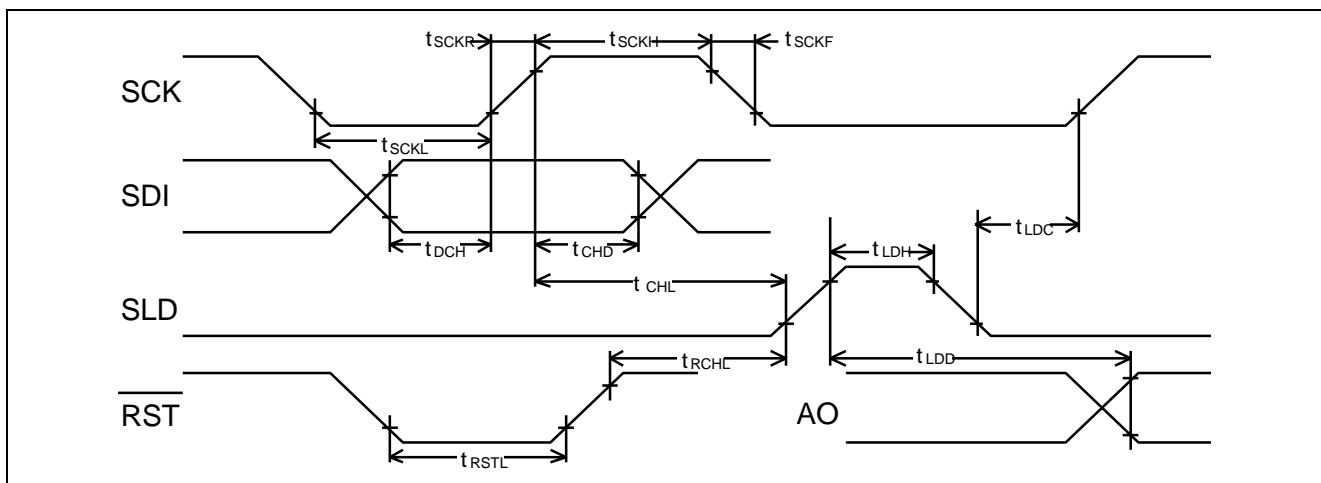
Item	Symbol	Rated Value	Unit	Conditions
Power supply voltage	VCC,VDD	-0.3 to 7.0	V	
Digital input voltage	VDIN	-0.3 to Vcc+0.3 (≤ 7.0)	V	DC voltage ("H" level)
Reference voltage input voltage	Vref	-0.3 to Vcc+0.3 (≤ 7.0)	V	
D-A output voltage	VAO	-0.3 to Vcc+0.3 (≤ 7.0)	V	
Permissible loss	Pd	300	mW	
Operating ambient temperature	Topr	-20 to +75	°C	
Storage temperature	Tstg	-40 to +125	°C	

Recommended Operating Conditions

(Unless specified otherwise, $V_{CC} = V_{DD} = 5\text{ V} \pm 10\%$, $V_{ref} = 2\text{ V to } V_{CC}$, $V_{SS} = \text{GND} = 0\text{ V}$, $f_{sck} = 5\text{ MHz}$, $V_{DINH} = V_{DD}$, $V_{DINL} = V_{SS}$, $T_a = 20^\circ\text{C to } 75^\circ\text{C}$)

Item	Symbol	Specification Values			Unit	Test Conditions
		Min.	Typ.	Max.		
Analog power supply voltage	VCC	2.7		5.5	V	$V_{CC} = V_{DD}$
Digital power supply voltage	VDD	2.7		5.5	V	$V_{CC} = V_{DD}$
Reference voltage	Vref	2.0		5.5	V	$V_{ref} \leq V_{CC}$
Serial clock frequency	fsck			10	MHz	
"H" level digital input voltage	VDINH	0.5VDD		VDD	V	
"L" level digital input voltage	VDINL	VSS		0.2VDD	V	
Clock "H" pulse width	tsckH	30			ns	$V_{CC} = V_{DD} \geq 2.7\text{V}$
Clock "L" pulse width	tsckL	30			ns	$V_{CC} = V_{DD} \geq 2.7\text{V}$
Clock rise time	tsckR			200	ns	
Clock fall time	tsckF			200	ns	
Data setup time	tDCH	10			ns	
Data hold time	tCHD	20			ns	
Load setup time	tCHL	40			ns	
Load hold time	tLDC	20			ns	
Load "H" pulse width	tLDH	20			ns	
Reset "L" pulse width	tRSTL	50			ns	
Load setup time after reset release	tRCHL	50			ns	

Timing Chart



Electrical Characteristics

(Unless specified otherwise, $V_{CC} = V_{DD} = 5\text{ V} \pm 10\%$, $V_{ref} = 2\text{ V}$ to V_{CC} , $V_{SS} = GND = 0\text{ V}$, $f_{sck} = 5\text{ MHz}$, $V_{DINH} = V_{DD}$, $V_{DINL} = V_{SS}$, $T_a = 20^\circ\text{C}$ to 75°C)

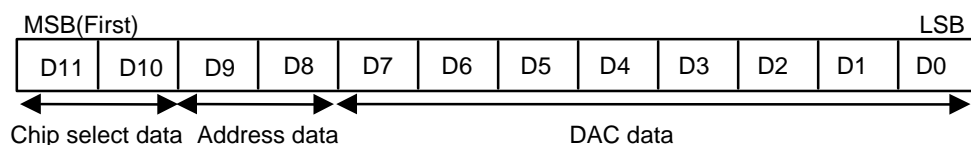
(1) Digital block

Item	Symbol	Specification Values			Unit	Test Conditions
		Min.	Typ.	Max.		
Digital block circuit current	IDD			1.0	mA	
Input leakage current	IDINLK	-10	0	10	μA	$V_{DIN} = V_{SS}$ to V_{DD}
Input threshold voltage	VDINT	0.2VDD		0.5VDD	V	
Input hysteresis voltage	ΔV_{DINT}		100		mV	

(2) Analog block

Item	Symbol	Specification Values			Unit	Test Conditions
		Min.	Typ.	Max.		
Analog block circuit current	ICC		0.8	2.0	mA	No load
Reference voltage input current	Iref		0.5	1.0	mA	All channels: Maximum current conditions
Differential nonlinearity error	SDL	-1.0		1.0	LSB	$V_{CC} = V_{DD} = 2.7\text{V}$ to 5.5V
Nonlinearity error	SNL	-1.5		1.5	LSB	IA0: With no load
Zero scale error	SZERO	-2.0		2.0	LSB	
Full-scale error	SFULL	-2.0		2.0	LSB	
Output current	IAO	± 0.5			mA	$V_{OA} = 0.1\text{V}$ to $V_{CC} - 0.1\text{V}$
Settling time	tLDD		5	10	μs	$V_{OA} = 0.5 \leftrightarrow 4.5\text{V}$, $I_{OA} = 0.1\text{mA}$, $C_o = 50\text{pF}$ output absorbed within $\pm 0.5\text{ LSB}$
Power-on reset voltage	VPR	0.8	1.5	2.5	V	$V_{CC} = 0\text{ V} \rightarrow 5\text{ V}$, $V_{OA} = 0\text{ V}$ setting voltage (reference values)

Digital Data Format



(1) Chip select data

D11	D10	CS1	CS0
0	0	L	L
0	1	L	H
1	0	H	L
1	1	H	H

Data is transferred only when logic of D11 and D10 matches CS pin setting (CS1, CS0).

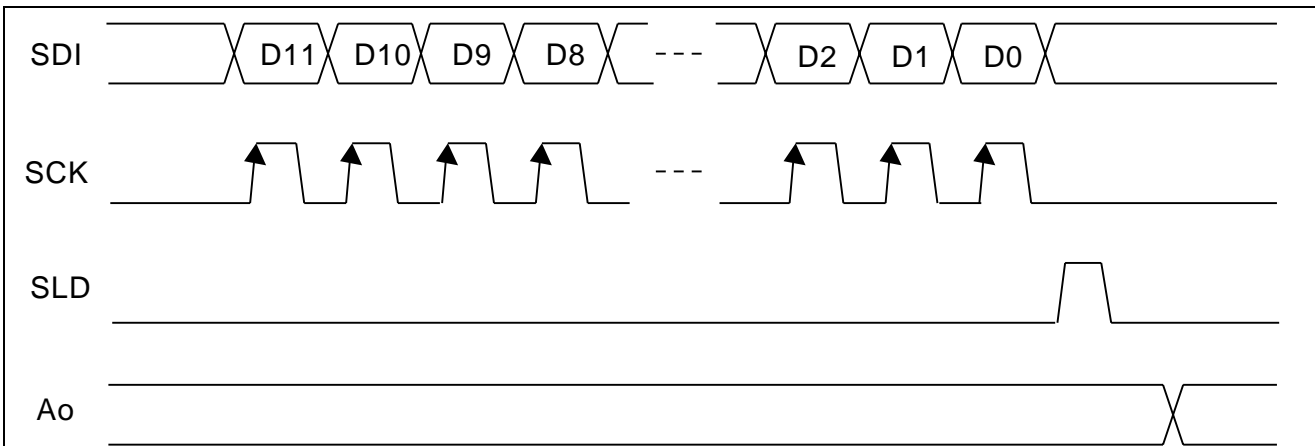
(2) Address data

D8	D9	Channel Selection
0	0	AO1 selected
0	1	AO2 selected
1	0	AO3 selected
1	1	AO4 selected

DAC Data

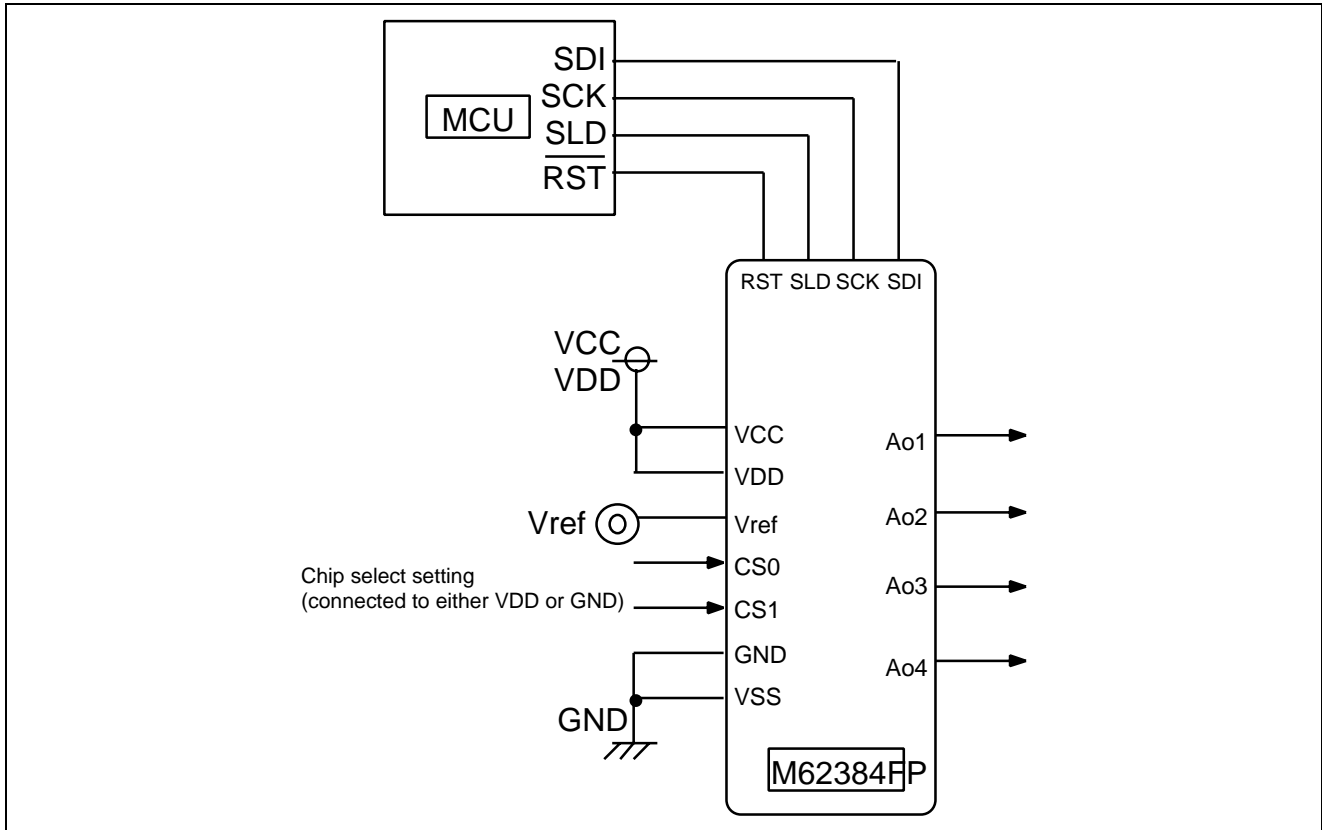
D7	D6	D5	D4	D3	D2	D1	D0	D-A output
0	0	0	0	0	0	0	0	$(0/256) \times V_{ref}$
0	0	0	0	0	0	0	1	$(1/256) \times V_{ref}$
0	0	0	0	0	0	1	0	$(2/256) \times V_{ref}$
0	0	0	0	0	0	1	1	$(3/256) \times V_{ref}$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	1	0	$(254/256) \times V_{ref}$
1	1	1	1	1	1	1	1	$(255/256) \times V_{ref}$

Data Timing Chart



When SLD is high, data captured in the shift register is loaded into the 8-bit latch corresponding to the address. Therefore, SCK should be held high or low when SLD is high.

Sample Application Circuit



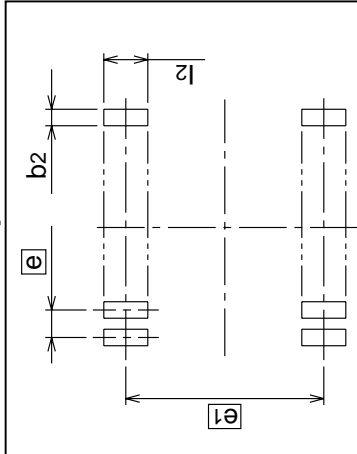
Package Dimensions

16P2N-A

(MMP)

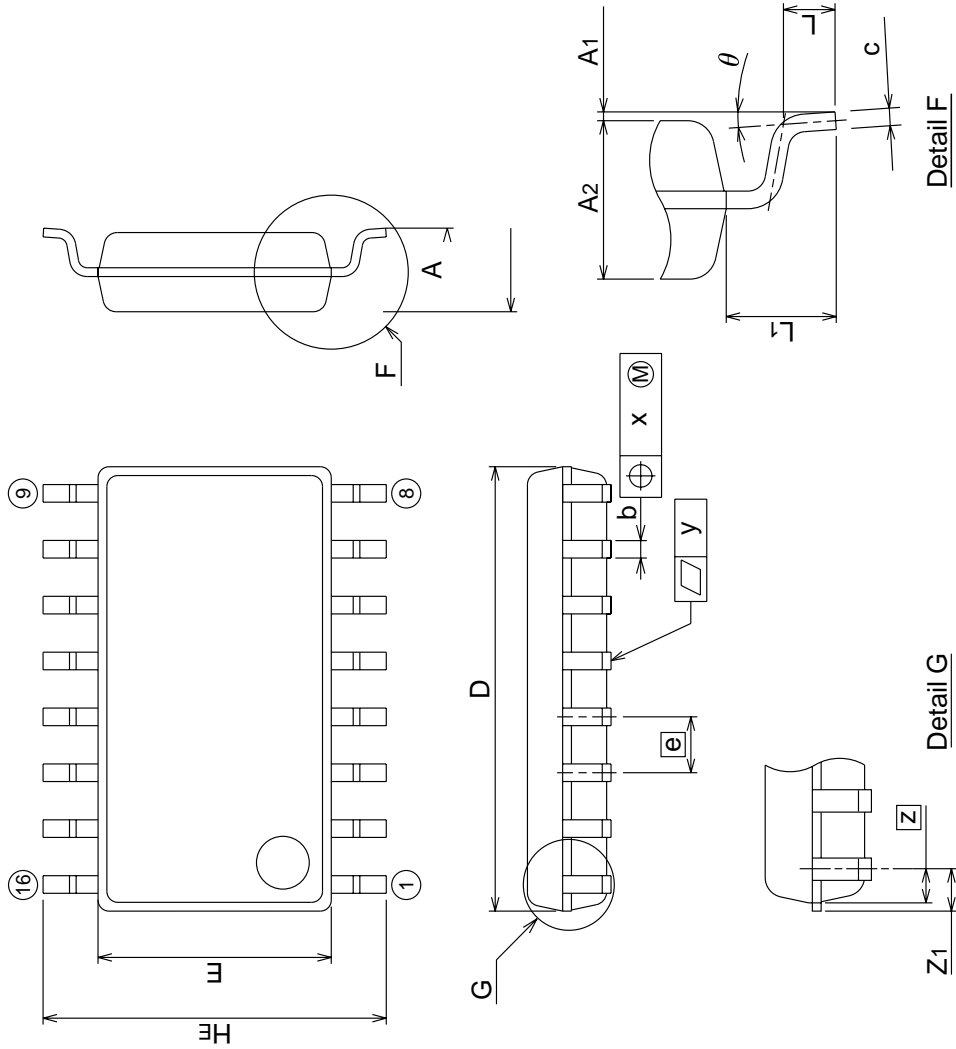
EIAJ Package Code SOP16-P-300-1.27	JEDEC Code —	Weight(g) 0.2	Lead Material Cu Alloy
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Plastic 16pin 300mil SOP



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	0	0.1	2.1
A1	—	1.8	—
A2	0.35	0.4	0.5
b	0.18	0.2	0.25
D	10.0	10.1	10.2
E	5.2	5.3	5.4
e	—	1.27	—
HE	7.5	7.8	8.1
L	0.4	0.6	0.8
L1	—	1.25	—
Z	—	0.605	—
Z1	—	—	0.755
x	—	—	0.25
y	—	—	0.1
θ	0°	—	8°
b2	—	0.76	—
e1	—	7.62	—
l2	1.27	—	—



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