

M62381FP

8-BIT 8CH MULTIPLYING D-A CONVERTER WITH BUFFER AMPLIFIERS

DESCRIPTION

The M62381FP is an integrated circuit semiconductor of CMOS structure with 8 channels of built-in 8-bit resolution multiplication type D-A converters.

The input data is a easy-to-use 3-wire serial transfer method and it is able to cascading serial use with Do terminal.

This device is capable of 4 quadrant multiplication because of built-in inverting type amplifier.

FEATURES

- Digital data transfer method
3-wire 12-bit serial data transfer method(DI,CLK,LD)
- High pressure proof($V_{DD} \pm 5V$)
- Short setting time
- Built-in reset terminal,all the buffer amplifier outputs forces zero volts.

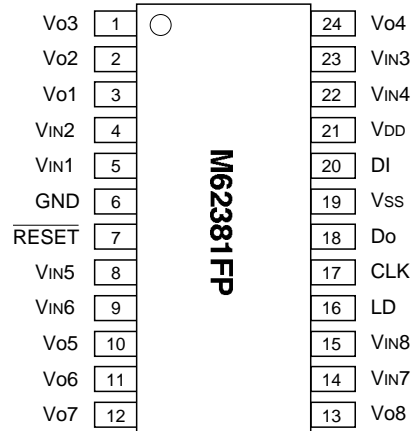
APPLICATION

Signal gain control of DISPLAY-MONITOR or CTV.

Conversion from digital control data analog control data for form-use and industrial equipment.

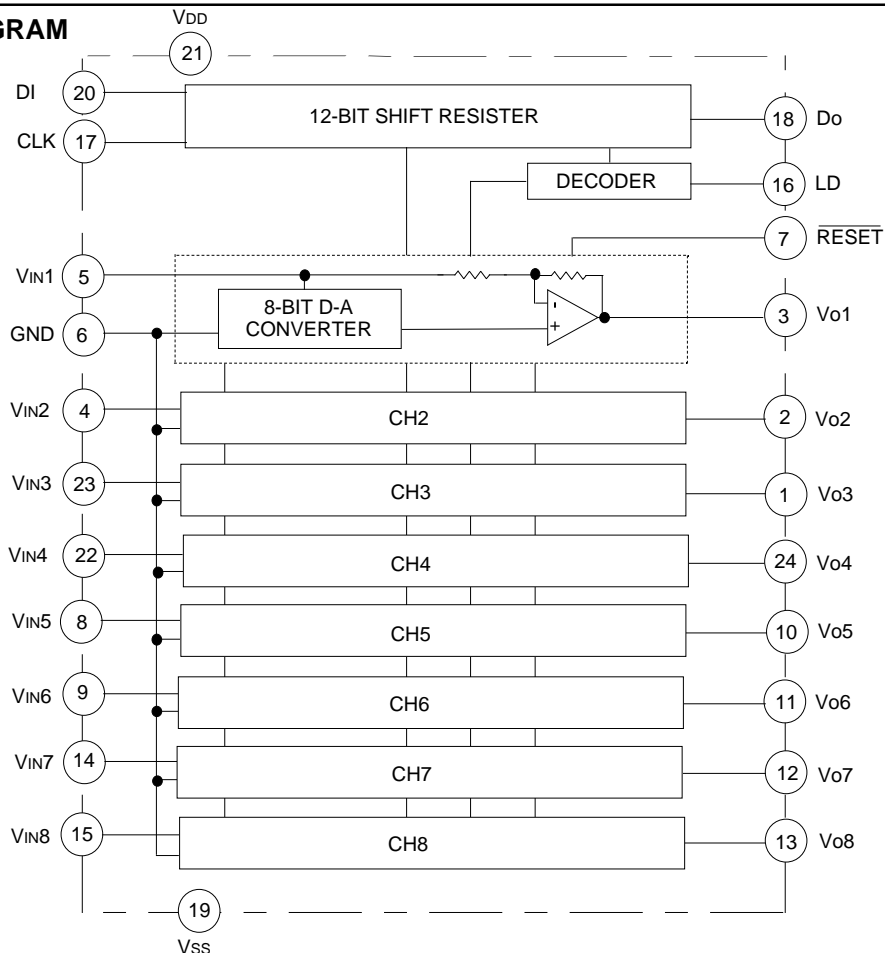
Automatic adjustment by combination with EEPROM and micro-computer.
(replacement of conventional half-fixed resistor.)

PIN CONFIGURATION (TOP VIEW)



Outline 24P2V-A

BLOCK DIAGRAM



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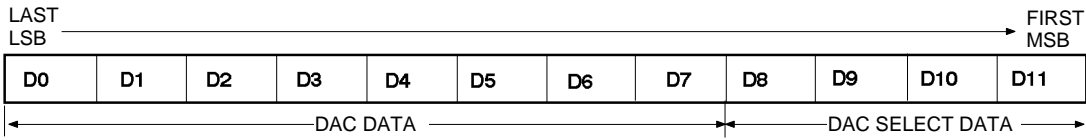
EXPLANATION OF TERMINALS

Pin No.	Symbol	Function
⑳	DI	Serial data input terminal
⑱	Do	Serial data output terminal
⑰	CLK	Serial clock input terminal
⑯	LD	When LD terminal level is "H", latch circuit data is load
③	Vo1	8-bit resolution D-A converter output terminal
②	Vo2	
①	Vo3	
⑳	Vo4	
⑩	Vo5	
⑪	Vo6	
⑫	Vo7	
⑬	Vo8	
㉑	VDD	Analog and digital common power supply terminal
⑲	VSS	Analog negative power supply terminal
⑥	GND	GND terminal
⑤	VIN1	D-A converter reference input terminal
④	VIN2	
㉓	VIN3	
㉒	VIN4	
⑧	VIN5	
⑨	VIN6	
⑭	VIN7	
⑮	VIN8	
⑦	RESET	When RESET terminal level is "H", all D-A output terminal became "0V"

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DIGITAL DATA FORMAT



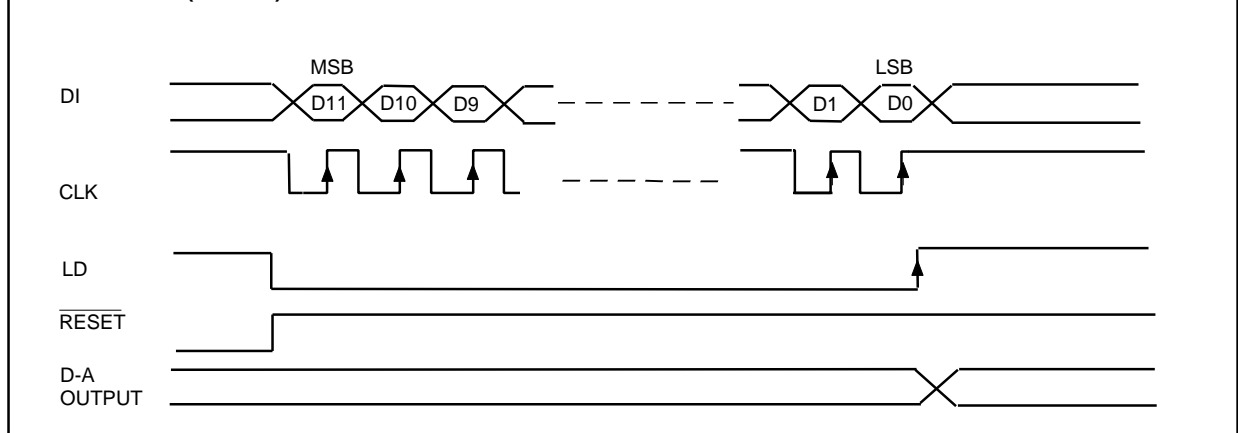
(1) DAC set up data

MSB				LSB				D-A output
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	$-V_{IN}$
0	0	0	0	0	0	0	1	$(1/128-1) \times V_{IN}$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	1	1	1	1	1	1	$(127/128-1) \times V_{IN}$
1	0	0	0	0	0	0	0	$(128/128-1) \times V_{IN}$
1	0	0	0	0	0	0	1	$(129/128-1) \times V_{IN}$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	1	0	$(254/128-1) \times V_{IN}$
1	1	1	1	1	1	1	1	$(255/128-1) \times V_{IN}$

(2) DAC select data

MSB			LSB	DAC selection
D11	D10	D9	D8	
0	0	0	0	Don't care
0	0	0	1	ch1 selection
0	0	1	0	ch2 selection
⋮	⋮	⋮	⋮	⋮
0	1	1	1	ch7 selection
1	0	0	0	ch8 selection
1	0	0	1	Don't care
⋮	⋮	⋮	⋮	⋮
1	1	1	1	Don't care

TIMING CHART (MODEL)



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{DD}	Supply voltage		-0.3 to +6.0	V
V _{IN}	Digital input voltage		-0.3 to +6.0	V
V _{SS}	Analog negative supply voltage		-6.0 to +3.0	V
V _{IN}	Input voltage		V _{SS} +0.3 to V _{DD} -0.3	V
V _O	Output voltage		V _{SS} +0.3 to V _{DD} -0.3	V
T _{opr}	Operating temperature		-20 to +85	°C
T _{stg}	Storage temperature		-40 to +125	°C

ELECTRICAL CHARACTERISTICS

Digital part(V_{DD}=+5V, V_{SS}=-5V, V_{DD}≥V_{IN}≥V_{SS}, GND=0V, T_a=-20 to +85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V _{DD}	Supply voltage		4.5	5.0	5.5	V
I _{ILK}	Input leak current	V _{IN} =0 to V _{CC}	-10		10	μA
V _{IL}	Input low voltage				0.2V _{DD}	V
V _{IH}	Input high voltage		0.8V _{DD}			V
V _{OL}	Output low voltage	I _{OL} =2.5mA			0.4	V
V _{OH}	Output high voltage	I _{OH} =-400μA	V _{DD} -0.4			V

Analog part(V_{DD}=+5V, V_{SS}=-5V, V_{DD}≥V_{IN}≥V_{SS}, GND=0V, T_a=-20 to +85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
I _{IN}	D-A converter reference input current			0.2		mA
V _{AO}	Buffer amplifier output voltage range	I _{AO} =±500μA	VAOZERO +0.15		VAOFULL -0.15	V
I _{AO}	Buffer amplifier output current range	I _{AO} =±1mA	VAOZERO +0.3		VAOFULL -0.3	V
I _{AO}	Buffer amplifier output current range	V _{AO} =V _{AOZERO} +0.3 to V _{AOFULL} -0.3	-1.0		1.0	mA
RES	Resolution		8			bit
DNL	Differential nonlinearity	V _{DD} -0.5≥V _{IN} ≥V _{SS} +0.5	-1.0		1.0	LSB
NL	Nonlinearity		-1.5		1.5	LSB
EG	Gain error		-3		3	%FS

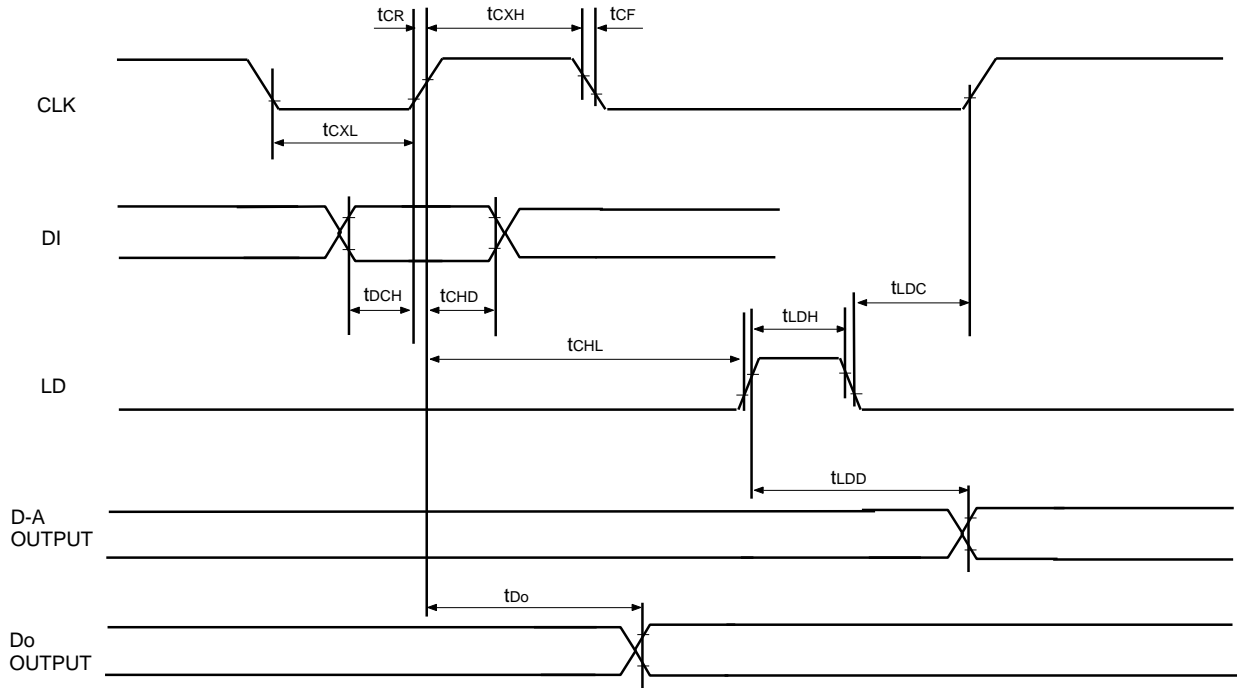
AC CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t _{CXL}	Clock "L" pulse width		200			ns
t _{CXH}	Clock "H" pulse width		200			ns
t _{CR}	Clock rise time				200	ns
t _{CF}	Clock fall time				200	ns
t _{DCH}	Data set up time		30			ns
t _{CHD}	Data hold time		60			ns
t _{CHL}	LD set up time		200			ns
t _{LDH}	LD hold time		100			ns
t _{LDC}	LD "H" pulse width		100			ns
t _{DO}	Data output delay time	C _L =100pF	70		350	ns
t _{LDD}	D-A output setting time	Without load				ns

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TIMING CHART



APPLICATION EXAMPLE

