RENESAS

M62342HP 8-Bit, 2-Channel D/A Converter (Buffered)

> REJ03F0271-0100 Rev.1.00 Mar 25, 2008

Description

The M62342HP is a CMOS-structure semiconductor integrated circuit incorporating two 8-bit D/A converter channels with output buffer op-amps.

Serial data transfer type input can easily be used through a combination of three lines: DI, CLK, and LD.

Outputs incorporate buffer op-amps that have a drive capacity of 1 mA or above for both sink and source, and can operate over the entire voltage range from almost ground to V_{CC} (0 to 5 V), making peripheral elements unnecessary and enabling configuration of a system with few component parts.

This product is currently under development, and specifications and other details may be modified at a future date.

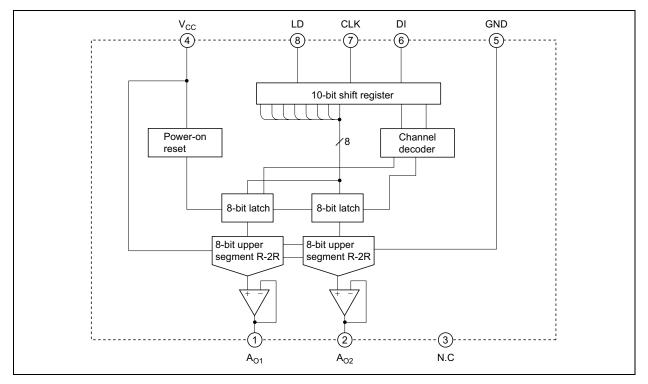
Features

- Data transfer format 10-bit serial data input type
- Output buffer op-amps
 Operable over entire voltage range from almost ground to V_{CC} (0 to 5 V)
- High output current capacity ±1 mA or higher

Application

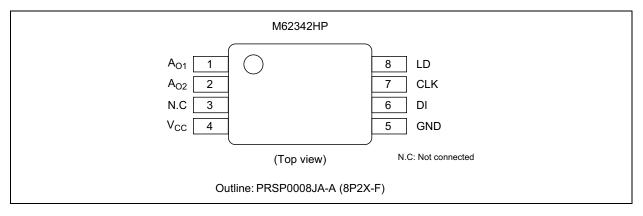
Signal gain setting and automatic adjustment in DSC, CTV, and display monitors, conversion from digital data to analog data in consumer and industrial products

Block Diagram



REJ03F0271-0100 Rev.1.00 Mar 25, 2008 Page 1 of 7 RENESAS

Pin Arrangement



Pin Description

Pin No.	Symbol	Function					
6	DI	Serial data input pin. Inputs serial data with a 10-bit data length.					
7	CLK	Serial clock input pin. Input signal from DI pin is input to 10-bit shift register at rise of shift clock.					
8	LD	Load pin. When "H" level is input to LD pin, value in 10-bit shift register is loaded into decoder and D/A output register.					
1	A _{O1}	8-bit resolution D/A converter output pins					
2	A _{O2}	(After power-on, all channels are reset and DAC data 00h is output.)					
3	N.C.	(Not connected)					
4	V _{CC}	Power supply voltage pin					
5	GND	GND pin					

Absolute Maximum Ratings

Item	Symbol	Rated Value	Unit
Power supply voltage	Power supply voltage V _{CC}		V
Input voltage Vin		–0.3 to $V_{CC}\text{+}0.3 \leq 7.0$	V
Output voltage Vo		–0.3 to V _{CC} +0.3 \leq 7.0	V
Internal power consumption Pd		200	mW
Operating ambient temperature	Topr	-20 to +85	°C
Storage temperature Tstg		-40 to +125	C°

Electrical Characteristics

(Unless specified otherwise, $V_{CC} = +5 \text{ V} \pm 10\%$, GND = 0 V, Ta = -20°C to 85°C)

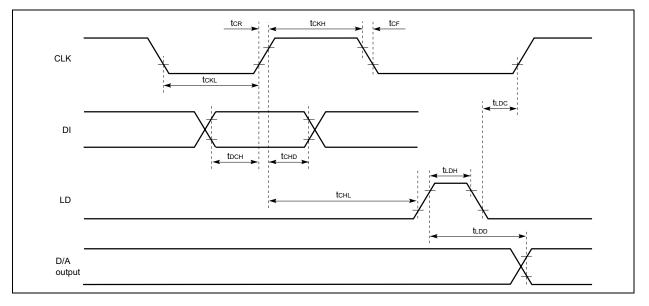
		Spe	cification V	alues			
Item	Symbol	Min	Тур	Max	Unit	Test Conditions	
Power supply voltage	Vcc	2.7	5.0	5.5	V		
Power supply current	Icc	—	0.7	2.5	mA	At CLK = 1 MHz operation, $I_{AO} = 0 \mu A$ D/A data: 6 Ah (at maximum current)	
		_	0.5	1.6		$DI = CLK = LD = GND, I_{AO} = 0 \ \mu A$	
Input leakage current	l _{ILK}	-10	_	10	μΑ	$V_{IN} = 0$ to V_{CC}	
Input voltage "L"	V _{IL}	0	_	0.2V _{CC}	V		
Input voltage "H"	V _{IH}	$0.5V_{CC}$	_	V _{CC}	V		
Buffer amp output	V _{AO}	0.1	_	V _{CC} -0.1	V	$I_{AO} = \pm 100 \ \mu A$	
voltage range		0.1	_	V _{CC} -0.2		$I_{AO} = \pm 500 \ \mu A$	
Buffer amp output drive range	I _{AO}	-1.0	—	1.0	mA	Upper saturation voltage = 0.3 V Lower saturation voltage = 0.2 V	
Differential nonlinearity error	S _{DL}	-1.0	_	1.0	LSB	$V_{CC} = 5.12 \text{ V} (20 \text{ mV/LSB})$ No load (I _{AO} = 0)	
Nonlinearity error	SL	-1.5		1.5	LSB		
Zero point error	SZERO	-2.0	_	2.0	LSB		
Full-scale error	S _{FULL}	-2.0	_	2.0	LSB		
Oscillation limit output capacitance	Co	—	—	0.1	μF		
Buffer amp output impedance	R ₀	—	5.0	—	Ω		

AC Characteristics

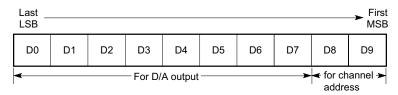
(Unless specified otherwise, $V_{CC} = +5 \text{ V} \pm 10\%$, GND = 0 V, Ta = -20°C to 85°C)

		Specification Values				
Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Clock "L" pulse width	t _{CKL}	200		—	ns	
Clock "H" pulse width	t _{скн}	200		—	ns	
Clock rise time	t _{CR}		-	200	ns	
Clock fall time	t _{CF}	_	_	200	ns	
Data setup time	t _{DCH}	30		—	ns	
Data hold time	t _{CHD}	60		—	ns	
Load setup time	t _{CHL}	200		—	ns	
Load hold time	t _{LDC}	100		—	ns	
Load "H" pulse width	t _{LDH}	100	_	—	ns	
D-A output settling time t _{LDD}		_		300	μS	Until output reaches last 1/2 LSB

Timing Chart



Digital Data Format



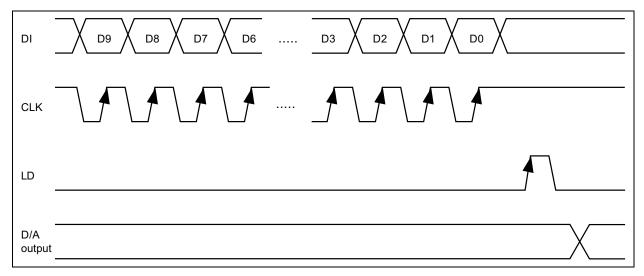
D/A Data

D0	D1	D2	D3	D4	D5	D6	D7	D-A output
0	0	0	0	0	0	0	0	V _{CC} /256×1
1	0	0	0	0	0	0	0	V _{CC} /256×2
0	1	0	0	0	0	0	0	V _{CC} /256×3
1	1	0	0	0	0	0	0	V _{CC} /256×4
	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
0	1	1	1	1	1	1	1	V _{CC} /256×255
1	1	1	1	1	1	1	1	V _{CC} /256×256

Channel Select Data

D8	D9	Channel Selection
0	0	AO1 selected
1	0	AO2 selected
0	1	Don't care
1	1	Don't care

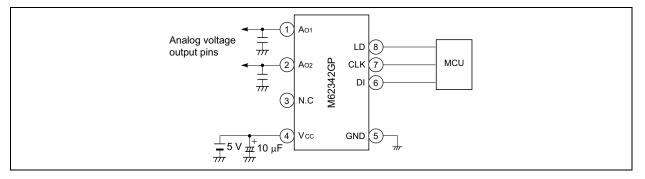
Data Timing Chart (Model)



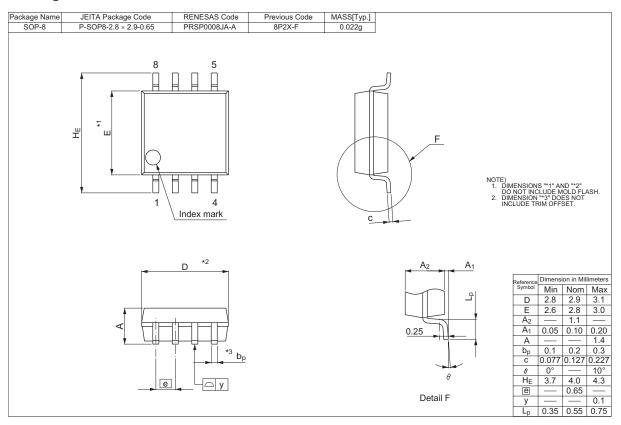
Usage Notes

- 1. With this IC, D/A converter upper reference voltage setting is performed by means of the power supply voltage. If ripples or spikes are imposed on this pin, conversion accuracy may fall. When using this IC, a capacitor must be inserted between the power supply pin and GND in order to ensure stable D/A conversion.
- 2. The output buffer amps of this IC are highly tolerant of capacitive loads. Therefore, connecting capacitors (0.1 μ F max.) between the output pins and ground in order to eliminate jitter or noise due to output line wiring presents no problems whatever in terms of operation.

Sample Standard Application Circuit



Package Dimensions



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