M62342GP

8-Bit, 2-Channel D-A Converter (Buffered)

REJ03F0074-0100Z
Rev.1.0
Sep.19.2003

Description

The M62342GP is a CMOS-structure semiconductor integrated circuit incorporating two 8-bit D-A converter channels with output buffer op-amps.

Serial data transfer type input can easily be used through a combination of three lines: DI, CLK, and LD.

Outputs incorporate buffer op-amps that have a drive capacity of 1 mA or above for both sink and source, and can operate over the entire voltage range from almost ground to VCC (0 to 5 V), making peripheral elements unnecessary and enabling configuration of a system with few component parts.

This product is currently under development, and specifications and other details may be modified at a future date.

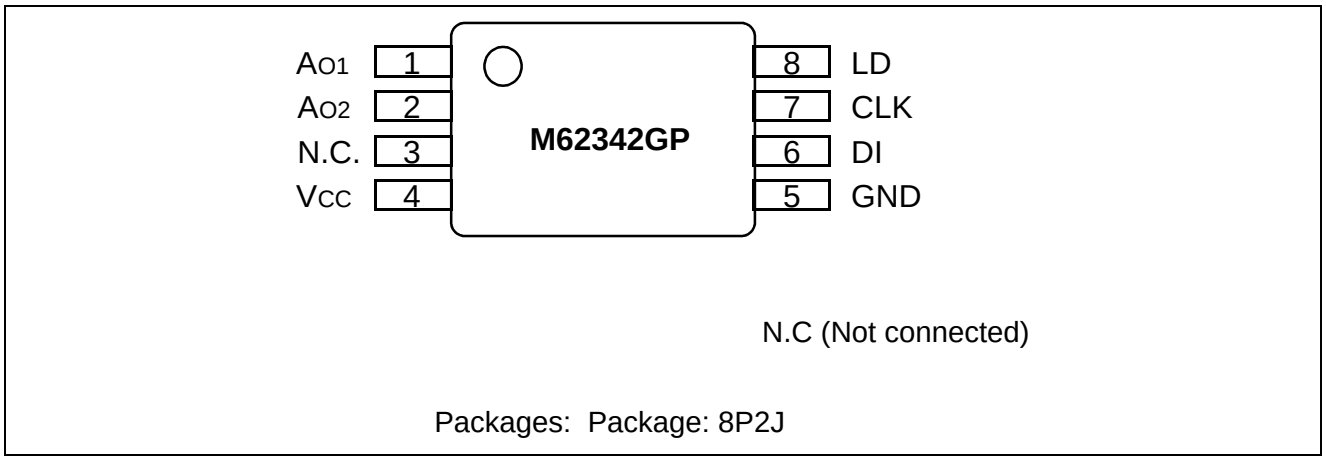
Features

- Data transfer format
  10-bit serial data input type
- Output buffer op-amps
  Operable over entire voltage range from almost ground to VCC (0 to 5 V)
- High output current capacity
  ±1 mA or higher

Application

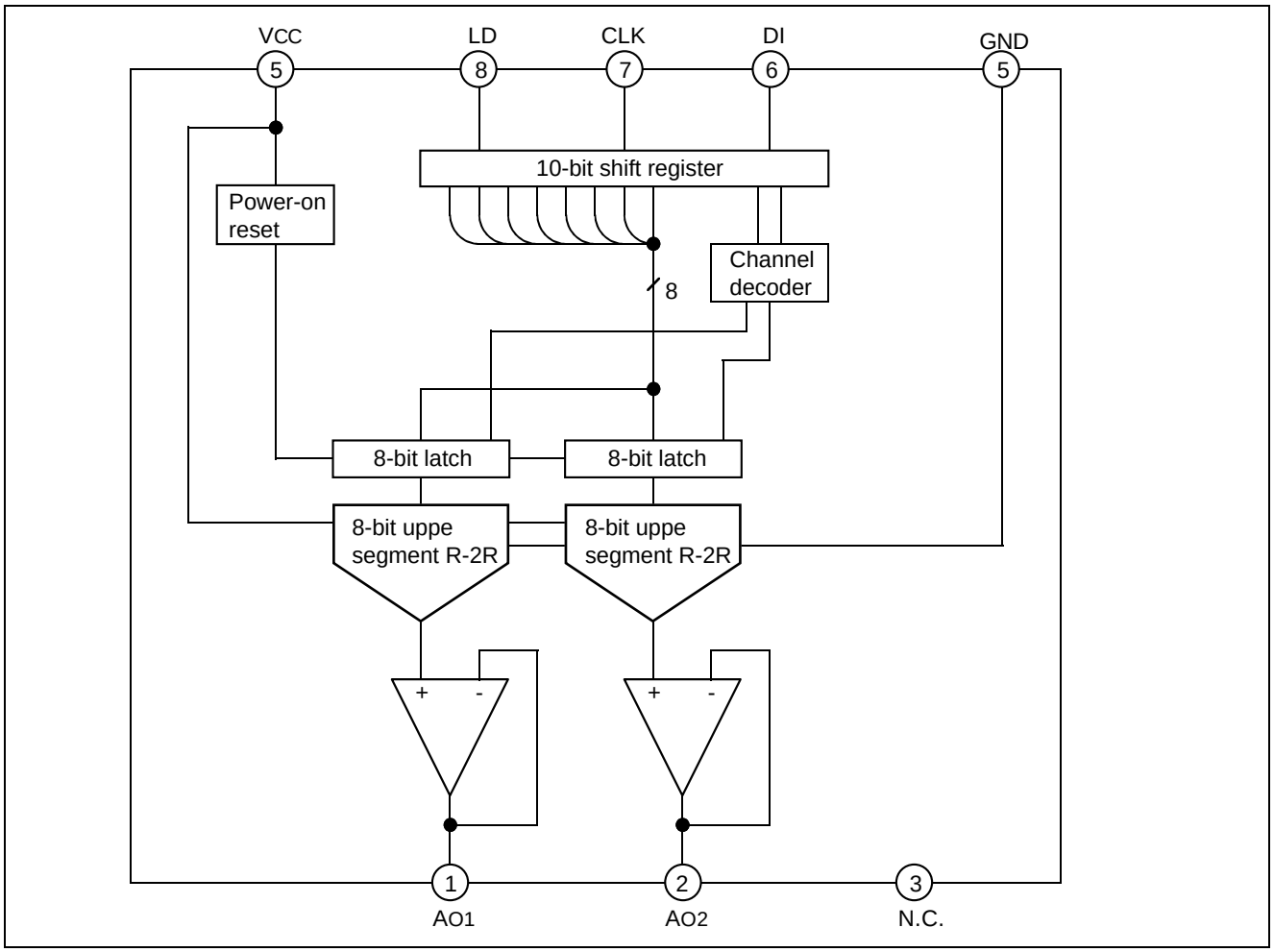
Signal gain setting and automatic adjustment in DSC, CTV, and display monitors, conversion from digital data to analog data in consumer and industrial products

Pin Connection Diagram (Top View)



Packages: Package: 8P2J

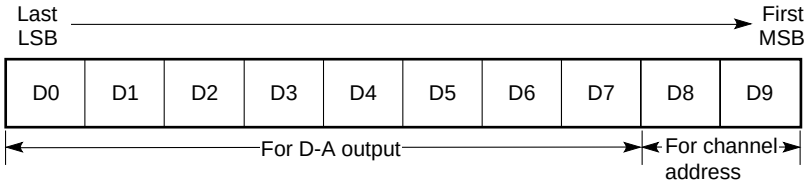
Block Diagram



Pin Description

Pin No.	Symbol	Function
6	DI	Serial data input pin. Inputs serial data with a 10-bit data length.
7	CLK	Serial clock input pin. Input signal from DI pin is input to 10-bit shift register at rise of shift clock.
8	LD	Load pin. When “H” level is input to LD pin, value in 10-bit shift register is loaded into decoder and D-A output register.
1	Ao1	8-bit resolution D-A converter output pins (After power-on, all channels are reset and DAC data 00h is output.)
2	Ao2	
3	N.C.	(Not connected)
4	Vcc	Power supply voltage pin
5	GND	GND pin

Digital Data Format



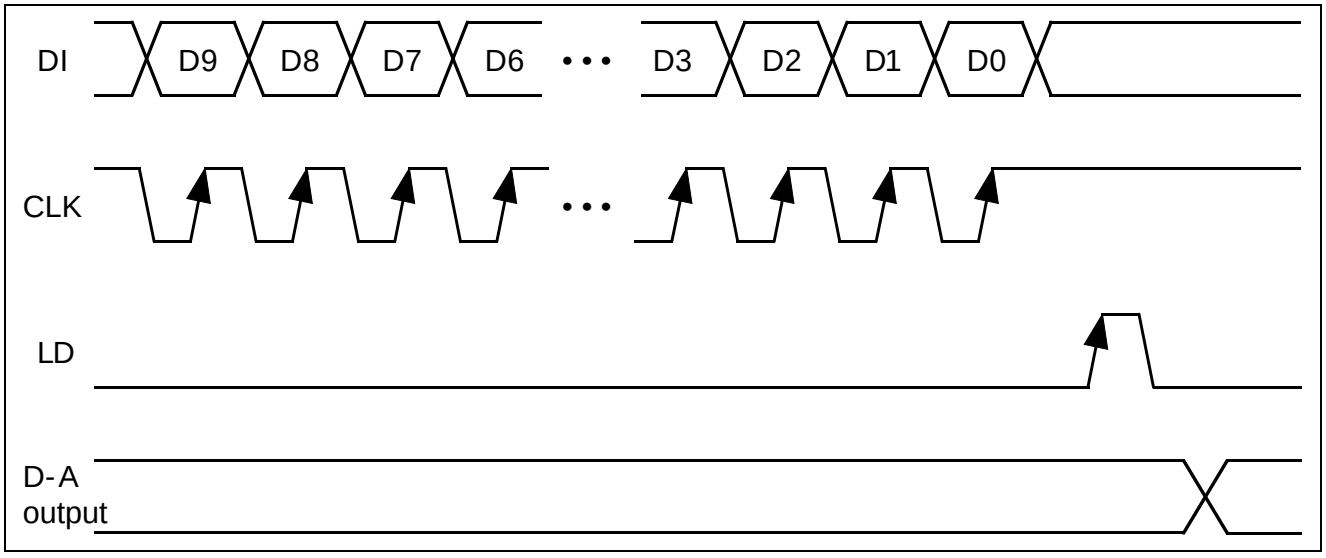
D-A Data

D0	D1	D2	D3	D4	D5	D6	D7	D-A output
0	0	0	0	0	0	0	0	Vcc/256×1
1	0	0	0	0	0	0	0	Vcc/256×2
0	1	0	0	0	0	0	0	Vcc/256×3
1	1	0	0	0	0	0	0	Vcc/256×4
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
0	1	1	1	1	1	1	1	Vcc/256×255
1	1	1	1	1	1	1	1	Vcc/256×256

Channel Select Data

D8	D9	Channel Selection
0	0	AO1 selected
1	0	AO2 selected
0	1	Don't care
1	1	Don't care

Data Timing Chart (Model)



Absolute Maximum Ratings

Item	Symbol	Rated Value	Unit
Power supply voltage	VCC	-0.3 to 7.0	V
Input voltage	Vin	-0.3 to Vcc+0.3 ≤ 7.0	V
Output voltage	Vo	-0.3 to Vcc+0.3 ≤ 7.0	V
Internal power consumption	Pd	200	mW
Operating ambient temperature	Topr	-20 to +85	°C
Storage temperature	Tstg	-55 to +125	°C

Electrical Characteristics

(Unless specified otherwise, VCC = +5 V ±10%, GND = 0 V, Ta = -20ºC to 85ºC)

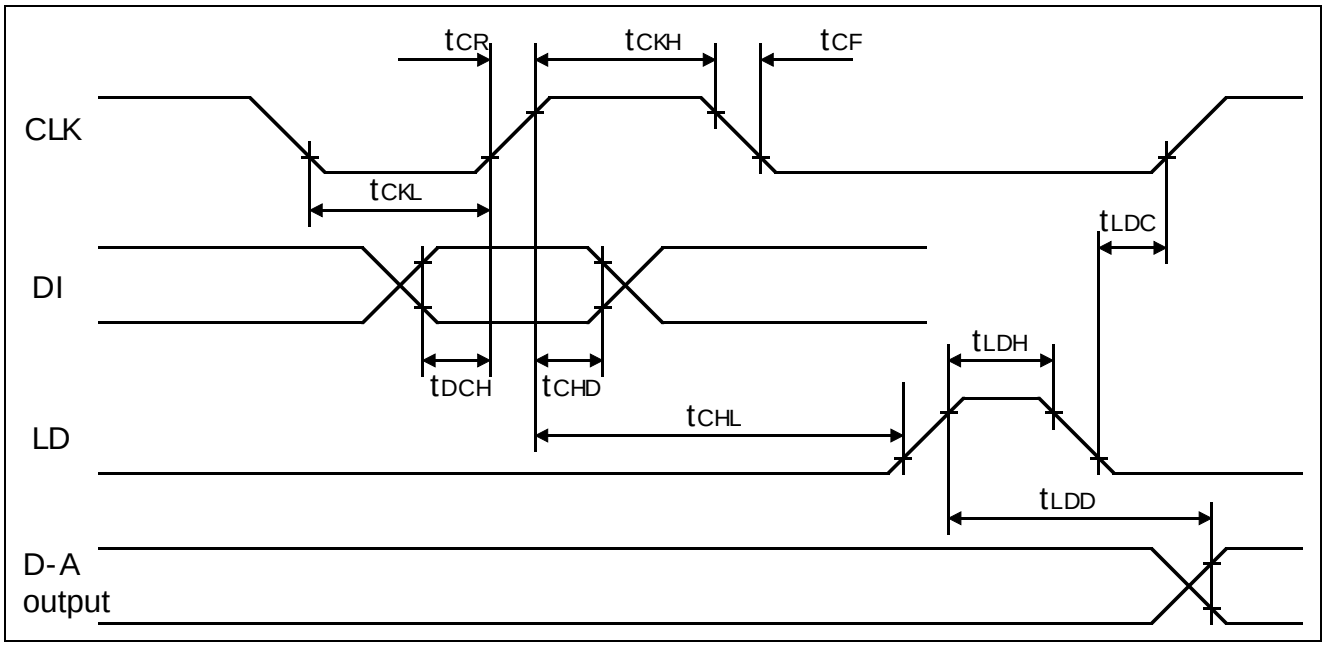
		Specification Values				
Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Power supply voltage	Vcc	2.7	5.0	5.5	V	
Power supply current	Icc	0	0.7	2.5	mA	At CLK = 1 MHz operation, IAO = 0 µA D-A data: 6 Ah (at maximum current)
		0	0.5	1.6		DI = CLK = LD = GND, IAO = 0µA
Input leakage current	IILK	–10		10	µA	VIN = 0 to Vcc
Input voltage “L”	VIL	0		0.2Vcc	V	
Input voltage “H”	VIH	0.5Vcc		Vcc	V	
Buffer amp output voltage range	VAO	0.1		Vcc–0.1	V	IAO = ±100 µA
		0.1		Vcc–0.2		IAO = ±500 µA
Buffer amp output drive range	IAO	–1.0		1.0	mA	Upper saturation voltage = 0.3 V Lower saturation voltage = 0.2 V
Differential nonlinearity error	SDL	–1.0		1.0	LSB	Vcc = 5.12V (20mV/LSB) No load (IAO = 0)
Nonlinearity error	SL	–1.5		1.5	LSB	
Zero point error	SZERO	–2.0		2.0	LSB	
Full-scale error	SFULL	–2.0		2.0	LSB	
Oscillation limit output capacitance	Co			0.1	µF	
Buffer amp output impedance	Ro		5.0			

AC Characteristics

(Unless specified otherwise, VCC = +5 V ±10%, GND = 0 V, Ta = -20ºC to 85ºC)

		Specification Values				
Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Clock “L” pulse width	tCKL	200			ns	
Clock “H” pulse width	tCKH	200			ns	
Clock rise time	tCR			200	ns	
Clock fall time	tCF			200	ns	
Data setup time	tDCH	30			ns	
Data hold time	tCHD	60			ns	
Load setup time	tCHL	200			ns	
Load hold time	tLDC	100			ns	
Load “H” pulse width	tLDH	100			ns	
D-A output settling time	tLDD			300	µs	Until output reaches last 1/2 LSB

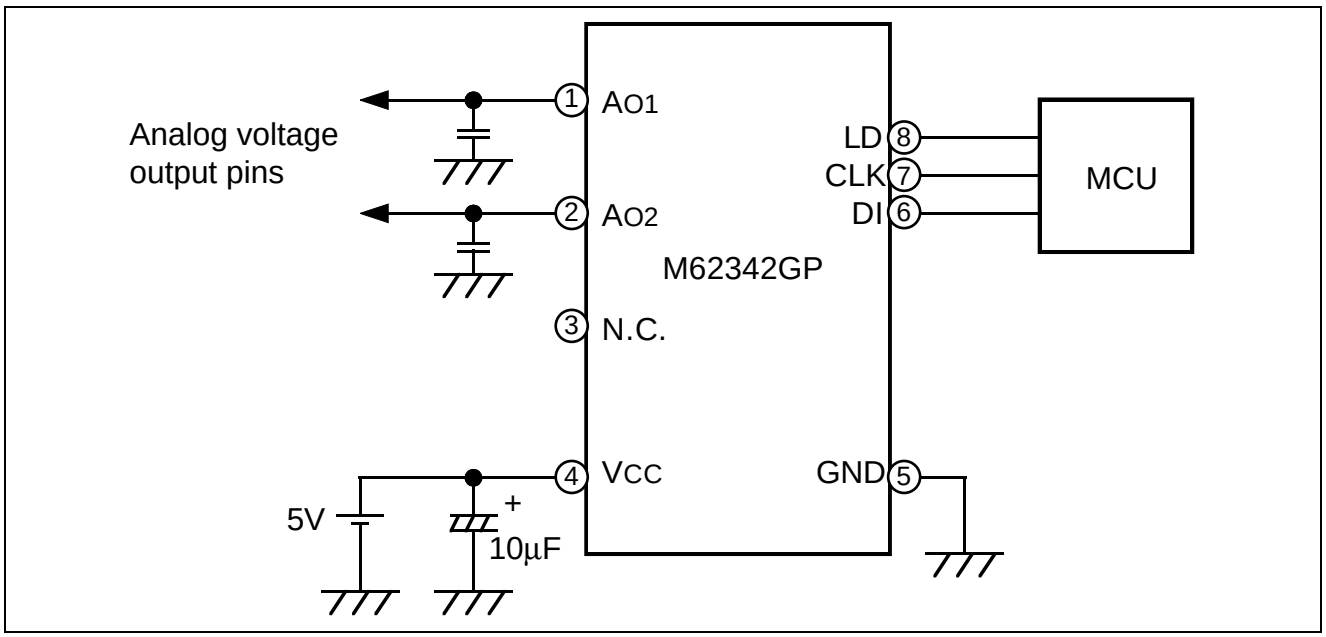
Timing Chart



Usage Notes

1. With this IC, D-A converter upper reference voltage setting is performed by means of the power supply voltage. If ripples or spikes are imposed on this pin, conversion accuracy may fall. When using this IC, a capacitor must be inserted between the power supply pin and GND in order to ensure stable D-A conversion.
2. The output buffer amps of this IC are highly tolerant of capacitive loads. Therefore, connecting capacitors (0.1 µF max.) between the output pins and ground in order to eliminate jitter or noise due to output line wiring presents no problems whatever in terms of operation.

Sample Standard Application Circuit

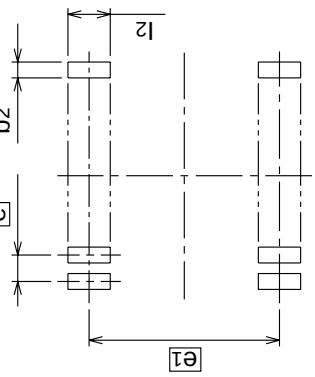


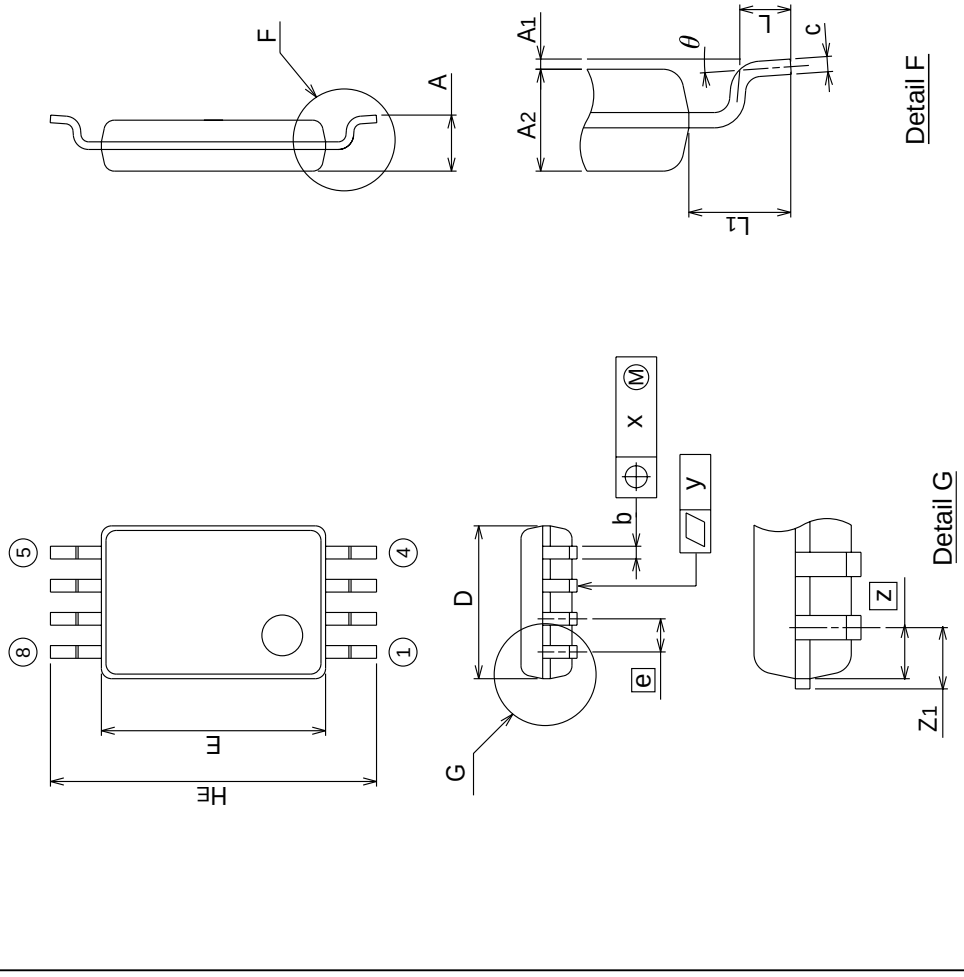
Package Dimensions

Plastic 8pin 175mil SSOP

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.2
A_1	0	0.1	0.2
A_2	–	1.0	–
b	0.2	0.25	0.32
c	0.14	0.15	0.2
D	2.9	3.0	3.1
E	4.3	4.4	4.5
e	–	0.65	–
H_E	6.2	6.4	6.6
L	0.3	0.5	0.7
L_1	–	1.0	–
z	–	0.525	–
Z_1	–	–	0.675
x	–	–	0.13
y	–	–	0.1
θ	0°	–	8°
b_2	–	0.35	–
e_1	–	5.8	–
l_2	1.0	–	–

Recommended Mount Pad





EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SSOP8-P-175-0.65	–		Cu Alloy

8P2J-A

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