

M62333P/FP
M62338P/FP

8-BIT 3CH I²C BUS D-A CONVERTER WITH BUFFER AMPLIFIERS

DESCRIPTION

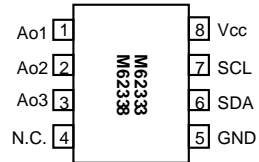
The M62333/M62338 is an integrated circuit semiconductor of CMOS structure with 3 channels of built in D-A converters with output buffer operational amplifiers.

The input is 2-wires serial method is used for the transfer format of digital data to allow connection with a microcomputer with minimum wiring.

The output buffer operational amplifier employs AB class output circuit with sync and source drive capacity of 1.0mA or more, and it operates in the whole voltage range from Vcc to ground.

The M62333 and the M62338 differ only in their slave address.

PIN CONFIGURATION(TOP VIEW)



Outline 8P4 (P)
8P2S-A (FP)

N.C.:NO CONNECTION

FEATURES

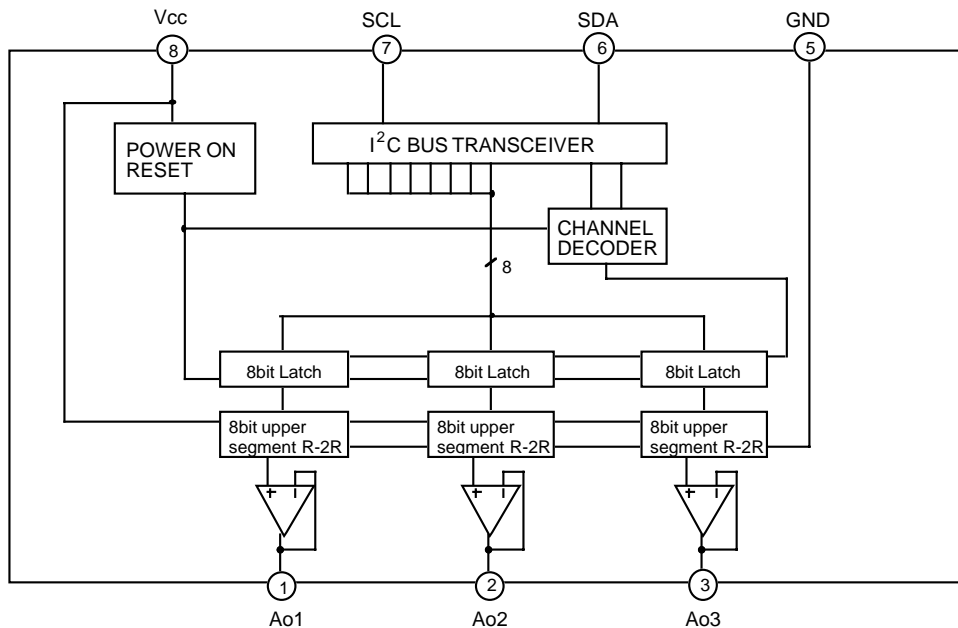
- Digital data transfer format
- I²C BUS serial data method
- Output buffer operational amplifier
it operates in the whole voltage range from Vcc to ground.
- High output current drive capacity
±1.0mA over

APPLICATION

Conversion from digital data to analog control data for home-use and industrial equipment.

Signal gain control or automatic adjustment of DISPLAY-MONITOR or CTV.

BLOCK DIAGRAM



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EXPLANATION OF TERMINALS

Pin No.	Symbol	Function
⑥	SDA	Serial data input terminal
⑦	SCL	Serial clock input terminal
①	Ao1	8-bit resolution D-A converter output terminal
②	Ao2	
③	Ao3	
⑧	Vcc	Power supply terminal
⑤	GND	GND terminal

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		-0.3 to 7.0	V
Vin	Input voltage		-0.3 to Vcc+0.3	V
Vo	Output voltage		-0.3 to Vcc+0.3	V
Pd	Power dissipation		417 (DIP) / 272 (FP)	mW
ToDr	Operating temperature		-20 to 85	°C
Tstg	Storage temperature		-55 to 125	°C

ELECTRICAL CHARACTERISTICS (Vcc=+5V±10%, GND=0V, Ta=-20 to 85°C unless otherwise noted)

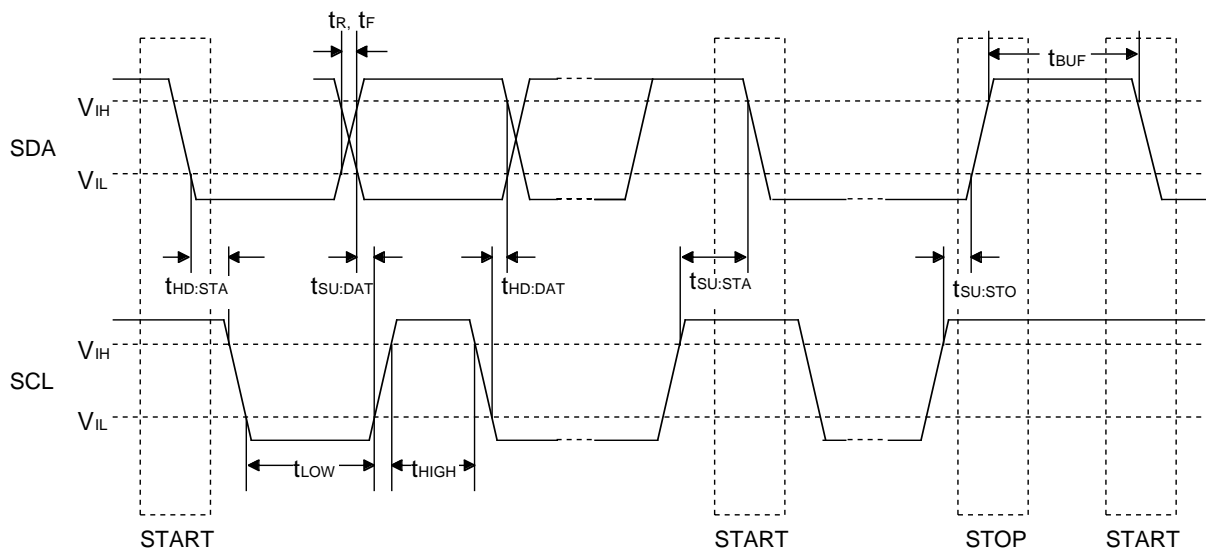
Symbol	Parameter	Test conditions	Ratings			Unit
			MIN	TYP	MAX	
Vcc	Supply voltage		2.7	5.0	5.5	V
Icc	Supply current	CLK=500kHz Operation, IAO=0μA Data : 6Ah (at maximum current)	0	0.9	2.7	mA
		SDA=SCL=GND, IAO=0μA	0	0.6	1.8	mA
IILK	Input leak current	VIN=0 to Vcc	-10		10	μA
VIL	Input low voltage				0.2Vcc	V
VIH	Input high voltage		0.8Vcc			V
VAO	Buffer amplifier output voltage range	IAO=±100μA	0.1		Vcc-0.1	V
		IAO=±500μA	0.2		Vcc-0.2	V
IAO	Buffer amplifier output drive range	Upper side saturation voltage=0.3V Lower side saturation voltage=0.2V	-1.0		1.0	mA
SDL	Differential nonlinearity	Vcc=5.12V(20mV/LSB) without load (IAO=0)	-1.0		1.0	LSB
SL	Nonlinearity		-1.5		1.5	LSB
SZERO	Zero code error		-2.0		2.0	LSB
SFULL	Full scale error		-2.0		2.0	LSB
Co	Output capacitive load				0.1	μF
Ro	Buffer amplifier output impedance			5.0		Ω

I²C BUS LINE CHARACTERISTICS

Symbol	Parameter	Min.	Max.	units
f _{SCL}	SCL clock frequency	0	100	KHz
t _{BUF}	Time the bus must be free before a new transmission can start	4.7	-	μs
t _{HD:STA}	Hold time START Condition. After this period, the first clock pulse is generated.	4.0	-	μs
t _{LOW}	LOW period of the clock	4.7	-	μs
t _{HIGH}	HIGH period of the clock	4.0	-	μs
t _{SU:STA}	Set-up time for START condition (Only relevant for a repeated START condition)	4.7	-	μs
t _{HD:DAT}	Hold time DATA	0	-	μs
t _{SU:DAT}	Set-up time DATA	250	-	ns
t _R	Rise time of both SDA and SCL lines	-	1000	ns
t _F	Fall time of both SDA and SCL lines	-	300	ns
t _{SU:STO}	Set-up time for STOP condition	4.0	-	μs

- Note that a transmitter must internally provide at least a hold time to bridge the undefined region (max.300 ns) of the falling edge of SCL.

TIMING CHART



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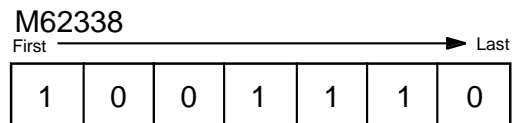
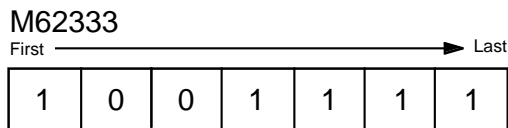
I²C BUS FORMAT



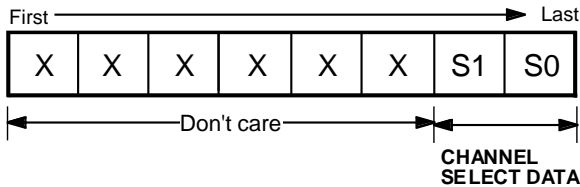
STA: start condition
W: write(SDA=Low)

A: affirmation bit
STP: stop condition

• **SLAVE ADDRESS**



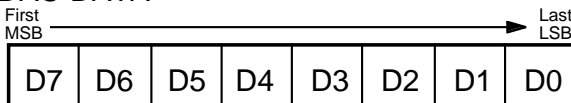
• **SUB ADDRESS**



CHANNEL SELECT DATA

S1	S0	Channel selection
0	0	ch1 selection
0	1	ch2 selection
1	0	ch3 selection
1	1	Don't care

• **DAC DATA**

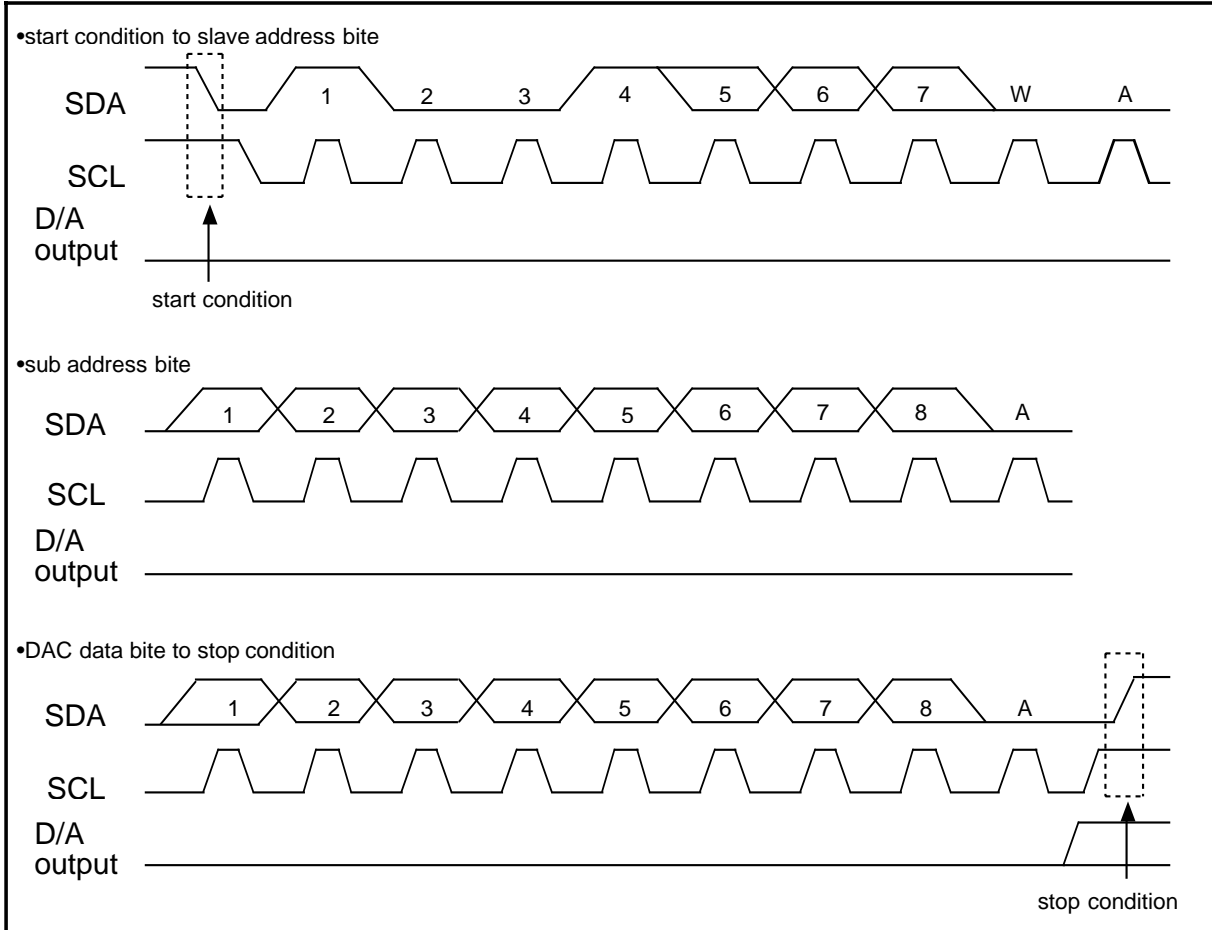


First MSB	D7	D6	D5	D4	D3	D2	D1	Last LSB	DAC output
	0	0	0	0	0	0	0	0	$V_{cc}/256 \times 1$
	0	0	0	0	0	0	0	1	$V_{cc}/256 \times 2$
	0	0	0	0	0	0	1	0	$V_{cc}/256 \times 3$
	0	0	0	0	0	0	1	1	$V_{cc}/256 \times 4$
	:	:	:	:	:	:	:	:	:
	1	1	1	1	1	1	1	0	$V_{cc}/256 \times 255$
	1	1	1	1	1	1	1	1	V_{cc}

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8-BIT 3CH I²C BUS D-A CONVERTER WITH BUFFER AMPLIFIERS

TIMING CHART (MODEL)



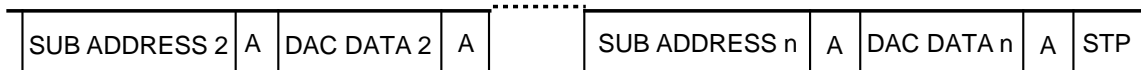
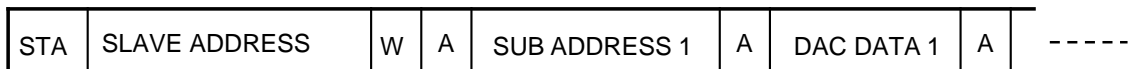
•Start condition With SCL at HIGH,SDA line goes from HIGH to LOW

•Stop condition With SCL at HIGH,SDA line goes from LOW to HIGH

(Under normal circumstances,SDA is changed when SCL is LOW)

•Acknowledge bit The receiving IC has to pull down SDA line whenever receive slave data.
(The transmitting IC releases the SDA line just then transmit 8bit data.)

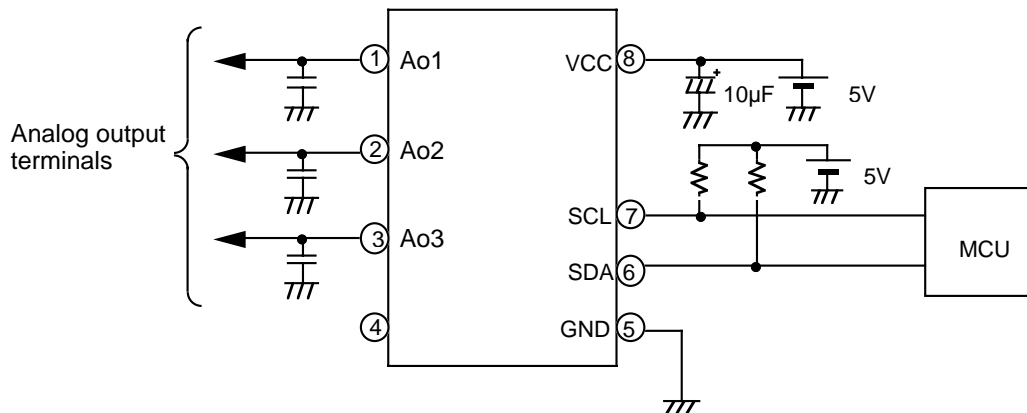
Digital Data Formats



PRECAUTION FOR USE

Supply voltage terminal(Vcc) is also used for D-A converter upper reference voltage setting. IF ripple or spike is input this terminal,accuracy of D-A conversion is down. So,when use this device,please connect capacitor among Vcc to GND for stable D-A conversion.

This IC's output amplifier has an advantage to capacitive load.So it's no problem at device action when connect capacitor (0.1μ F MAX) among output to GND for every noise eliminate.

APPLICATION EXAMPLE**Note regarding I²C BUS**

- Purchase of MITSUBISHI ELECTRIC CORPORATION'S I²C components conveys a license under the Philips I²C Patent Rights to use these components an I²C system,provided that the system conforms to I²C Standard Specification as defined by Philips.

Keep safety first in your circuit designs!

- Mitsubishi Electric Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury,fire or property damage. Remember to give due consideration to safety when making your circuit design, in order to prevent fires from spreading, redundancy, malfunction or other mishap.